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► **To cite this version:**

Aurélie Villard, Alan Lelah, Daniel Brissaud, Marc Mantelli. An eco-design tool for manufacturers of semi-conductor technologies: looking for environmental opportunities in the design phase. 2012 IEEE ISSST, May 2011, Boston, United States. pp.1-6, 10.1109/ISSST.2012.6228013 . hal-00737235

HAL Id: hal-00737235

<https://hal.science/hal-00737235>

Submitted on 1 Oct 2012

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An eco-design tool for manufacturers of semi-conductor technologies: looking for environmental opportunities in the design phase

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Abstract—The paper presents an eco-design methodology, dedicated to semi-conductor components manufacturers. This method aims to increase the designers' environmental consciousness and drive them systematically to explore innovative opportunities that can positively impact the environment during the early stages of design phase.

The method relies on an original LCA-based tool for the environmental analysis of integrated circuits. It is developed in collaboration with a pilot team so as to help them develop and integrate their own eco-design approach. It allows the designers to acquire basic environmental knowledge and know-how during the analysis phase while ensuring high environmental performances of the microchips. The tool is organized into three main axes: characterizing design decisions in terms of impacts; controlling the evolution of new generations compared to older ones; and finding levers for improvement.

The environmental evaluation of a technology under development was initially assessed but as it is a preliminary work, the results were not directly used to design or re-design this technology. This pilot experiment gave encouraging results and validated the method capable of arousing the designers' interest on the environmental impact of their activity. The interpretation of the results allowed the design team to establish trends and directions for improvement for the future technologies they will design.

Index Terms—eco-design, life cycle assessment, semi-conductor technologies

I. INTRODUCTION

As the society has turned into a connected and wired community, the fast multiplication of electric and electronic products contributes to increasing environmental issues like ever-increasing world-wide electrical consumption and considerable production of e-waste. To control these blended exponential developments, design of electric and electronic products have been subject in these recent years to a growing body of environmental legislation e.g. European Union's directives (RoHS and WEEE).

Facing with this higher and higher legislative pressure, finished goods manufacturers which launches their products had to better know intermediate products. That pressure

justifies that an effort has to be done in the semi-conductor industry to design and manufacture cleaner components or at least to better know the environmental impact generated by all these microelectronic components.

Semi-conductor industry usually responds to external pressure on environmental concerns thanks to its natural strategic roadmaps. The semiconductor industry mainstream is driven by a phenomenon, called Moore law, which states that the number of transistors that can be placed inexpensively on an integrated circuit (IC) doubles approximately every two years. This phenomenon induces a positive effect on the environmental because there are more and more components per unit of production, the wafer, for quasi equivalent manufacturing flows between technological generations, called nodes. Moreover, designers are challenged by customers to design low power and energy efficient circuit which drastically reduces the environmental impact of the microchip during its use phase. These trends have lead high technical challenges and have forced designers to be more and more competitive by developing innovative solutions.

II. ECO-DESIGN IN THE SEMI-CONDUCTOR SECTOR

Since designers deal with increasing technological stakes in relation to both the miniaturization of circuits and the search for energy efficiency, up to today, the design effort has been essentially limited to energy saving solutions or to responding to legally enforced restriction of substances [1]. In this context, an assessment in the semi-conductor sector shows that the direct integration of environmental constraints in ICs design is an emerging concern [2], [3].

Drivers in new technologies design comes from standard industrial values: cost, functionalities, size and efficiency. At designer-level, there are other constraints: electrical performances, testability, reliability, choice of materials (avoid banned substances like PFOS in photoresists). Environmental performances are not measured and so cannot weigh in decision-making processes.

Eco-design represents a natural process for industries wanting to assume their role in safeguarding the environment and resources. The constraints linked to environmental impacts become a decisive factor which can be systematically integrated in the earlier stages of technology development. There have been several previous approaches [2], [4], [5] to

develop environmental design and evaluation tools for the semi-conductor industry. Murphy [6] developed a parametric model to predict changes in inventory in wafer fabrication process. Somani [7] provided a “rapid methodology for evaluating new process options”. The direct duplication of such methods for a given company poses several problems due to their theoretical complexity, the nature of the necessary information or the in-house organization of work in the company.

The paper describes an eco-design tool, based on a process-level approach and supported by advanced environmental analysis. The tool is dedicated to manufacturers of semi-conductor technologies working in a specific industrial context. First, the method for environmental evaluation of IC technologies is described. Then the functionalities of the tool are described and finally a demonstration is done on an under-development technology.

III. ENVIRONMENTAL EVALUATION OF IC TECHNOLOGY

A. IC technology description

The manufacturing of an IC is a complex process with the trend of being more and more intricate. The “manufacturing route” is made of more than four hundreds steps. The specificity of IC lies in the fact that a lot of secondary materials, which does not remain on the final microchip, are used during the manufacturing phase [8].

The basic pattern is the transistor, drawn on a silicon wafer substrate. Metallic interconnections between transistors, in copper or aluminum, determine the specific function of the electrical circuit. To draw features on the initial silicon substrate, the successive poly-silicon, oxide and metal layers, a series of successive photolithographic and etch loops are applied to the wafer: more than 40 loops and as many photolithographic masks are likely to be used for the more complex ICs. Then, a manufacturing process flow can be divided in “modules”, which correspond to specific “mask levels” and so process loops.

For instance, for the module “definition of the electrode of a transistor”, the process sequence is: photolithography, doping and photoresist removal; whereas for the module “formation of via between two metal layers” –to establish electric connections- the sequence is: photolithography, etching, photoresist removal, material deposition and polishing. Depending on technology specificities, this sequence can vary with extra cleanings, decontaminations and hardenings.

B. Applying LCA to IC technology

Life cycle assessment (LCA) was selected as the support for designers for marking design option regarding a large spectrum of environmental impacts [9]. LCA is a tool used for drawing the profile of a product, which means determining the potential environmental impacts generated by this product over its full life cycle. Since the last decade, environmental analysis of microchips has been progressing towards LCA [10]-[11]. However, it is important to keep in mind that main challenges still remain in developing LCA tools to improve data modeling, keep pace with technology changes and handle uncertainty [12]-[13].

In our case, seven indicators are considered: they are called μ -KEPIs for “Key Environmental Performances Indicators for microelectronic industry”, related to the main concerns of semi-conductor manufacturers. The seven μ -KEPIs, μ_1 to μ_7 , are (without any order of magnitude): greenhouse effect, abiotic depletion, eutrophication, eco-toxicity in water, photochemical oxidation, electricity consumption during manufacturing and water consumption during manufacturing. As illustrated in Fig. 1, the scope for LCA is cradle to gate: IC life cycle starts when raw materials and energetic resources are extracted from the soil and finishes at the end of manufacturing.

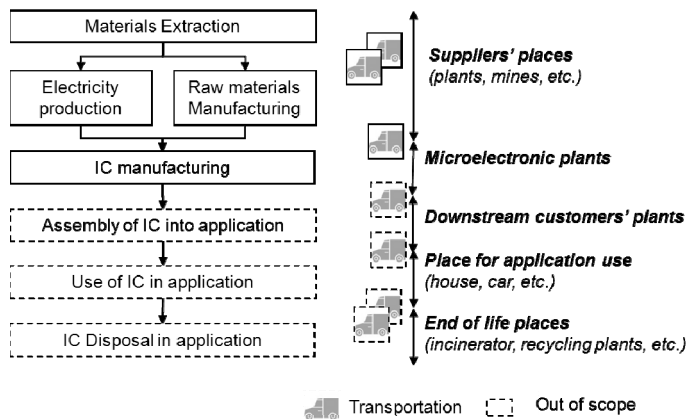


Fig. 1. Overview of the IC system: life cycle and scope for LCA

Practically, to assess the environmental analysis, material and energetic flows, in-coming or out-coming are inventoried. The Table I summarizes the data needed and the system implemented to collect them based on an industrial context.

Table I. Data collection

Data	Source
Process parameters (raw materials quantity, time)	“Recipe”, document managed by Process Engineer
Power of equipment (Watt)	Electricity facilities
Raw materials properties (composition, density, suppliers location)	Material Safety Datasheet
Raw and energetic materials impacts (environmental impact per kilogram)	Eco-Invent database
Treatment of chemical waste treatment (gas abatement, waste destination and waste water plant)	Environment service of the industrial plant

Any IC system is complex to model for LCA perspectives. A specific scope is required which is different from the one established for conventional products. Williams [14] developed the concept of the secondary materialization. It was the proposition that “increasingly complex products require additional secondary materials and energy to realize their lower entropy form”. In other words, the model for an IC is focused on the secondary raw materials used during manufacturing rather than on its structure or composition. A LCA is assessed separately on each manufacturing process step. Then the impact of the technology is the sum of the impacts of all the elementary process steps.

C. Use LCA to assess IC technology alternatives

LCA is used to compare a situation to its initial situation. The relative evolution of a new item N compared to parent item P is monitored with the deviation stated in percentage, for each μ -KEPIs (1). $I(N; \mu_i)$ refers to the μ -KEPI impact of the new item N on the μ_i . An item can be a technology, a module or a manufacturing step. The deviation can be stated independently in that way on the 7 μ -KEPIs.

$$Dev(N/P; \mu_i) = [I(N; \mu_i) - I(P; \mu_i)] / I(P; \mu_i) * 100 \quad (1)$$

In some cases, the trend – diminution or augmentation of the impact- can be different on the 7 μ -KEPIs. Then the environmental status of N compared to P , is stated with a single indicator, $e-Dev(N/P)$ (2).

$$e-Dev(N/P) = \sum_{i=1}^7 Dev(N/P; \mu_i) \quad (2)$$

The value of $e-Dev$ defines if the change is benefit considering the environment (table II).

Table II. Environmental status according e-Dev value

Case	e-Dev value	Environmental status
1	$e-Dev(N/P) > 10\%$	P is better than N
2	$e-Dev(N/P) < -10\%$	N is better than P
3	$0\% < e-Dev(N/P) < 10\%$ and all $(Dev(N/P; \mu_i) > 0)$	P is better than N
4	$-10\% < e-Dev(N/P) < 0\%$ and all $(Dev(N/P; \mu_i) < 0)$	N is better than P
5	$ e-Dev(N/P) < 10\%$ and at least two $Dev(N/P; \mu_i)$ have different signs	No decision are taken to discriminate N to P

Some precautions have been taken to avoid inappropriate understandings by designers who are not experts in LCA results interpretations: in the fifth case, any conclusion must be done by a LCA specialist and the results are compared to in-house thresholds, fixed in function of company strategic choices.

IV. TOOL DESCRIPTION

A. Expectations from an eco-design tool

For the deployment of a tool for eco-designing an IC technology, a designer-centered method was applied. The technologists' specificities were considered and mainly the data they can provide in the earlier stages of development. An opinion survey helped to define the outline of the results they judge to be useful and easy-to-use. The following of this section describes the automatic interface for simulating the process flow options during development of a semi-conductor technology by the technology designers, called technologists.

Eco-design tool for technologists is applied on technologies under development that are not yet materialized. It is organized around three axes:

- Characterize environmental performances of design options
- Control evolution of new generations compared to previous generations and so limit impacts of future technologies
- Find areas for improvement by underlining weak points.

In order to fulfill the three goals, the main stage consists of acquiring a better knowledge of the effect on the environment of the technology manufacturing, thanks to LCA analysis.

B. Quick LCA for IC technologies

Technologists' constraints are carefully evaluated to be in line with day-to-day tasks: the involvement is ensured more efficiently if the time allocated to the task is optimized and its complexity easily manageable.

The technologists are in charge to make evolving already existing technologies and improving their performances. They are neither radically creating new processes nor dealing with complex technological leaps. Hence, a strongly simplifying hypothesis is made: there is no radical design; the technologies are designed by analogy. So it is assumed that there is already the exact or a close version of all the elementary process steps used for manufacturing the IC, most materials has been already tested and the equipment properties are known. In terms of environmental pollution, that means that the evaluation can be easily managed if we consider that all the elementary recipes have been at least once used in the plant.

To do this, an option for assessing "Quick LCA" has been specifically developed for describing technology structure. Indeed, at the first stages of the design, the exact manufacturing route of the technology is not yet fixed: according to the functional specification, the technologist describes its technology in terms of structure and nature of different modules. According technologists experience, 20 key-parameters have been identified for modeling any non-volatile memory (NVM) technology. The technologists define a new key-parameter when a new structure is created.

The technologist specifies the changes compared to the referent technologies based on these key parameters. For instance, the key parameter "salicide" – which is an alloy used to minimize parasitic resistance between silicon parts and metal levels – depends of the material forming the layer and its thickness: if at least one of these parameters is modified, in-coming and out-coming flows can be deduced from assimilated modules.

"Quick LCA" option gives the opportunity to quickly deduce the μ -KEPIs of a new technology by downloading μ -KEPIs of parent technologies. The only condition is that parent technologies have been already evaluated and that their key parameters and associated μ -KEPIs are recorded in a database. In some cases, a module has already been elaborated but needs major updates to match the new technology specificities. Then, it is interesting to go deeper into the details and so evaluate directly the impact of a new module with a specific LCA. It is particularly advised when the sign of the deviation cannot be deduced instinctively or when the manufacturing technique is innovative.

C. Processing of results

Once "Quick LCA" is applied to the new technology, projected environmental impacts of a technology were known several months before its industrialization.

LCA results processing permits to identify hotspots: the main contributions to impact categories (emissions, raw materials,

chemical substances, water or electricity) are computable so as to the most impacting modules or manufacturing steps.

Moreover, the technologist has the opportunity to compare two design options (e.g. two materials forming the salicide) and observe their effect on the environment. Indeed, the calculation of deviation between two options is automatized.

A database in a searchable format is available for consultation: it provides a “ranking” of the deviation between modules. It can be easily translated into guidelines e.g. “CoSi₂ Salicide - 2000 Angstroms” is preferable to “NiSi₂ Salicide - 2000μm” or “Back-end of line copper” is preferable to “Back-end of line Aluminum”.

Eco-design measures can be proposed at the end of the process. At this stage of the design, the manufacturing route is not yet fixed: the presentation of the different LCA results highlights hotspots and the technologist gets enough time and margins of freedom to modify the most damaging modules – at the condition of having unchanged quality and performance characteristics.

V. APPLICATION OF THE TOOL TO A DESIGN REVIEW

A. Preliminary work

The tool is tested by a R&D team on an under-development technology *N*. This demonstration occurs during a design review. The development of an IC technology takes about two years. Regularly during this period, the design team joins together during design reviews to evaluate the job achieved by the different actors and to make a point on the future steps. At this design stage, most of technical specificities of the technology *N* are fixed but no sample has been yet tested.

The team is constituted with 5 technologists and a project leader. The experimentation aims at measuring, by means of the eco-design interface, the future environmental impact of this technology *N* once it will be industrialized and ready to be integrated in its final electronic application.

The technology *N* is designed in order to answer new technical specifications in terms of functionalities and dimensions: IC size, electricity consumption and memory access time will be decreased.

Three technologies have been identified by the project leader as parent technologies coming from older technological nodes. They are numbered as follows *P*₁, *P*₂ and *P*₃. The technology *N* has mixed characteristics coming from these pre-existing technologies but they are all NVM technologies, based on same 90nm node. So process route of technology *N* has similarities with the parent technologies.

Once the μ-KEPIs of the three parent technologies and theirs recipes are recorded, the environmental evaluation of the technology *N* can be assessed with R&D team help.

B. During design review

As a reproduction of the tool interface, Table III and Table IV summarize the data collected during the meeting. Grey boxes were filled by activating drop-down menus. For 14 Type-A parameters, the technologists reply to a theoretical path of questioning: the most likely key parameters, the maturity status of each parameter (*already existing* or *new*) and in the first case which is the parent technology. The technologists

have the possibility to mention other modules not included in Type-A parameters.

For the Type-B key-parameter, the technologists capture the value directly. Finally for Type-C key-parameters, the technologists answer by “yes” or “no” for describing the types of transistor embedded into the technology.

Table III. Technologists’ answers for Type-A key-parameters

Type	Key parameters	Status	Parent technology
A : specify if the module is “new” or “existing”	Cell	Existing	<i>P</i> ₂
	Active	New	
	Matrix	Existing	<i>P</i> ₂
	Floating gate	New	
	Salicide protection	Existing	<i>P</i> ₁
	Salicide	Existing	<i>P</i> ₁
	Contact	Existing	<i>P</i> ₂
	Spacer	Existing	<i>P</i> ₁
	Back end of line	Existing	<i>P</i> ₁
	Last aluminum layer	Existing	<i>P</i> ₁
	Poly-metal dielectric	Existing	<i>P</i> ₁
	Gate	Existing	<i>P</i> ₁
	Inter-metal dielectric	Existing	<i>P</i> ₁
	Passivation	Existing	<i>P</i> ₁
A: Specify non-mentioned modules	Extra module 1 : Floating gate doping	Existing	<i>P</i> ₂

Table IV. Technologists’ answers for Type-B and Type-C key-parameters

Type	Key parameters	Value
B : capture value	Metal layers	5
C : select “yes” for embedded transistors; if not select “no”	High voltage	yes
	Low voltage	yes
	Medium voltage	no
	Ultra high voltage	no
	High speed	no

Only two of the three parent technologies, *P*₁ and *P*₂, were useful to conduct the analysis on the technology *N*. No new structure has been planned to be designed for this technology. For “active” and “floating gate” modules, specific LCAs must be assessed with the current primary knowledge at this stage of the design.

The case presented in this section for illustrating “new LCA” studies a change of the manufacturing conditions in the definition of a floating gate (FG) module. Floating gate is a specific structure of non-volatile memories used as a memory cell to stock electrons.

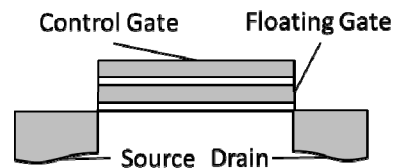


Fig. 2. Cross-section of a transistor floating-gate

The process sequence to form the FG is: poly-silicon deposition, photolithography for FG doping, ionic implantation in FG, photoresist removal, cleaning, photolithography for FG feature definition, cleaning, FG etching and photoresist removal.

Because of the dimension shrinks, 3 process steps are modified in the new module *N* compared to the module from which it is inspired *P*: the FG doping by ionic implantation,

the photolithography for the FG definition and the FG etching (Table V). As the flow is not yet frozen, the evaluation of new process modules requires assumptions on the recipe parameters (duration, chemicals flows, etc.). The benefits or losses in terms of environmental performances are not a priori obvious because there are several changes into recipes.

Table V. Description of the changes in floating gate module

Process step	Changes in structure	Changes in recipe
Doping	Less deep implant : energy of ionic implantation is decreased	Less energy consumed Lower quantity of gases
Photo-lithography	Smaller dimensions increase the risks to have line collapse so the thickness of photoresist is decreased.	Small variations of time (<1%)
Etching	Smaller dimensions increase the risks of defectivity (default due to wrong patterns). The profile of the etching into the line is changed.	Different recipe. Lower consumptions: Cl ₂ , HBr, CF ₄ Higher consumptions: CH ₂ F ₂

In changing the structure of the module “floating gate” and modifying its associated processes, LCA stresses that the module is improved compared to the previous generation and so the environmental pressure of the future microchip is reduced (Fig. 3).

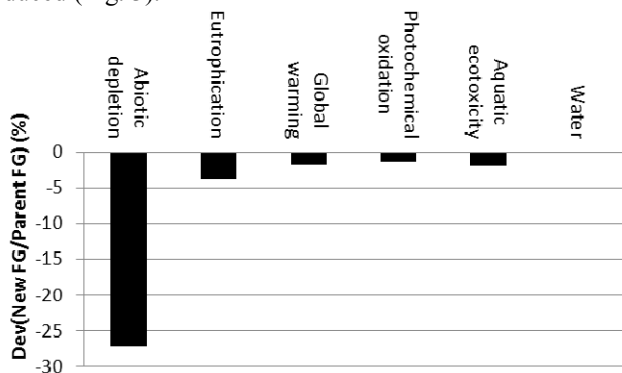


Fig.3. Illustration of the environmental benefit from “parent FG module” to “new FG module”

C. After the design review

The interpretation of the results gives rise to an extra meeting with the R&D team. Fig. 4 shows one of the graphs displayed: the environmental impacts of the technology *N* compared to the parent generations regarding global warming potential.

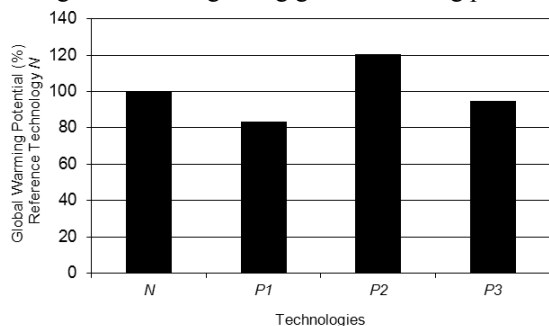


Fig. 4. Environmental impacts for technology *N* and its parent technologies

Pareto graphs for each μ -KEPI are computable: the ten most damaging areas, the ten most damaging elementary steps, the sources which together count for more than 90% of the damage. The interpretation of these graphs allowed the R&D team to establish trends and directions for improvement and several ideas arose on how to improve the performances of the technology *N*.

Since copper has been used for forming metal layers in “back-end of line” module, the quality of water through of the indicator “aquatic eco-toxicity” has been considerably deteriorated: a survey has been opened for decreasing copper consumption and consequently emissions of copper particles in wastewater. One suggestion is to decrease the thickness initially deposited of each copper line and then to create a more accurate process to remove the excess material by CMP (chemical and mechanical polishing).

Same kind of work has been asked to engineers responsible of wet benches for wafer cleanings, for decreasing ultrapure water consumption which is responsible for 16.5% of eutrophication effect.

Besides to measure environmental impacts of new techniques, the experiment gives rise to other surprising observations. In FG module, the photoresist thickness for UV insolation is decreased. However, at process level, the volume of photoresist required to be deposited on the wafer is the same as previously. Indeed, the volume of photoresist coated on the wafer is a constant whatever the requested final thickness is. This volume is defined by the properties of the material like its viscosity. The thickness remaining is defined by the rotation speed of the plate on which the wafer lies and the excess is eliminated by centrifuge effect (Fig.5).

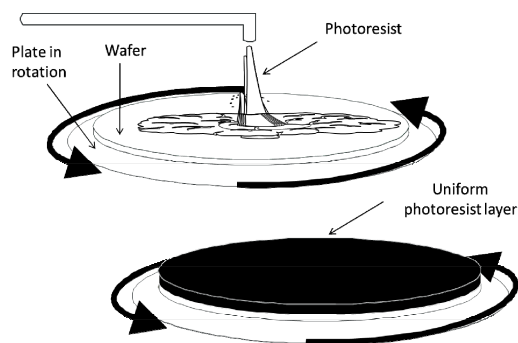


Fig.5. Schematic representation of the deposition of photoresist on the wafer

Whereas all environmental aspects are improved in the FG module, the benefit is particularly important for the indicator “abiotic depletion”. Indeed, in the CML indicator for abiotic depletion, the substance “xenon, in air” is the fifth most sensitive contribution [15]. Xenon is poorly used in microelectronic industry but it used in ionic implantation to create a plasma close to the wafer surface to make electrons available for the deepest levels, and so avoid charging effect. Just the fact to reduce the process duration of 10 seconds per wafer in FG doping will allow a drastic diminution, 74%, of the deviation of the ionic implantation regarding abiotic depletion effect.

VI. CONCLUSIONS AND PERSPECTIVES

The environmental evaluation of an under-development technology has been successfully assessed thanks to the collaboration with a design team. It was part of the elaboration and test of a prototype tool presented in this paper. It was expected from this prototype tool to show designers that environmental criteria could be systematically included into their decision-making process. This experiment was a first step of eco-design in this R&D team and gave several perspectives before envisaging to be used systematically for eco-design perspectives. First of all, it has proved that environmental assessment of new technology is possible.

In such an eco-design process, the collaboration and active participation of all the design team is required. This method could be systemized and integrated into day-to-day work only if it is not introducing unreasonable constraints on the workload: the time allocated to this new task should be minor. That is why designers' constraints were carefully evaluated to be in line with their day-to-day tasks. Mainly, the use of a simplifying hypothesis that design is mostly made by analogy has been appreciated and supported: each time a LCA of a technology, a module or a process step is assessed, the seven μ -KEPIs are recorded in a database. The more the knowledge of old technologies accumulates, the more the range of manufacturing processes that are covered grows and so the quicker the evaluation of future technologies will be.

For future deployments, the integration in STMicroelectronics of a parametric model at process level as the one proposed by [6] is wished. It will permit to deduct the environmental impacts of future technologies at a process unit level. Moreover, the key-parameters are bound to change when other technologies like MEMS components will be modeled and when technologies will reach other technological nodes. Indeed these changes will cause the creation of new cells and structures.

This experiment has validated a method able to make aware designers about environmental aspects without any unreasonable constraints. Even if the approach has not been used and integrated for design, the designers were aware about environmental impact of their activities and that any design decisions are likely to modify the environmental impacts of the future microchip. The interpretation of the results allows the whole design team to discover environmental properties of the ICs life cycle.

ACKNOWLEDGMENT

The authors wish to thank all the members of Rousset Technology Center of STMicroelectronics, for providing support and creativity during this project.

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