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To cite this version:

Fabrice Caignet, Nicolas Monnereau, Nicolas Nolhier, Marise Bafleur. Behavioral ESD Protection Modeling to perform System Level ESD Efficient Design. Asia-Pacific Symposium on Electromagnetic Compatibility (APEMC), May 2012, SINGAPORE, Singapore. pp.401-404. hal-00722644

HAL Id: hal-00722644

https://hal.science/hal-00722644v1

Submitted on 2 Aug 2012

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Behavioral ESD Protection Modeling to perform System Level ESD Efficient Design

Fabrice Caignet, Nicolas Monnereau, Nicolas Nolhier, Marise Bafleur

***Abstract*—For both Equipment Manufacturers (EM) and semiconductor suppliers, the prediction of ElectroStatic Discharge (ESD) events into design phase is becoming a challenging issue to insure rehability into system level considerations. This is mainly due to the shrinking of Integrated Circuits (IC) technology, which decreases the robustness level and increase the probability of failures. In this paper, we will present how to build IC's models taking into account behavioral description of ESD protections, to perform system level ESD simulations. The IBIS (Input/output Buffer Information Specification) models are mixed with information extracted from Transmission Line Pulsing (TLP) measurement's techniques to build system simulations. The methodology is detailed and proved in some case studies addressing the current propagation path and the susceptibility of the ICs. The main goal of the proposed model is that it could be shared by IC suppliers and EMs to ensure that ICs can handle system level ESD events.**

***Index Terms*—System Level ESD, EMC, IBIS.**

I. Introduction

WITH the explosion of electronic products and the failure's requirements of EM, it becomes more and more difficult to estimate what would be the impact of an ESD on ICs depending on the system implementation. The test method for system level stress is defined for example in the IEC61000-4-2 standard [1]. ESD requirements are even more severe on circuits with "global pins" tied to connectors and directly exposed to external aggressions of a system. The level of ESD stress required during the system qualification is increasing over the years. We also observe a trend where the robustness decreases with technology nodes evolution [2].

To ensure that chips can handle system level ESD events, EMs face the problem of the lack of information concerning the internal ESD strategy of the ICs. The same problem was observed few years ago concerning signal integrity (SI), and gave birth to the IBIS standard[3]. This file contains behavioral data of parasitic elements (of package, inputs and outputs) and description of buffers that are needed for SI simulation. The main advantage of IBIS is to provide exchangeable information that help EMs. Keeping the concept of IBIS description, we proposed to build the IC models with both IBIS and ESD protections to perform System Efficiency ESD Design (SEED) according to the methodology presented in figure 1. This methodology, based on a previously published work [4], is intended to model a system composed of digital ICs mounted on a Print Circuit Board (PCB).

The simulation is set with the assembly of "LEGO-like" blocs following the hierarchy of the system composed of multiple elements: ICs, PCB lines, passive components and the test bench environment. In previous studies we have developed a system level methodology based on a hierarchical view [4], [5], [6] using VHDL-AMS [7]. The more complex part is to implement, into the behavioral model of the IC, sufficient and accurate elements to be able to predict both robustness and susceptibility during ESD events.

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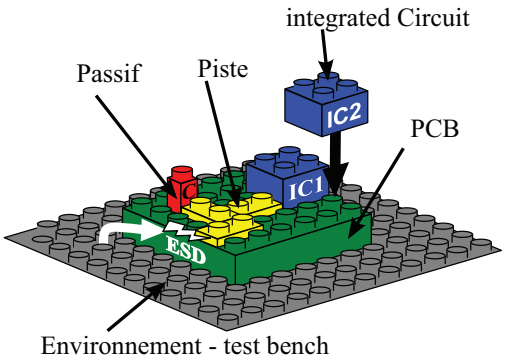

Figure 1. ESD system level modeling methodology

Our first approach is to look at the IBIS information that have to be kept in order to perform SEED. The concept of SEED have been proposed by the ESD Association to provide solutions to fixe system level ESD, to both EM and IC suppliers. The second step will be to build the behavioral description of the ESD strategy from TLP measurements, and to combine these models with IBIS to elaborate the final IC model. We will then prove that very simple models can give accurate results over simple cases of study. To validate the approach the proposed behavioral models of the on-chip protections are compared with physical models. Finally, to point out the importance of such behavioral description, two points of view will be addressed : the EMs who face the problem of mis-informations and the IC suppliers that have to achieved the ESD strategy of the IC from a large variety of basic component's implementations.

II. Behavioral description of the IC

A. Advantages and limitations of IBIS models

ESD signals have high di/dt and so, the parasitic elements of IBIS are important to estimate the dynamic of the current that goes inside the chip and to the IC protections. In previous works [4], we have demonstrated that during normal operating conditions the parasitic elements of IBIS and the passive components of the board can create complex events like delayed-triggered of snapback protections, and forces the

current path leading to the destruction of the ICs. An example of complex, and non predictable shape is reported in Figure 6. This example extracted from [4] details that IBIS inductances have to be implemented into the IC model. The paper also shows that drivers (from IBIS) drive part of the current.

The IBIS files allow simulating complex ESD events, but they are not sufficient to perform whole simulations. They are not sufficient to predict fault as shown in the paper [5], where the probability of failure was investigated. IBIS contains I/V data of the diodes between Input/output and VDD (called Power clamp in IBIS), and to ground. These diodes are static ones and are only given from -VDD to 2*VDD, which is a too small range for ESD events. Moreover, IBIS suffers from a lack of information concerning the central power clamp (PC) protection between VDD and VSS, which is crucial for the ESD strategy. An equivalent model of the IC used in paper [4], extracted from IBIS file, is reported on the schematic of Figure 2.

IBIS has to be extended with full strategy protection description to build the IC model. The idea is to replace the I(V) characteristics of the given diodes by new I(V) curves, and to add the protections not defined, and above all, the Power Clamp (PC) between VDD and VSS. Then, a full behavioral description of the ESD strategy is built. To keep the IBIS concept, no prior knowledge of IC internal structures would be available, which is often the case for system designers at OEM level. Measurements are needed to extract information about ESD protections of the chip. TLP tester and curve tracer are used to extract quasi-static and static characteristics between each pair of IC pins. From these measurements, three types of devices were identified in the example reported in paper [4], all assembled in a classical strategy protection as show in figure 3.

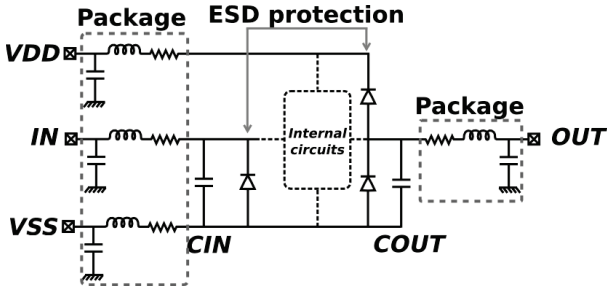

Figure 2. Equivalent IC model obtained from IBIS [4]

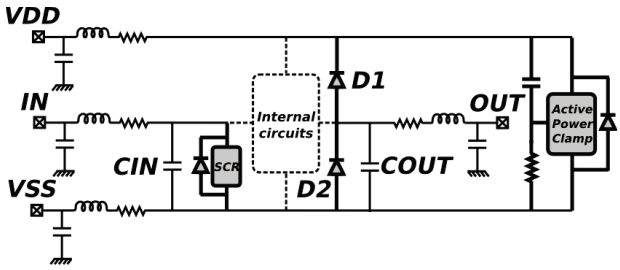

Figure 3. Modified IC model including new ESD protection strategy and parasitic elements of IBIS [4]

B. Behavioral description of the protections from TLP measurements

Various sorts of components can be extracted from the TLP measurements, like simple diodes, or more complex structures with snapback, like Silicon Controlled Rectifier (SCR), or structures that clamp with dynamic conditions (triggered MOSFET - PC). From all these structures we proposed to use the most simplified I(V) characteristics possible. Due to the high current of ESD stresses, small disagreements are not important regarding the accuracy. Moreover, behavioral models don't reveal any knowledge of ESD protections and can be exchengeable between IC suppliers and EM.

1) Diodes: Diodes are good examples to expose the philosophy. Only two parameters can be given like the triggering voltage, Vth, and the on-state resistance, Ron. This defines a very simple two states machine diagram. When the voltage across the diode is under Vth, the diode is off (State 0), no current flows into the protection. Otherwise we are in state 1 with the equation is V=Ron.I.

2) Snapback: For snapback protection the same philosophy is used and defines 4 states, reported on the measured I(V) curves (Fig. 4 a), and following the state diagram reported in fig. 4.b. Six couples of voltages and currents are defined as parameters. These (Vx,Ix) couples define the inflection points of the SCR and the equivalent equations for the states 0, 1, 2 and 3. The model has been used in previous works for simulation of ESD stress injection (TLP and IEC 61000-4-2) [8], [6]. Such model could suffer from convergence issues, but this is solved by adding in parallel to the SCR, the equivalent parasitic capacitance (often given into IBIS). It prevents the internal voltage of the SCR from a strong drop.

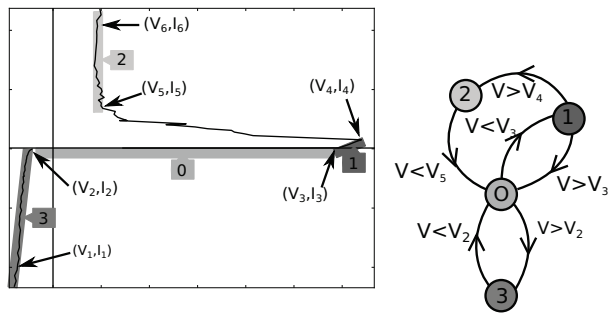

Figure 4. Parameters to build the state machine of an SCR

3) Power Clamp (PC): PC are based on MOS transistors with complex triggering conditions. Basically they are built around a strong MOSFET driven by an RC-triggered structure. The proposed behavioral model is a two state machine, defined like diodes, but the triggering condition is set on a dV/dt without knowing the effective RC delay. A similar structure has been implemented into the study of paper [8]where the susceptibility of failure is compared with measurements into Direct Power Injection (DPI) configuration [9]. The PC drives part of the current during the stress, reducing the failure level that could be predicted using only IBIS information.

Validation of behavioral models into ESD strategy: Finally we need to check that the models are valid on discharge paths that involve more than one protection element. In all available cases, we observed a discrepancy lower than 20 %. One of the largest discrepancy results is shown on Figure 5 for a stress from Out to Vss pins, of the ESD protection strategy presented in figure 4. One limit of this modeling approach is that serial resistances might not be extracted properly as they are extracted only for individual protection devices (pin to pin).

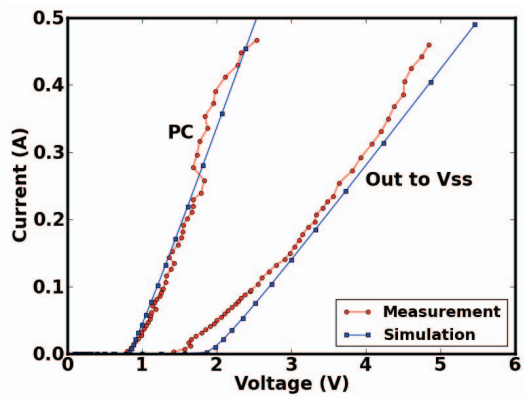

Figure 5. TLP measurements and simulations of the Power Clamp (PC) (Vdd to Vss) and of Out to Vss stress that combines two protection elements (diode + PC)

III. Validation of the accuracy of behavioral description

It appears that a combination of IBIS information (parasitic elements and buffers) with a full behavioral description of the ESD protections is used for the whole IC model. The new circuit model added to the modeling methodology [4] allows analyzing the system behavior during an ESD disturbance, and predicting its susceptibility regarding system level ESD. The IC model is combined with PCB lines, passive components (including external decoupling capacitance, DC block...) and all the test-bench elements (including generator, oscilloscope and cables) hierarchically by following the topology of the system. The figure 6 reports a TLP stress injection between OUT and VSS, in the configuration presented figure 3, while and external decoupling capacitance is placed between VDD and VSS (the current going out of the chip on pin VSS is computed). Without the external capacitance, all the stress goes through the ESD strategy as expected. With the external capacitance, a complex shape is observe mainly obtained by parasitics elements (positive and negative pics are dued to the package inductances).

In Figure 7, the stress is injected into the input pin of configuration of Figure 3, with and without an external decoupling capacitance. A stronger peak current than expected is observed. Its amplitude is determined by the inductance of the package and the high frequency elements of the external capacitance. The simulations show that both physical and behavioral models of the protections give the same results. this is mainly due to the fact that the parasitic elements play a more determinative role than the protections, which have a very low intrinsic resistance (lower than 1Ω).

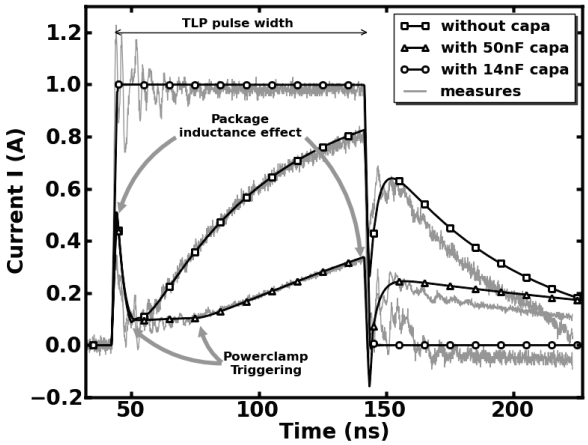

Figure 6. Measurement and simulation comparison of a TLP stress injection between output and VSS with and without external decoupling capacitance [4].

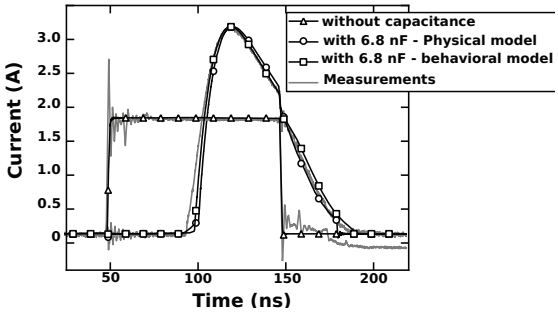

Figure 7. Measurement and simulation comparison of a TLP stress injection between IN and VSS with and without external decoupling capacitance.

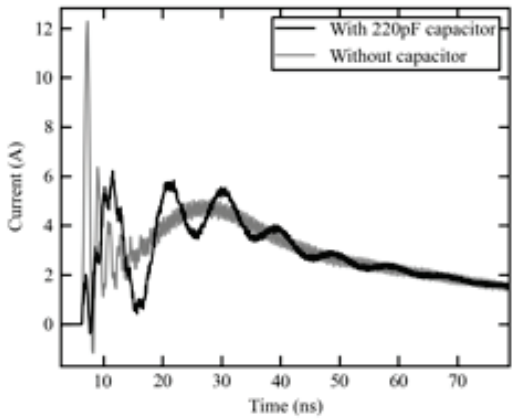

Figure 8. Simulations of the current in function of time, which flows through the ESD structure for 2kV GUN pulse, injected from LIN pin to ground, without and with 220pF external capacitor [6].

In these both examples, the proposed behavioral models obtained by TLP measurements, in addition with IBIS models, fit well with the measurements. The behavioral models give a good accuracy, even for complex current paths involving more than one structure.

Such methodology has been used to investigate IEC 61000-4-2 injection on the LIN driver pin of an automotive component [6]. The IC have to survive in both configurations : with and without capacitance connected to the pin. So, to develop the internal ESD protection structure and strategy, IC designers have to predict the impact of the external capacitance into final system level conditions. The current going into the ESD structure, which is an SCR, has been predicted and is reported in figure 8, the stress injection is 2KV, 8A peak. As it can be noticed, there is a great difference between the two configurations, with and without the external capacitance. This lead to a protection structure that have to survive even for a strong peak current which is 3/2 higher than the injected stress (12A for 8 A injected), and for a classical HBM stress. This great difference can not be predicted without taking into account the whole system in the simulation, and so, behavioral description is helpful to define the ESD structure constraints.

The proposed models based on state machine diagram of the protections were compared to physical models [10] and the simulation time is reported in Figure 9(b). SCR and power clamp (PC) structures have been placed in the same system level condition (Simple one - Fig 9 (a)). Compared to semi-empiritical models the simulation computing time of the behavioral can be more than, one decade faster for SCR and 3 decades for PC structures, for high di/dt. From IC supplier point of view this allows the design of complex ESD strategy with a lot of protections, reducing the time analysis.

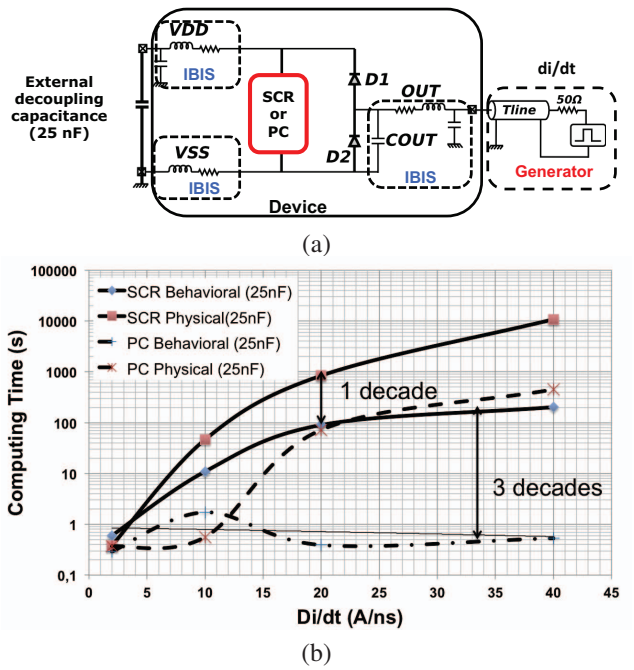

Figure 9. (a) Basic system level configuration to test the computed time. (b) Comparison of the computing time of physical and behavioral models

IV. Conclusion

To face the complexity of predicting the impact of ESD at system level, the designers need information from the ICs. The information can only be obtained if there is a high level of abstraction of the internal ESD strategy of the ICs. We propose, keeping the philosophy of IBIS files, to improve IC model with full behavioral ESD protections models that protect the intellectual property of semiconductor's manufacturers. The models we suggest are based on state machine diagram, with a minimum set of parameters like resistances and inflection points. We demonstrate that these models are sufficient to predict with good accuracy the current path, and so, the impact of ESD discharge. To summarize figure 10 reports the requirements to build the IC block. Both system designers and IC suppliers can use such models. This work is under development at the ESDA working group WG14- "System Level ESD", and the results of the discussions have to be discussed...

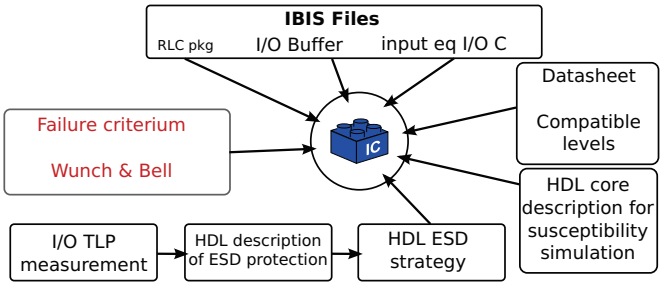

Figure 10. Methodology used to build System Level ESD IC model

Acknowledgment

This work is supported by the french National Research Agency (ANR VTT) E-SAFE Project (ESD Safe automotive system)

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