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Behavioral-Modeling Methodology to Predict Electrostatic-Discharge Susceptibility Failures at System Level : an IBIS Improvement

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Abstract— In this paper, a behavioral modeling methodology to predict ElectroStatic-Discharge (ESD) failures at system level is proposed and validated. The proposed models enable time domain simulation to determine voltage and current waveforms inside and outside an IC during ESD events in order to predict the susceptibility of an electronic system to ESD. Very-high-speed integrated circuit Hardware Description Language – Analog and Mixed Signals (VHDL-AMS) is used as the description language. The purpose of this methodology is based on the improvement of Input Output Buffer Information Specification (IBIS) models widely used in signal integrity (SI) simulation. In this paper the additional information required to be added to IBIS files is described, and comparison between simulations and measurements are exposed.

Keywords—component; Electrostatic discharge (ESD), Input Output Buffer Information Specification (IBIS), behavioral modeling, ElectroMagnetic Compatibility (EMC), Time-domain simulation, VHDL-AMS

I. INTRODUCTION

When designing a system, Signal Integrity (SI) simulations are performed to analyze the circuit behavior and to verify if the final product is not subject to typical problems such as overshoot, undershoot, impedance mismatch, crosstalk or other issues related to ElectroMagnetic Compatibility (EMC). Before the middle of the 90's, the availability of models for circuit's description was very limited and manufacturers were reluctant to give chip internal details required by OEM designers to carry out proper SI simulation. Over the last fifteen years, the IBIS standard, also known as ANSI/EIA-656 [1], has been developed to bring system designers enough integrated-circuit behavioral information to investigate systems SI without releasing any intellectual property from founders.

System-level-ESD investigation is confronted to the same problem as for SI simulations. No circuit's models are available from manufacturers and system designers cannot perform simulations of a whole system without a huge amount of investigations. Failure issues revealed by the IEC61000-4-2 test standard [2] are becoming more and more a concern since the IC's technologies have reached deep submicron dimensions.

It is very important to distinguish and consider two aspects with regard to reliability: the robustness which is the destruction of the product, and the susceptibility related to software failures like reset, clock cycle losses, data error, and others. Up to now, designers of electronic-system focused on the robustness of a product. However, nowadays, more and more applications involve the user's safety. As a result, the products have to fulfill different classes of functionalities defined by the standards [2]. In the automotive application, products must handle an ESD event without any disturbances like reset or even clock loss [3]. From the system designer's point of view, no information about IC internal structures is available to predict failures during ESD events. The manufacturer provides only the datasheets (functionality and electrical characteristics) and IBIS models, but up to now no information that could allow running ESD simulations. IBIS files already provide a lot of information about I/O pins of an IC buffer. One of the main advantages is that it does not reveal any information about architecture or process, which can compromise the intellectual property of semiconductor manufacturers. An improvement of these models with relevant parameters for network ESD protection elements into the IC would allow achieving system level IC models. To this purpose, a behavioral modeling methodology, in the same spirit of IBIS concept, i.e. preservation of proprietary information, is proposed in this paper.

After this brief introduction about the ESD system level context, section II describes the modeling methodology developed from IBIS model to perform susceptibility simulations. Afterwards, section III reports simple cases analysis where the propagation and susceptibility are investigated. The comparison between simulation and measurement results is performed and failure sources are highlighted. Finally, the conclusion is given in section IV.

II. MODELING METHODOLOGY

This methodology, based on a previously published work [4], is intended to model a system composed of digital ICs mounted on a Print Circuit Board (PCB). The main principle consists in modeling each system part separately and assembling all parts hierarchically by following the system topology. The PCB and environment modeling is carried out following the methodology described in [4], but a new

approach for the ICs is developed. A behavioral modeling is applied to model the IC ESD protections and the IC core is modeled to take into account the circuit operation. The two next sections describe respectively the IC ESD protections and core modeling.

A. ESD Protection Modeling

In the following paragraph, all the protections will be described in VHDL-AMS in order to have full behavioral description. The main advantage is that physical knowledge of their operating principle is not primordial. The modeling approach is based on the possibility to simulate mixed signals [5]. VHDL-AMS has two independent computation cores. In the analog core, the model is split into several modes such as: no conduction, reverse or forward conduction, snapback or others. Each mode is associated to an equation. In the digital core, a state machine change conditions is defined to select the analog equation according to the behavioral ESD structure. The digital core allows defining complex change conditions that cannot be implemented in the analog core like strong discontinuities or thresholds on rising events. The full methodology to build the protection's models and the relationships between the two VHDL-AMS cores will be illustrated on the description of an ESD protection based on a Silicon Controlled Rectifier (SCR) in the following.

1) Extracting Parameters from measurement

To extract information from the circuit, static and quasi-static Transmission Line Pulsing (TLP) measurements [6] are performed. TLP measurement example of the SCR-based ESD protection structure is given in figure 1. The inflexion's points of the measured waveform are extracted as parameters to build the model. Six couples of voltage and current parameters (V_x, I_x) are needed to implement the full SCR model as reported in figure 1 and table 1. Four states, highlighted in color on the measurement, are identified: no conduction (0), reverse conduction before snapback (1), snapback (2), forward conduction (3). For each SCR state, a generic linear equation is used. The current I and voltage V are, respectively, the current flowing through and the voltage across the structure. The curve slope and the y-intercept are computed from parameters of table 1. For the SCR, four simultaneous equations, each defined by a state, must be solved. A simultaneous "If" statement structure is used to switch from one equation to the other.

Change-equation conditions could be defined by two-ways. For simple structures, such as a diode, condition could be directly defined in the analog solver on voltage or current level. In this case, only the analog core is used. This kind of condition does not permit to model a structure such as a SCR. The main difficulty with SCR is the modeling of the discontinuity when it goes into snapback states. To define more complex change states conditions, the digital core is used as explained in the next section.

TABLE I. SCR PARAMETER EXTRACT FROM QUASI-STATIC CURVE

Parameters	1	2	3	4	5	6
Voltage (V)	-1.5	-0.1	11.8	12.9	1.9	2.2
Current (A)	-0.4	0	0	0.05	0.1	0.4

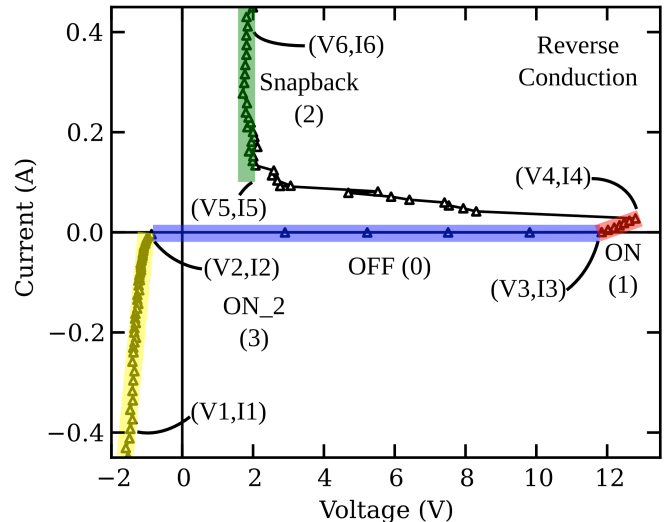


Figure 1: Quasi-static (TLP) measurement of a SCR protection structure.

2) Using the Digital Core for State machine

This section describes how to define the change state conditions for the model using the digital core. To start with, a state diagram is developed to define the release statement conditions of the SCR (figure 2), in which all the changes are reported. Moving from State 0 to State 3 implies that the voltage across the SCR must be higher than V_3 defined by the parameter number 3 in Table 1. Reciprocally, to move from state 1 to state 0, the voltage across the SCR must be lower than V_3 . An access to a state can only be defined in one way. When the voltage V is above V_4 , the state switches to state 2. However, no return condition is defined between state 2 and 1. The SCR can leave state 2 only to switch to the state 0.

A digital signal used as flag allows indicating to the analog solver the state of the SCR as indicated in figure 3. It is updated each time the process ends. This flag is used as condition in the "If" statement of the analog core. The VHDL-AMS source corresponding to the SCR is reported in figure 4.

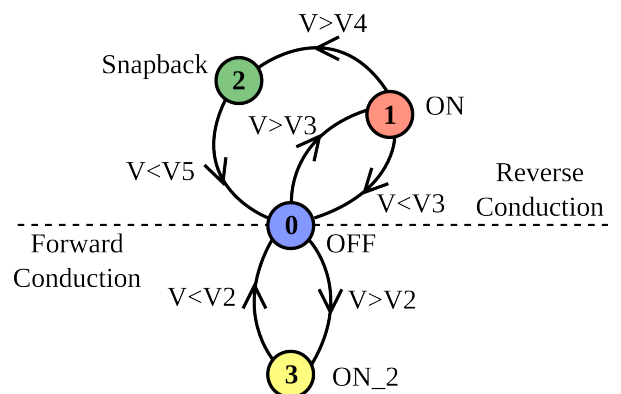


Figure 2: SCR state machine

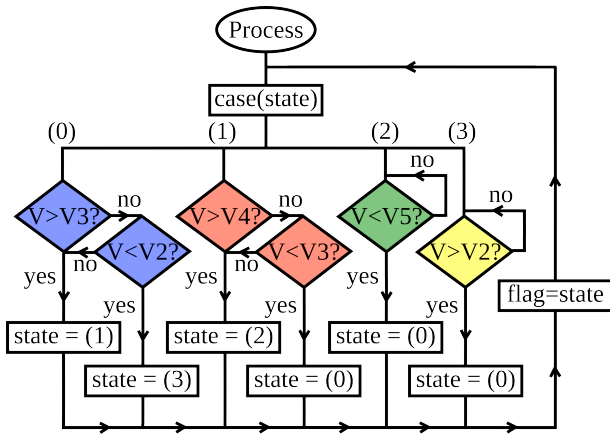


Figure 3: Process organization chart.

3) Interest and Validation

The main advantage of this method is that it is possible to model complex ESD functionalities such as the discontinuity induced by the snapback of a protection device. Moreover, VHDL-AMS allows complex interactions such as, for example, the derivative for the modeling of active ESD structure. Using reduced information, such as six I/V points for SCR structures, it is easy to build behavioral models for ESD system level simulation. Before using full behavioral models, semi-physical models have been investigated in [4]. The same results are obtained with a decrease in time computation with the behavioral models.

```
architecture behav of scr is
    quantity Vscr across Iscr through P to N;
    signal Flag: integer range 3 downto 0 := 0;
begin
    process --digital part
        variable state: integer range 3 downto 0 := 0;
    begin
        flag <= state;
        case state is
            when 0 => wait until Vscr'Above(v3) or (not Vscr'Above(-v2));
                if (not Vscr'Above(-v2)) then state:= 3;
                else state:=1;
                end if;
            when 1 => wait until ((not Vscr'Above(v3)) or Vscr'Above(v4));
                if (Vscr'Above(v4)) then state:= 2;
                else state:=0;
                end if;
            when 2 => wait until not Vscr'Above(v5);
                state:=0;
            when 3 => wait until Vscr'Above(-v2);
                state:=0;
            when others => null;
        end case;
    end process;
    --analog part
    if (Flag = 2) use Iscr == ((i6-i5)/(v6-v5)) * Vscr + (i6-v6*((i6-i5)/(v6-v5)));
    elsif (Flag = 1) use Iscr == ((i4-i3)/(v4-v3)) * Vscr + (i4-v4*((i4-i3)/(v4-v3)));
    elsif (Flag = 3) use Iscr == ((i2-i1)/(v2-v1)) * Vscr + (i2-v2*((i2-i1)/(v2-v1)));
    else Iscr = 0.0; --etat OFF
    end use;
    break on flag; --link between analog and digital
end architecture behav;
```

Figure 4: VHDL-AMS SCR description.

B. Circuit modeling from IBIS and Behavioral ESD Protection Model

The circuit modeling is based on the IBIS model, which is provided by the manufacturer to the designer and contains information for each pin of the integrated circuit. This file, generated in ASCII text format, contains $I(V)$ tables of IC buffers and ESD clamps, $V(t)$ tables for the dynamic output buffers, passive-elements of the package pins, input/output (I/O) equivalent capacitances (C_{comp}) and others. Note that in IBIS standard, the structure called “power clamp” represents the structure between one I/O and V_{DD} , and not the protection

between V_{DD} and V_{SS} as commonly used in the ESD community. Although IBIS files are very useful for signal integrity simulations, information about ESD protection is still incomplete for ESD system level simulation. All the ESD current paths are not considered – for example, IBIS files do not include the power supply protection between V_{DD} and V_{SS} pins. The $I(V)$ characteristic of ESD clamps are only given from $-1 \times V_{DD}$ to $2 \times V_{DD}$ which is not sufficient for the full ESD response. Moreover this range is not high enough to represent the snapback of the protections that can lead to sudden variations of the internal and external voltages and current paths.

To model the circuit, information about pin packages, I/O equivalent capacitances and I/O buffers from IBIS files are reused. However, the behavioral models developed in the previous section replace the models of the ESD protections. Figure 5 shows the simplified schematic of the integrated circuit. “IBIS Packages blocks” include R, L and C passive elements to model the packages. The “2-state IBIS output buffer” blocks reported in figure 5 include the $v(t)$ and $i(v)$ curve of the pull-up and the pull-down allowing to reproduce the output transition. The “IBIS Input Buffer” defines the High-level and Low-level input voltage (V_{IH} and V_{IL}), extracted from the datasheet, proportional to $V_{DD}-V_{SS}$. The function of the circuit core, represented in blue on figure 5, is described in VHDL.

The new circuit model added to the modeling methodology [4] allows analyzing the system behavior during an ESD disturbance and predicting its susceptibility regarding system level ESD.

C. Full System model

The IC model is combined with PCB lines, passive components (including external decoupling capacitance, DC block...) and all the test-bench elements (including generator, oscilloscope and cables) hierarchically by following the topology of the system [4].

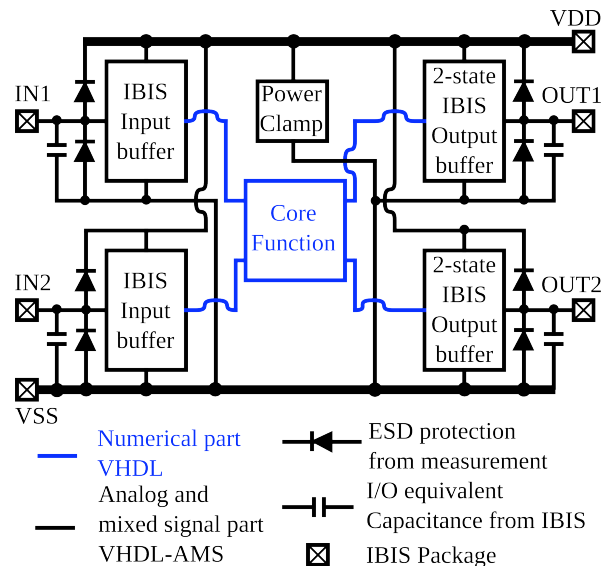


Figure 5: Simplified integrated circuit model with ESD protection and input and output buffers from IBIS model.

III. VALIDATION ON SIMPLE ANALYSIS CASES

A. Importance of modified IBIS implementation.

In order to validate the model, comparison between semi-physical model from [4] and modified IBIS model is carried out. The impact of I/O IBIS buffer is analyzed.

1) Description of Experiment and Test Bench

The studied system is build around a simple inverter in 0.25 μ m CMOS technology. An external decoupling capacitor is placed as closed as possible to the IC, between the VDD pin and the ground plane (figure 6). Another capacitance is placed close to the input as an Electromagnetic Interference (EMI) filter or external ESD protection. Transmission Line Pulsing (TLP) tester is used to inject a 100ns rectangular pulse with 1 ns rise and fall times. It has an excellent reproducibility and does not generate electromagnetic disturbances, which is not the case of classical system level gun tester according to IEC61000-4-2 standard [7-8]. To measure the current flowing into the circuit, a “one-ohm measurement” method inspired from the EMC standard IEC61967 [9] is used. Two cases are investigated: injection into the input and injection into the output.

2) Simulation and Mesurement Results

IBIS file does not provide enough information to carry out ESD simulation. Only a I(V) characteristic from $-1 \times V_{DD}$ to $2 \times V_{DD}$ without snapback was given. The circuit In-Vss ESD protection is actually an SCR that is included into our new model.

Figure 7 shows the simulation results superimposed to measurement results for a TLP pulse injected from input to ground. Without the IN-GND capacitor, the TLP current flows as expected through the ESD structure. However, when a capacitor is added, the external capacitor (C) diverts all the current until its voltage reaches the triggering voltage of the SCR. Right after the SCR snapback, the ESD structure conducts the ESD and the capacitor discharge currents leading to a strong current peak. This is a clear illustration that the ESD protection snapback behavior that is missing in standard IBIS model is required for proper ESD analysis.

Modified IBIS model gives very similar results when compared to semi-physical model (figure 7) with the advantage of a decreased computation time.

In Figure 8, the TLP pulse is injected between output and ground. During the TLP event, the ESD current flows into the ESD protection network and the external decoupling capacitor (Vdd-ground). The resulting current waveform is fully detailed in [4]. Part of this complex shape is related to the ESD clamp between VDD and ground which is not included in IBIS file.

Another interesting point can be noticed in figure 8. The 100 mA current flowing into the circuit corresponds to the conduction of the NMOS output-buffer transistor. This conduction is due to the gate-coupling capacitor (C_{gd}) charging up rapidly during the TLP rising edge. In the semi-physical modeling, a Spice level 1 MOS structure fitted from the data given in IBIS is used. A small difference of around 50mA is observed between the two models but can be neglected as ESD stress level increases.

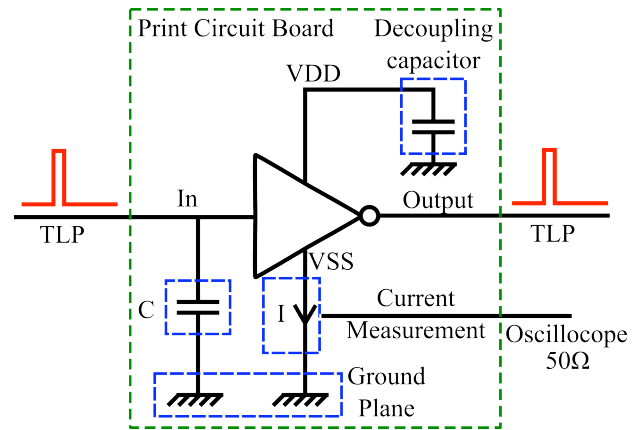


Figure 6: Simplified schematic of the system implemented for study the propagation

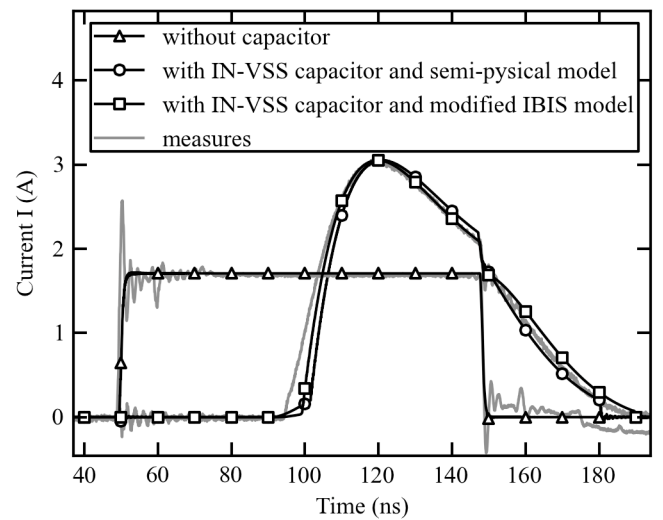


Figure 7: Measurements and simulations of the current I for TLP pulse injected from input and ground.

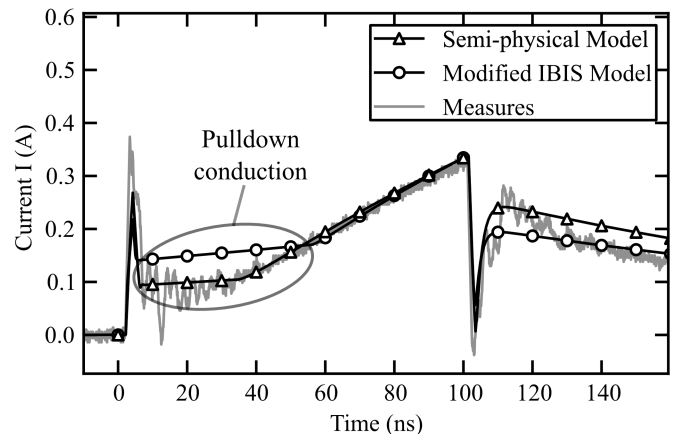


Figure 8: Measurements and simulations of the current I for TLP pulse injected from output and ground.

B. Study of the susceptibility

1) Description of Experiment and Test Bench

Figure 9 shows the simplified schematic of the studied system built around a CMOS 0.25 μ m D flip-flop configured in frequency divider. An external decoupling capacitor is placed as close as possible to the IC, between VDD pin and the ground plane. A voltage regulator powers the D flip-flop through a decoupling network including a diode and a 5.6 μ H inductor. This network ensures that all the ESD current discharge stresses the device under test and not the regulator. The regulator current is limited to 150 mA to prevent eventual latch-up problems. If a latch-up occurs, short-circuiting the power pin, a voltage drop on the regulator output will be visible.

To evaluate the susceptibility of the circuit, an ESD disturbance is injected into the V_{DD} pin using the DPI (Direct Power Injection) technique [10]. The TLP is connected through a DC block composed of a 6.8nF capacitor. A function generator is connected to the CLK pin to synchronize the D flip-flop. The susceptibility level of the output Q is monitored with an oscilloscope with 1M Ω termination. The oscilloscope is triggered on the rising edge of the TLP pulse obtained by a “peak of tee” voltage probe.

A dedicated PCB is designed for the study including all the elements previously described. The PCB is made on a 1.6mm thick FR4 substrate. SMA connectors have been used to connect the board to the TLP tester, function generator and other instruments. All the electronic components on the board (capacitors, inductors, resistances, and diodes) are Surface Mounted Devices (SMD).

2) Simulations and Measurements Results

As described in papers [11,12], whatever the ESD pulse intensity, the output is disturbed. Therefore, it is necessary to choose a failure criterion. In our case, the loss of almost one clock edge has been arbitrary chosen. The measurement and simulation of the whole system are performed with a 50nF external decoupling capacitor between VDD and ground and a 75V TLP injection. The clock input frequency is 2MHz. Figure 10 shows the comparison of measurements and simulations in two cases: no failure (a) and clock losses (b).

In configuration (a), the ESD disturbance occurs far from the clock synchronization signal (rising edge on clock). The output signal keeps still operating normally. In this case, two simulations (Simulation 1 and 2) are carried out to investigate the impact of the level of the input voltage threshold (VIH). In simulation 1 $V_{IH} = 0.7 \cdot V_{DD}$ as given by the datasheet. In simulation 2, $V_{IH} = 0.65 \cdot V_{DD}$. As reported in figure 11, a small variation of this parameter highlights a mismatch in the time response when the output signal returns to zero. When the TLP stress occurs, the internal voltage of the power supply bus increases as the external decoupling capacitor charges up. So, the CLK input voltage VIH does. When the synchronization occurs, VIH is higher than the clock input signal as shown by the simulation in figure 11. The external decoupling capacitor discharges through the pull-up. When VIH reaches the level of the input, the output switches to low-state. To correct this mismatch, an adjustment of VIH level has been performed.

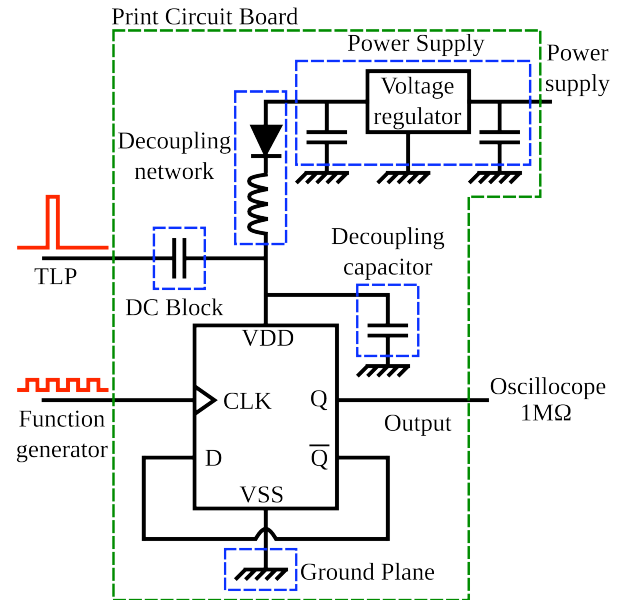


Figure 9: Simplified schematic of the system implemented for DPI testing.

In configuration (b), the synchronization signal is generated when the ESD perturbation on VDD is at its high level. This rising edge is not taken into account by the D flip-flop. The output voltage is holding up to the high level. One period of the input signal is lost. CLK VIH level is larger than the clock input level. The CLK input rising edge is not taken in account and the output does not switch to low-state. An error occurs according to the chosen failure criterion.

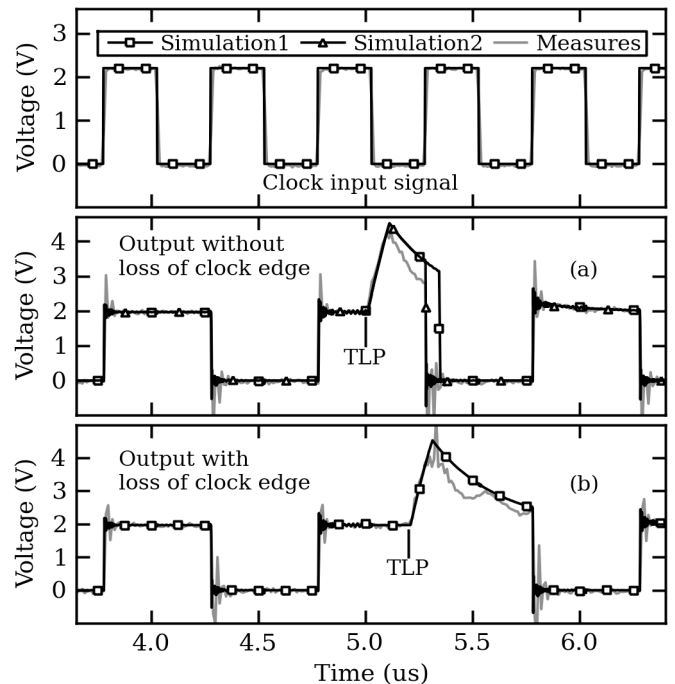


Figure 10: Transient measurements and simulations of the output voltage for configuration (a) and (b) perform with a 50nF external decoupling capacitor, for 75V TLP injection and 2MHz clock input frequency.

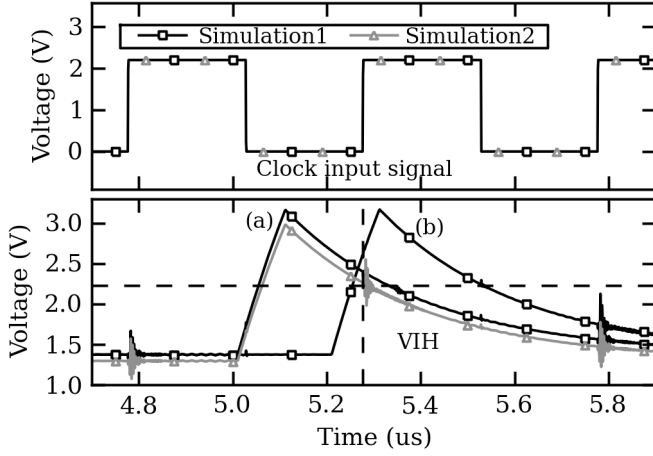


Figure 11: Transient simulations of the clock input signal and zoomed view on the CLK High-level VIH for configuration (a) and (b) performed with a 50nF external decoupling capacitor, for 75V TLP injection and 2MHz clock input frequency.

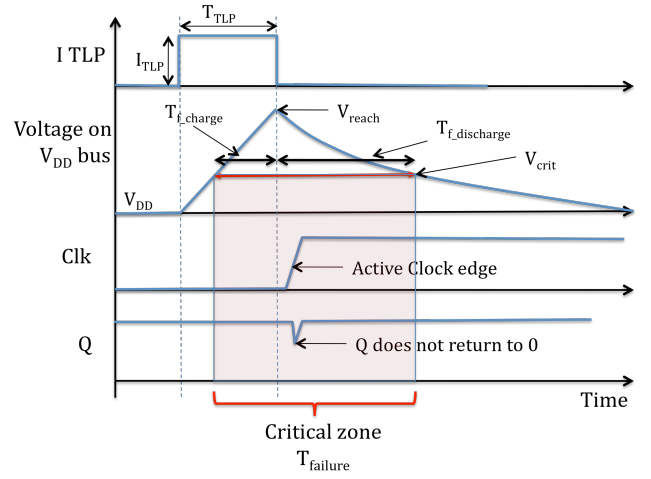


Figure 12: Chronograms showing the signal evolution when an ESD event occurs.

According to this set of equations, an error could happen as soon as V_{crit} is higher than 2.2V in our configuration ($T_{TLP} = 100$ ns and $C_{dec} = 50$ nF), so $V_{DD} > 3.15$ V. The minimum TLP pulse that could generate this perturbation is extracted from (1):

$$I_{TLP} > \frac{3.15 * C_{dec}}{t_{TLP}} \text{ i.e. } V_{TLP} > 52V$$

The failure probability will of course increase with the pulse amplitude. However, the charging of the capacitor will be limited when its voltage (V_{reach}) will reach the triggering voltage of the ESD protection structure. Then, the voltage across the external capacitor remains constant because the (Vdd-GND) ESD structure does not have snapback. Some more investigations on the probability of failure still need to be performed in this particular case.

IV. CONCLUSION

In this paper an improvement of IBIS models with behavioral ESD protection descriptions is proposed and validated on simple cases. The behavioral models implemented into VHDL-AMS are based on a limited number of parameters that can easily be extracted from measurements. Simulations show good correlation with measurement, and short computation time. Our modeling approach is good enough to predict the electrical behavior during an ESD event, in particular the analysis of the circuit interaction with the system during operation. We demonstrated that all the current paths could be obtained using the proposed modeling approach. The IBIS concepts are preserved, i.e. no proprietary information related to architectural structure of the IC is revealed. So, the designer can easily reproduce this methodology for any other circuit. An improvement of IBIS models should be considered to perform a dedicated "cookbook" for ESD protection models by implementing additional parameters. Adding such parameters in the IBIS files could be of great interest for OEM system designers.

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Let us assume that, as reported in figure 12, a failure is generated if the power supply reaches V_{crit} and if a clock event occurs during the critical time zone ($T_{failure}$), which is the sum of T_{f_charge} and $T_{f_discharge}$. V_{crit} corresponds to the VDD increase level that holds up VIH higher than the input clock level.

3) Estimation of T_{f_charge} :

Considering that the increase of V_{DD} during the TLP pulse is forced by the external capacitor C_{dec} , we can use the basic equation:

$$I = C \frac{dV}{dt} \quad (1)$$

V_{crit} is reached at the time:

$$t_{crit} = \frac{(V_{crit} - V_{DD}) \cdot C_{dec}}{I_{TLP}} \quad (2)$$

If V_{reach} is over V_{crit} . Then T_{f_charge} is defined by

$$T_{f_charge} = T_{TLP} - t_{crit} \quad (3)$$

4) Estimation of $T_{f_discharge}$:

The discharge is more complex because the only discharge path goes through the IC via its pull-up transistor. The equivalent resistance, R_{pull_up} , given by the IBIS files is around 10 Ohms and so, the evolution of the discharge voltage is:

$$V_{disch}(t) = V_{DD} + (V_{reach} - V_{DD})e^{-t/\tau} \quad (4)$$

where τ is the $R_{pull_up} * C_{dec}$ product. It results that the $T_{f_discharge}$ is :

$$T_{f_discharge} = -\tau \cdot \ln\left(\frac{V_{crit} - V_{DD}}{V_{reach} - V_{DD}}\right) \quad (5)$$

$$T_{f_discharge} = -\tau \cdot \ln\left(\frac{(V_{crit} - V_{DD}) \cdot C_{dec}}{I_{TLP} T_{TLP} - V_{DD} \cdot C_{dec}}\right) \quad (6)$$

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