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High-temperature operation MOS-IGBT power clamp for improved ESD protection in smart power SOI technology

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Abstract: We propose a new MOS-IGBT power clamp for high-temperature operation providing a very compact high-robustness ESD protection with low temperature sensitivity. It is achieved by inserting in the same LDMOS device P+ diffusions in the drain with various N+/P+ ratios whose impact on R_{ON} and holding current at high temperatures is thoroughly studied.

I. Introduction

Within the context of a sustainable development and to face the challenges of fossil energy shortage, transports are becoming more electrically driven and require new generations of power devices and electronic circuits. In particular, with the advent of wide bandgap semiconductors such as GaN and SiC, the driving circuitry that is still realized with silicon technologies, has to be placed as close as possible to the power devices and should be able to operate at high temperature (≥ 200°C). In addition to this high temperature constraint, ESD requirements from the integrated circuit to the system are particularly severe: for example, in automotive applications, 2-8kV in contact according to the IEC 61000-4-2 standard is often required. It has to be reminded that this ESD standard requires tests both for unpowered and powered systems. For the latter testing, the effect of temperature has to be taken into account in the ESD design window.

The challenge of high temperature operation requires Silicon On Insulator (SOI) technology since it will provide a perfect electric insulation between each active device. Regarding ESD robustness, the proposed protection should provide a high failure current but also work at high temperature, its performance being as insensitive as possible to this parameter.

In this paper, we propose a study of an ESD protection solution based on mixing MOS and IGBT structures in the same device that allows SCR triggering to reach high ESD robustness and a low sensitivity to temperature.

II. SOI smart power technology and proposed ESD protection

The chosen technology is a SOI smart power technology TFSMART 1 provided by Telefunken Semiconductors. TFSMART 1 is a 0.8µm Bipolar CMOS DMOS merged technology on SOI. In this technology, the buried oxide and active silicon thicknesses are 500 nm and 2µm, respectively. Between each device, the width of the trench isolation is equal to 0.8 µm, then providing a perfect electric insulation between active devices under both DC and AC conditions. The process contains 0.8µm CMOS part for 5V supply voltage, lateral npn-transistors and lateral pnp-transistors, P-type and N-type lateral DMOS devices with complete deep trench isolation between wells and vertical oxide isolation to handle wafer/substrate for different supply voltages. These power devices are optimized for various voltage ranges (25V, 45V, 65V and 80V) and minimized on-resistance. Figure 1 presents a schematic cross-section of the technology for the P-type and N-type lateral power MOS devices, P-LDMOS and N-LDMOS.

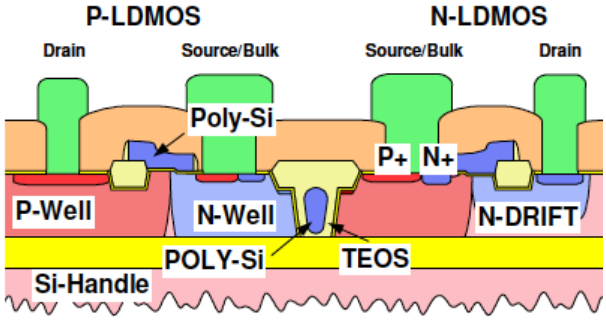

Figure 1: Cross-section of P-LDMOS and N-LDMOS of TFSMART 1 technology.

Regarding the N-LDMOS devices, TFSMART 1 library contains two types of structures. The first one is named SBC (source body short), since the source N-diffusion is shorted to the P-type body diffusion. This short is implemented by inserting within the source N-diffusion a P^+-body contact. The second one, called SBO (source body open), has a shallow trench isolation (STI) between the source and the body contact. This latter structure allows biasing the body at a different voltage from the source.

In this technology, the N-LDMOS 25V with increased gate-drain ballasting distance is used to provide a high-voltage ESD power clamp. It is composed of 11 identical cells that are formed of two 150µm-fingers with closed gate and a central drain diffusion, the body being connected to the source. The corresponding surface is 302 µm x 183 µm and it provides a 2 KV HBM robustness (Imax = 1.7 A TLP) according to TFSMART1 foundry data [2]. The performance of this MOS-based protection structure, namely its on-resistance, is very sensitive to the temperature [1]. Its on-resistance increases from 3.8Ω at 25°C to 6.3Ω at 125°C. If this temperature behavior is not taken into account, it could induce detrimental effects such as a lower failure current and even could lead to not provide the expected protection due to the failing of compliance with the ESD design window. To compensate this effect, the size of the power clamp protection has to be increased.

To cope with these issues, we contemplated developing a new ESD protection. The basic concept we study in this paper consists in combining MOS and bipolar effects in order to compensate the detrimental effects of the temperature. To improve the ESD robustness, we also take advantage of the turn-on of the parasitic thyristor of the structure that will provide a very low on-resistance.

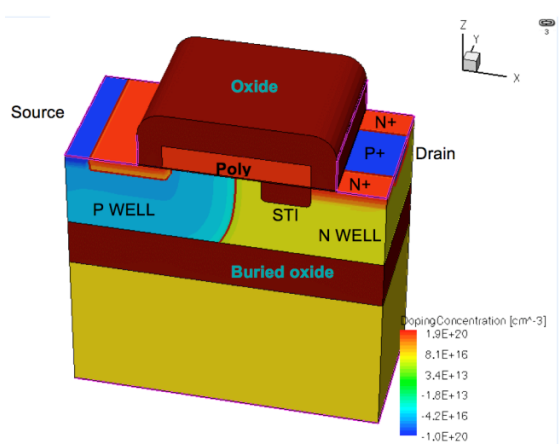

Figure 2: Mixed structure LDMOS-LIGBT with P^+/N^+ ratio equal to 1.

To do so, we combine within the structure of the N-LDMOS a lateral IGBT by implementing in the drain region both N^+ and P^+ diffusions with different ratios. An illustration of such implementation is shown in Figure 2 where the N^+/P^+ ratio is equal to 1. The protection is triggered via its gate to allow protecting low voltage circuitry and an early triggering of the structure (MOS then IGBT) to compensate the intrinsic SCR slow response. Such MOS-thyristor combination was already proposed to improve the performance of power device structures [3]. Using an LIGBT was already proposed to implement an efficient ESD power clamp in an SOI smart power technology [4]. The authors demonstrated the improved performance compared to an NDRIFTMOS device. However, combining the three devices in a single device was not yet studied.

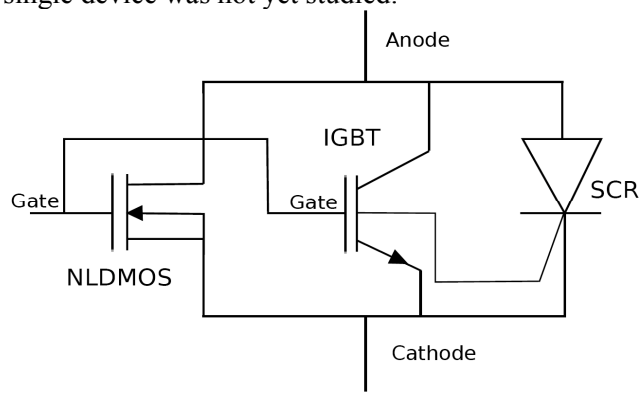

Figure 3: Equivalent electrical schematic of the mixed structure LDMOS-LIGBT.

The main concept is to combine and merge in the same device an LDMOS, which will turn on as soon as its gate is activated, a lateral IGBT that should allow reducing the on-resistance of the full device thanks to minority carrier injection and a thyristor to provide a high-current capability, as shown by the electrical schematic of Figure 3.

To study the impact of the N^+/P^+ ratio on the ESD performance, we designed a test chip with various structures going from a N-LDMOS to a LIGBT and mixed structures called 2P1N, 1P1N and 1P2N with respective N^+/P^+ ratio of 0.5, 1 and 2. The structures are designed in such a way that the gate can be externally biased. They are based one of the elementary cells of the NLDMOS25V-based power clamp (figure 4). In this cell the central N^+ drain is replaced by an alternance of N^+ and P^+ diffusions with different respective ratios.

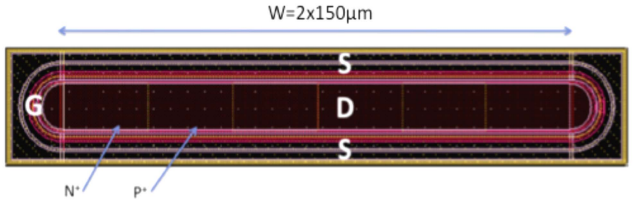

Figure 4: Layout of the mixed structures without metal and contact levels.

III. Static characterization (I-V) of the proposed structures

Figure 5 presents the DC characterization for the mixed structure 1P2N at room temperature with V_{GS} varying from 1V to 4V. It can be noticed that the device prematurely switches into the SCR mode whatever the V_{GS}. The measurement setup being limited at 0.1 A, it is difficult to be sure if the device enters the IGBT mode before the SCR one.

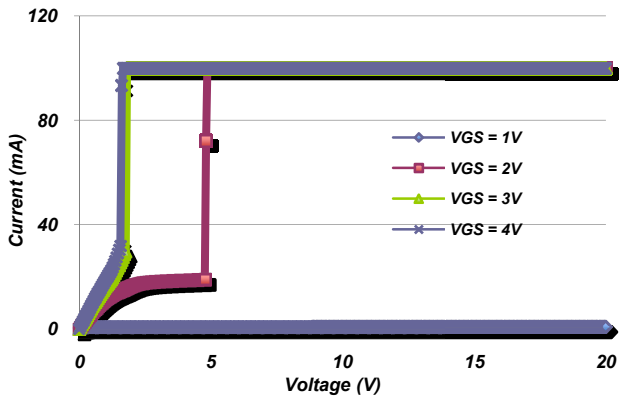

Figure 5: DC characteristics for the mixed structures 1P2N at room temperature for V_{GS} varying from 1 V to 4 V.

To solve this issue, we carried out the same measurement using a curve tracer (Figure 6). This confirmed that the device does not switch into the IGBT mode between NLDMOS and SCR modes.

We observed the same behaviour whatever the N^+/P^+ ratio. In this technology, the designed IGBT is not yet optimised, and as a result, the parasitic thyristor is triggered as soon as the IGBT is activated. In section VI, we propose design solutions to optimise these mixed structures to get an effective IGBT operation before SCR turn-on.

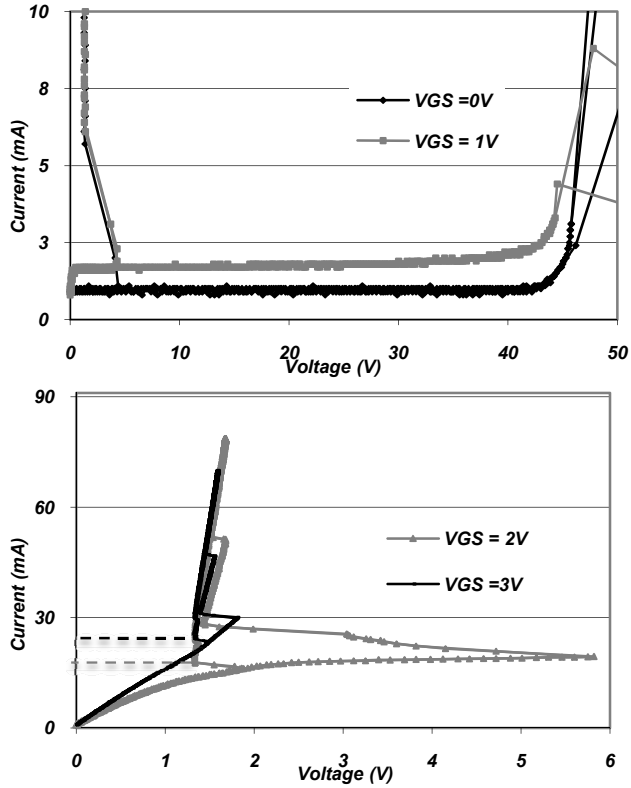

Figure 6: 1P2N structure characteristics using a curve tracer at room temperature for V_{GS} = 0 and 1 V (top), and for V_{GS} = 2 and 3 V (bottom). Dotted lines in bottom figure indicate I_H.

IV. Experimental results at room temperature

To assess the ESD behavior and robustness of the proposed structures, TLP measurements were carried out at wafer level on a Celestron TLP (50 Ω) test bench. A calibration is performed before starting the measurement to eliminate the series resistances due to wire connections. TLP pulses have 100 ns duration and a rise time of 1 ns.

The first set of measurement of the various structures was performed with their gates tied to ground.

Figure 7 summarizes the results for all mixed devices including the NLDMOS and the LIGBT. Regarding the N-LDMOS, it can be noticed that as soon as the voltage reaches the breakdown voltage, although it includes a ballast resistor into the drain, the structure snaps back and fails. This behavior is observed on four different devices (Figure 7).

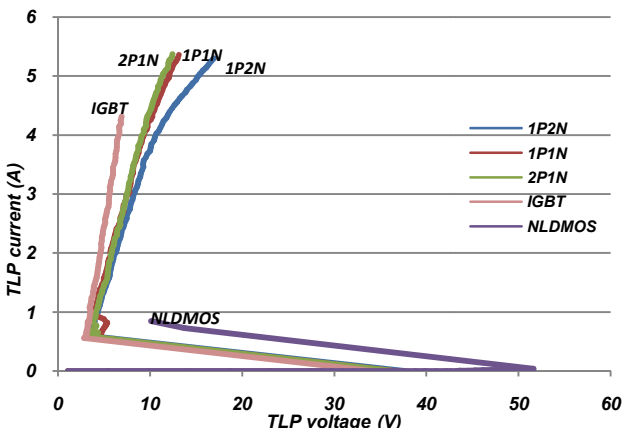

Figure 7: TLP characteristics of mixed structures, NLDMOS and LIGBT with VGS=0V.

For the mixed structures including the LIGBT, it can be first noticed that the triggering voltage is lower than the one of the N-LDMOS: around 37V to be compared to 52V. This reduction is related to the insertion of P^+ diffusions within the drain. Indeed their presence leads to a punch-through effect in the PNP device created with the N-Drift and P-Well regions of the N-LDMOS (Figure 1). Moreover, the four tested structures have a very high ESD robustness (>5.5A) and could not be destroyed due to the limitation of the TLP test bench. All structures exhibit a very strong snapback meaning that the parasitic thyristor is homogeneously triggered [5]. As expected, structures with a smaller N^+/P^+ ratio have a lower on-resistance.

With a silicon surface divided by 11, the proposed structure provides a much higher ESD robustness than the initial power clamp whose maximum current level is 1.7A.

The structures are also characterized as a function of the gate bias V_{GS}. As shown in Figure 8 for a gate bias voltage of 2V, the triggering voltage can be easily lowered and adjusted to a low voltage value compatible with the ESD design window of a low voltage circuitry by tuning the gate voltage. The high current behavior, above one ampere of current, is identical to the one observed with a grounded gate. However, when a gate voltage is applied, the proposed structures start to turn-on first as an LDMOS, then as an IGBT and finally, when a certain voltage and current is reached, the parasitic SCR is activated. However, the current resolution of the TLP test bench does not allow differentiating between the LDMOS and the IGBT mode. It is likely that, given the DC measured behavior, the structures switch to the SCR mode as soon as the IGBT is activated. It has to be noticed that the triggering voltage of the SCR strongly depends on the N^+/P^+ ratio. The lower this ratio, the lower is the SCR triggering voltage.

These measurements are not performed up to failure, so as subsequent temperature measurement could be carried out. However, we can notice that the IGBT, although having a much better on-resistance, exhibits a high resistance behavior above 2.3 A. Actually this IGBT device is not a full IGBT, since it includes a minimum-size N^+ diffusion in the center of the drain to avoid design rules check errors. The presence of this diffusion might induce a temporary current focalization in the associated NPN bipolar device. However the high series resistance of its collector allows a ballasting effect as shown by the onset of a second snapback toward the SCR mode.

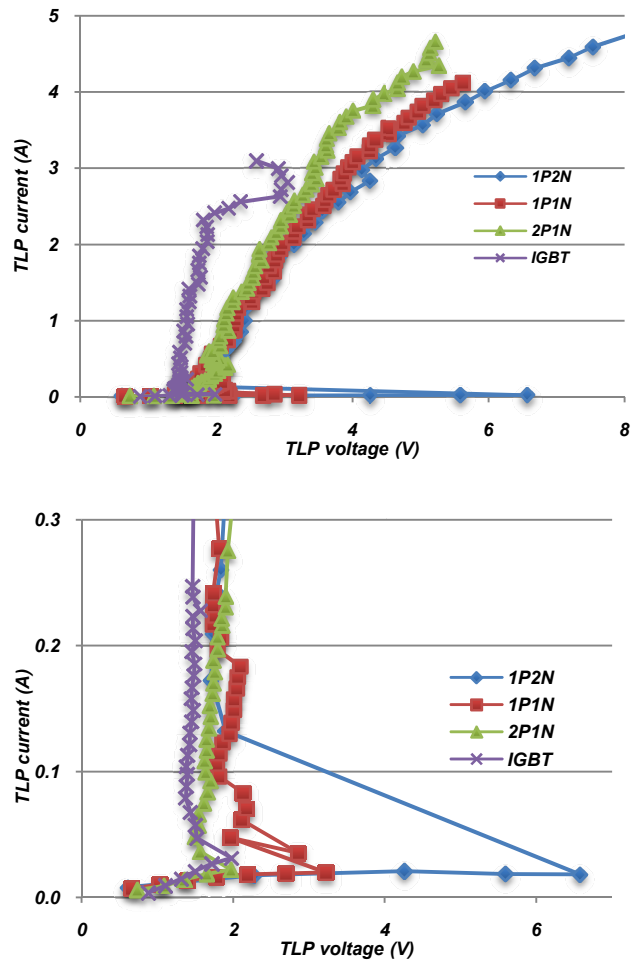

Figure 8: TLP characteristics of mixed structures and LIGBT with V_{GS}=2V (top: full curve; bottom: detail of triggering region).

V. High temperature behavior

There are few publications studying the temperature behavior of ESD protections structures [1] [6]. However, with a strong demand for high temperature applications (automotive, aeronautics, space, etc) and

an increasing need for high ESD robustness of powered systems, it is of great interest to take into account this parameter for the design of the ESD protection structures.

We performed TLP measurement at wafer level at different temperatures 25°C, 50°C, 100°C and 200°C. We report in Figure 9 the measurement of the respective on-resistance (R_{ON}) of LIGBT and mixed structures 2P1N, 1P1N and 1P2N with respective N^+/P^+ ratio of 0.5, 1 and 2 for different temperatures. It can be noticed that the temperature behavior is strongly impacted by the N^+/P^+ ratio. The R_{ON} of the LIGBT structure (N^+/P^+ ratio=0) varies by 75% whereas the R_{ON} of the other structures with a higher N^+/P^+ ratio varies in average by 135% between 25°C and 200°C.

The main interests for ESD protection structures exhibiting a low dependence with temperature are on the one hand, to guarantee that they fit the ESD design window whatever the temperature conditions and on the other hand, to limit the silicon area since no oversizing will not be required to compensate the degradation of their performance with temperature. As can be concluded from the results of Figure 9, the best results will be obtained with structures as close as possible to a full IGBT. The best trade-off to be found will be defined by the capability of the structure to withstand latch-up testing.

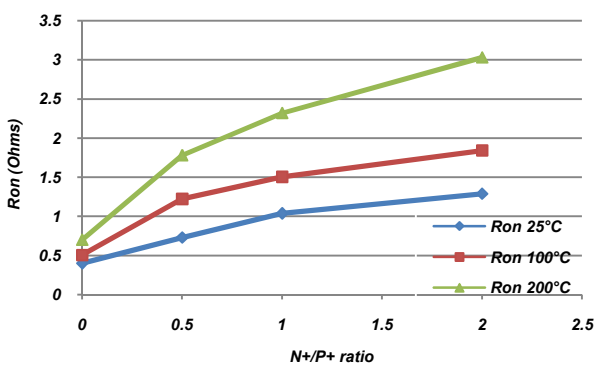

Figure 9: Measured on-resistance of LIGBT and mixed structures 2P1N, 1P1N and 1P2N with respective N+/P+ ratio of 0, 0.5, 1 and 2 at 25°C, 100°C and 200°C.

VI. Structure optimization

As previously noticed, in the high current regime, the parasitic SCR turns on in all structures that is very beneficial for the on-resistance of the structure. For this preliminary study, we did not optimize the holding current of the structures to guarantee latch-up safety. However we have evaluated a test method to support further study. Using 50Ω or 500Ω TLP testing does not allow properly characterizing the real holding current of the SCR. Indeed, decreasing continuously the ESD current until the SCR turns off is the most appropriate way to measure the real SCR holding current. TLP being a pulsed measurement, it cannot offer such a continuous decrease. Multilevel TLP could be one solution but the technique we selected, HBM-IV measurement, appears much easier and straightforward to carry out [10].

Table 1: Measured holding current of the different structures using wafer-level HBM at 25°C, 50°C, 100°C and 150°C at V_{GS}=0V.

	25°C	*50°C*	*100°C*	*150°C*
LIGBT	7.0 mA	6.7 mA	5.3 mA	5.0 mA
2P1N	7.0 mA	6.3 mA	4.7 mA	5.0 mA
1P1N	7.0 mA	6.5 mA	5.7 mA	5.3 mA
1P2N	7.2 mA	6.7 mA	5.0 mA	4.8 mA

We used a wafer-level HBM tester from Hanwa that allows acquiring I-V characteristics with a real HBM waveform. The falling part of the temporal HBM current and voltage waveforms is used in a straightforward way to determine the SCR holding current. Indeed, in the falling part of the HBM waveform, the SCR is triggered and conducts a decreasing current. When the current is insufficient to maintain the SCR operation (holding current) the voltage across the device starts to increase rapidly (Figure 10).

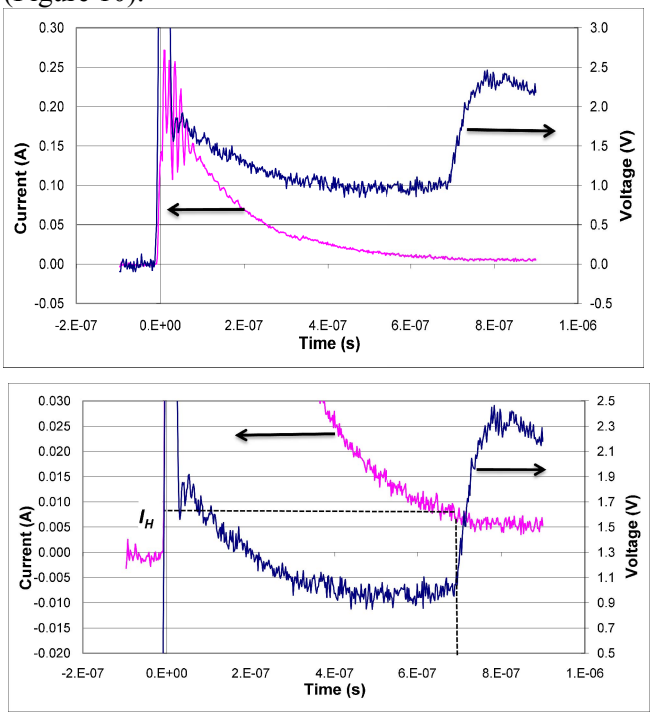

Figure 10: : Current and voltage characteristics under wafer level HBM of the structure 1P1N at V_{GS} = 0V (full curve (top) and zoomed curve (bottom)).

The values of the holding current of the proposed structures are summarized in Table 1 for various temperatures. As it can be noticed, for all the structures, its value is too low to guarantee a latch-up free operation [7]. The targeted I_H values should be higher or equal to 100 mA. It is interesting to note that this value is not very sensitive to temperature. Interestingly, it is not dependent on the N^+/P^+ ratio. This means that the main parameters that defines the holding current are the ones not impacted by this ratio, i.e. the bipolar current gains and the p-well body resistance.

The holding current is defined by the following parameters and equation [8]:

$$I_H = \frac{\beta_p(\beta_n+1)\cdot I_{NW} + \beta_n(\beta_p+1)\cdot I_{PW}}{\beta_n\beta_p - 1} \qquad (1)$$

Where β_n and β_p are the current gains of the parasitic NPN and PNP bipolar transistors and I_{NW} and I_{PW} the currents flowing into the N-well and P-well, respectively.

€

To increase I_H, as we cannot modify the current gain of the two bipolar transistors, the classical way is to reduce as much as possible the resistances of the two wells [9]. In the proposed structure, this means optimizing the N^+/P^+ ratio in the drain on the one hand and introducing P^+ diffusions into the N^+ source diffusion to reduce the P-Well resistance. Regarding the well resistances, the best solution would be to maximize the N^+/P^+ ratio into the drain whereas minimizing it into the source. To find out the best trade-off between high I_H and low on-resistance, we performed 3D simulations. They show that varying the N^+/P^+ ratio in both source and drain regions allows finely controlling and increasing I_H whereas keeping the ESD performance. However I_H measurements have shown that its value is almost independent of the N^+/P^+ ratio into the drain meaning that the SCR triggering is mainly controlled by the parasitic NPN bipolar transistor. Therefore, the most efficient way to increase I_H consists in engineering the source side that controls the parasitic NPN bipolar transistor.

All the structures used in this first test circuit are SBO type since the original LDMOS was implemented that way. A first solution to optimize the I_H value is to use SBC-type structures that allows significantly reducing the P-Well resistance (base of the NPN bipolar transistor). Using Sentaurus TCAD, we simulated a 3D structure to check the impact on the holding current. The structure under study is based on an NLDMOS 25 V. We could not access accurate doping profiles for this structure. To perform the 3D simulation on the NLDMOS 25V, we did some fitting according to TLP measurement, but the simulation results can only be considered as qualitative to compare the relative efficiency of different design solutions.

To perform the 3D simulations, we use a quasi-stationary simulation to minimize computing time since a transient simulation requires about one month. In addition, since the simulations are carried out in the low current regime around the holding current point, there is no need to activate the temperature equations.

To limit the computing time, the simulated structure is an elementary cell of 3µm-width. Therefore, the computed I_H should be scaled according to the real structure. According to equation (1) I_H is inversely proportional to the well resistances via I_{PW} and I_{NW} currents, and a scaling coefficient can be computed. According to the way we compute it, its value can be in the range of 6 to 10.

Figure 12 shows the difference between SBC and SBO 3µm-wide devices at room temperature and V_{GS}= 3 V for a mixed structure 1P1N. I_H increases from 5 mA for a SBO structure to 8 mA for a SBC one.

As the I_H current increase from 5 to 8 mA is not sufficient, another interesting solution consists in reducing the channel by locally replacing a part of the N^+ source diffusion by a P^+ diffusion, or inserting a P^+ diffusion into the source which does not reduce the channel. We named this structure Optimized mixed structure SBC (Figure 11)

The result of the 3D simulation for the structure of Figure 11 shows that I_H increases from 8 mA for a SBC mixed structure to 12 mA for an optimized mixed structure SBC (Figure 12). According to the simulation-scaling coefficient, the resulting I_H should be in the range of 100 mA therefore meeting the latch up specification.

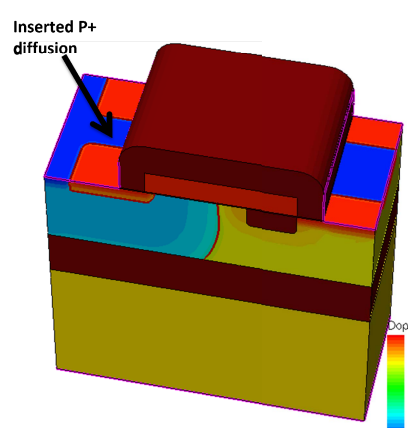

Figure 11: Optimized mixed structure SBC 1P1N.

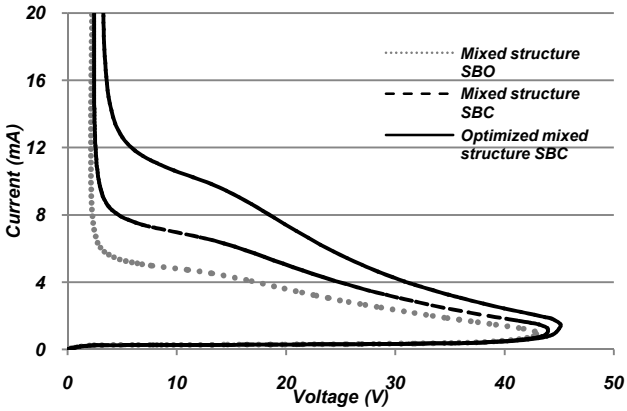

Figure 12: TLP characteristics difference between SBC mixed structure and reduced channel mixed channel at room temperature and at VGS = 3V

When applying a voltage to the gate, it can be noticed that the SBC structure exhibits the three modes of operation: LDMOS, LIGBT and finally SCR (Figure 13). It can be noticed that the triggering of the IGBT occurs at a higher drain voltage for the optimized structure.

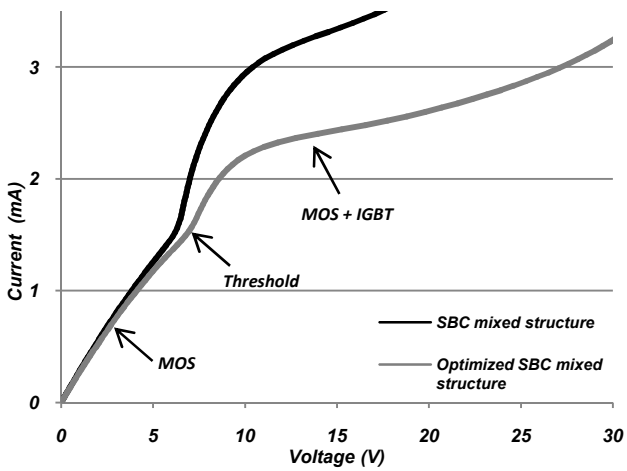

Figure 13: Comparison of DC characteristics: SBC mixed structure and Optimized mixed structure (reduced channel) at room temperature and at VGS = 7V.

By measurement, we also evidenced another original way to control the triggering of the SCR by taking advantage of the gate bias. We measured the impact of the gate voltage on the value of the holding current (see Figure 6). The results, summarized in Table 2, shows that increasing the gate voltage allows significantly rising the value of the holding current. From the grounded gate configuration to a V_{GS} of 3V, an increase factor of 4 to 5 is observed for the holding current.

Table 2: Impact of V_{GS} voltage on the value of holding current for the different structures.

V_{GS} (V)	0	1	2	3
I_H (1P2N) mA	6	6	17.5	24
I_H (1P1N) mA	5.5	6	17	23
I_H (2P1N) mA	4.5	5.2	17	23
I_H (IGBT) mA	5.5	7	18	23

We attribute the gate bias effect on the holding current to the transition from a SCR to an IGBT conduction-mode as schematically represented on Figure 14. This implies that the holding current of the hybrid structure would correspond to the saturation current of the IGBT. This is indeed what is observed. As can be seen from figures 5 and 6, the saturation current at V_{GS} = 4 V is about 20 mA which actually corresponds to the holding current of the structure at the same V_{GS} (Table 2).

To explain this behavior, we think that IGBT operation prevails on SCR one because the MOS transistor in parallel with the IGBT somewhat short-circuits the NPN bipolar transistor that is part of the SCR. Indeed, the MOS transistor injects electrons in the device N-Well drift region thus enhancing recombination of the holes injected by the PNP bipolar transistor and decreasing its collector current and as a result, the base current of the NPN bipolar transistor. This phenomenon might also be helped by the NPN-transistor current gain roll-down at low current density leading to a full shut down of the NPN transistor and by consequence of the SCR operation.

Of course, as measurement demonstrates that the SCR holding current can be controlled by the gate bias, such solution requires proper and intelligent control of the gate potential to really take advantage of this phenomenon. Indeed during normal circuit operation, when latchup could occur, gate control would allow switching from SCR uncontrolled operation to an IGBT operation that can then be switched off by pulling the gate back to ground. For unpowered operation a quite standard triggering circuit offering long enough gate biasing will be sufficient.

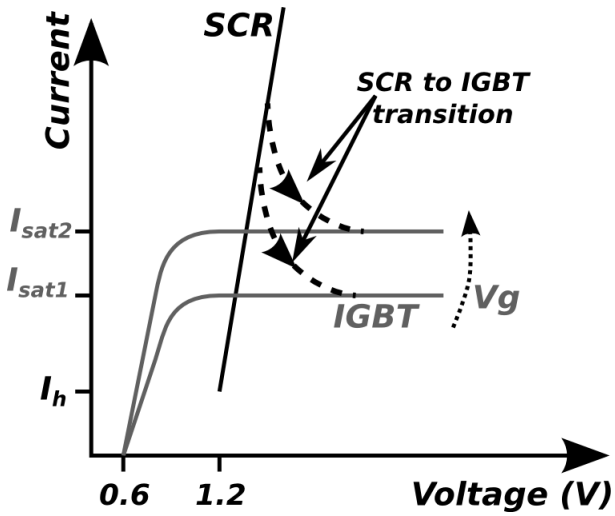

Figure 14 : Illustration of the transition from SCR to IGBT conduction mode at two different V_{GS}

VII. CONCLUSION

We proposed a new MOS-IGBT power clamp for high-temperature operation and improved ESD robustness. The basic concept is to trigger the structure as an IGBT but to also allow its parasitic SCR triggering. To do so, we combined within a same N-LDMOS a lateral IGBT by implementing P^+ diffusions in the N^+ drain region with different N^+/P^+ ratios. The proposed structures provide a high ESD robustness (> 5.5 A) with a ten times smaller silicon area compared to the initial LDMOS-based power clamp. Another beneficial effect of this design is that the performance of the ESD protection becomes much less sensitive to temperature. We proposed original design solutions to improve the immunity to latch-up of these structures by engineering the source side, on the one hand, and providing an additional control via the gate, on the other hand. These solutions were validated through comparative 3D simulations. A silicon test vehicle including various implementations of these solutions was designed but was not available on time for the final version of this paper.

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