



HAL
open science

Low Cost 3D Multilevel Interconnect Integration for RF and Microwave Applications

Ayad Ghannam, Lamine Ourak, David Bourrier, Christophe Viallon, Thierry Parra

► **To cite this version:**

Ayad Ghannam, Lamine Ourak, David Bourrier, Christophe Viallon, Thierry Parra. Low Cost 3D Multilevel Interconnect Integration for RF and Microwave Applications. 62nd Electronic Components and Technology Conference (ECTC 2012), May 2012, San Diego, United States. 5p. hal-00720570

HAL Id: hal-00720570

<https://hal.science/hal-00720570>

Submitted on 24 Jul 2012

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Low Cost 3D Multilevel Interconnect Integration for RF and Microwave Applications

Ayad Ghannam¹, David Bourrier¹, Lamine Ourak^{1,2}, Christophe Viallon^{1,2}, Thierry Parra^{1,2}

¹ CNRS ; LAAS ; 7 avenue Colonel Roche, F-31400 Toulouse, France

² University of Toulouse ; UPS ; LAAS ; F-31400 Toulouse, France

aghannam@laas.fr, bourrier@laas.fr, ourak@laas.fr, cviallon@laas.fr, parra@laas.fr

Abstract

This work presents a new and low cost multi-level 3D copper interconnect process for RF and microwave applications. This process extends 3D interconnect integration technologies from silicon to above-IC polymer. Therefore, 3D passive devices and multi-level interconnects can be integrated using a single electroplating step making the process suitable for 3D-MMIC integration. 3D interconnects are realized by patterning the SU-8 to specific locations to create the desired 3D shape. A 3D seed layer is deposited above the SU-8 and the substrate to insure 3D electroplating current flow. The BPN is used as a thick mold for copper electroplating with an aspect ratio as high as 16:1. An optimized electroplating process is later used to grow copper in a 3D technique, insuring transition between all metallic layers. Finally, high-Q (60 @ 6 GHz) power inductors have been designed and integrated above a 50 W RF power LDMOS device, using this process.

Introduction

Today, RF and microwave applications demands for increased functionality, higher density integration, better passive device performance, reduced footprint and cost are stressing for new and enhanced integration technologies. To meet these requirements, technologies like 3D-MMIC were introduced [1]-[4]. These technologies look promising because they offer a solution for both miniaturization and passive device performance issues. However, their complexity, cost and processing time increase quickly with each addition of a dielectric or a metallic layer, which hindered their large scale usage. Moreover, the performance of the passive devices is severely limited by the relatively thin dielectric layers. Thus, stacking several dielectric layers is required to improve the performance of these devices which often induces more complications like increased residual stress on the chip and the frequent need for mechanical dielectric leveling steps.

In another hand, to overcome 3D-MMIC limitations, a specific 3D interconnect technology is needed to replace current planar technologies used for implementation of passive circuits such as filters, matching networks, transformers ... or for the integration of inductors often realized from bond wires. This implies that the technology must allow the integration of both the interconnect and the vias for underneath connection.

Finally, current 3D interconnect technologies are focused on the 3D stacking of integrated circuits, at the IC-fab, or, at package level, to achieve a higher integration density and a smaller footprint of electronic components [5]. Such a technology would be more attractive if it could be applied as well for above-IC passive devices integration. However, this

feature cannot be insured since current technologies are mainly implemented on silicon substrates and could require additional processing steps like thinning, wafer bonding etc.

For this work, a thru polymer 3D multi-layer copper interconnect process has been developed to overcome all previous drawbacks and aims. This low cost process is compatible with standard lithography and electroplating techniques. It relies on dielectric patterning, 3D seed layer deposit and 3D copper electroplating to form 3D interconnects or passive devices in one single metallization step. As a result, and compared to planar technologies, the number of technological steps, is greatly reduced. Furthermore, residual stress is reduced and dielectric mechanical polishing step is eliminated which minimizes the risk of defect.

All process technological steps and the process implementation, for high-Q 3D interconnected RF power inductors integration above 50 W RF LDMOS transistors, are presented in this paper.

3D multi-level Interconnect Process

The process was designed to meet the requirements of reduced cost and processing time, 3D metal integration capability and enhanced passive devices performance. If one is capable of growing metallic layers three-dimensionally with minimum processing steps, all requirements will be met. Additionally, if the process capabilities can extend to multi-level metal integration with minimal supplementary steps, cost will be further reduced. Consequently, 3D multi-level metal integration using a single electroplating step appears as a main challenge.

To achieve 3D multi-level metal integration, we sought elevating the metal at specific locations; this allows the shaping of the 3D interconnect while ensuring metallic continuity with the underlying layers. Fig. 1 shows that by placing a pillar and after 3D electroplating, a 3D interconnect can be realized. Another variation is done using hollows (Fig. 2a) or a combination of both hollows and pillars (Fig. 2b). Stacking pillars and/or hollows can be used to add another metallic level. If metal crossing is not present, a single electroplating step can then be used to form 3D multi-level interconnects. However, if metal crossing is present, an additional electroplating step is required. Usually, this can be avoided by design. However, if mandatory, a first planar electroplating step at crossing locations might be used prior the integration of pillars/hollows.

Pillars and hollows can be obtained by spin-coating a polymer photoresist (BCB, polyimide, SU-8...) or laminating a dry film. For our work, the SU-8 negative photoresist was used as a dielectric for its advantageous technological properties and its good electrical properties for frequencies up to 7 GHz [6]. Furthermore, using standard lithography

process, this photoresist allows the realization of dielectric thicknesses ranging from few micrometers to several hundreds of micrometers, with vertical sidewalls. The vertical sidewalls make the SU-8 choice delicate since it presents the biggest challenge for 3D seed layer deposit, especially for SU-8 thicknesses higher than 30 μm . Therefore, once this challenge surpassed, any other polymer can be used regardless of the geometry of its sidewalls.

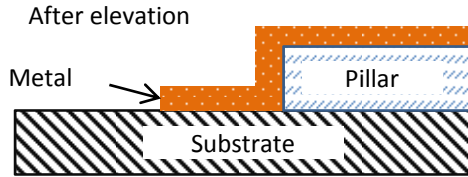


Fig. 1. Process principle: metal elevation to create 3D interconnect.

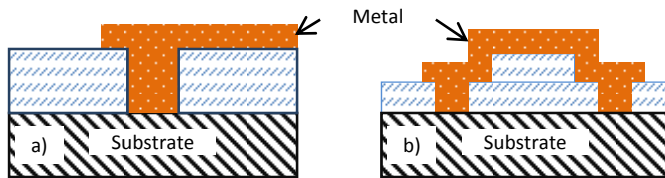


Fig. 2. 3D interconnects: a) using hollows. b) using hollow/pillar combination.

SU-8 lithography process comprises six steps, which are: 1/ spin-coating, 2/ pre-exposure bake, 3/ exposure, 4/ post-exposure bake (PEB), 5/ development and 6/ hard bake. In order to reduce the tensile stress of the SU-8 and cracking, at the end of the PEB cycle, the temperature must be ramped down to 25 $^{\circ}\text{C}$. The process used for a 90 μm thick SU8 layer deposit is the following:

1. Coating of SU8 3050: 8 ml spun at 1500 RPM for 30s.
2. Pre-anneal: 1 min @ 65 $^{\circ}\text{C}$ then 40 min @ 95 $^{\circ}\text{C}$.
3. Exposure: 360 mJ/cm^2 .
4. Post exposure bake: 1 min @ 65 $^{\circ}\text{C}$ then 3 min @ 95 $^{\circ}\text{C}$ then ramp down to 25 $^{\circ}\text{C}$.
5. Development: 15 min using PGMEA.
6. Final anneal: 1 min @ 65 $^{\circ}\text{C}$ then 2 min @ 125 $^{\circ}\text{C}$.

Depositing a seed layer is the next step after dielectric patterning. For this process and like Through Silicon Vias (TSV) technologies [7]-[10], the main challenge for successful 3D electroplating is a void free 3D seed layer. This challenge is affected mainly by the geometry of the sidewalls (vertical, diagonal...), the shape of the dielectric (hollow, pillar) and its thickness, the size of the hollows (if present) and the used equipment (evaporation, sputtering). In fact, if evaporation technique is used, the presence of a high vertical sidewall might create a shadow effect. This results into a locally thinned seed layer or even into voids (left part of Fig. 3). Such thin or inhomogeneous seed layer can fuse while applying the electroplating current. Sputtering technique can enhance the seed layer thickness homogeneity. However, in some severe cases, like the presence of narrow hollows, approaches like seed layer enhancement (SLE) [11] must be used. SLE, typically used in Through Silicon Vias (TSV) applications, is prepared using a chemical solution for deposition of a thin 3D conductive layer on all the surfaces. Although originally dedicated to silicon substrates, in-house

developments have allowed us to expand this technique to polymer substrates.

When the seed layer is homogenous (right part of Fig. 3), the electroplating current will circulate in a 3D way allowing copper growing on all exposed surfaces and sidewalls which are bound into the electroplating mold.

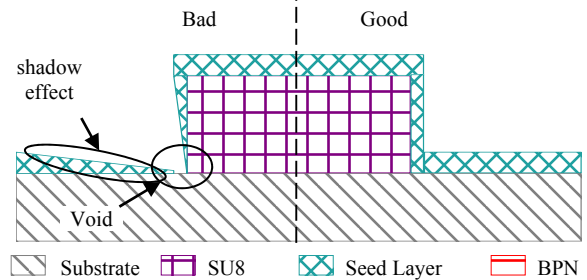


Fig. 3. Illustration of 3D seed layer deposit difficulties.

During process development, we used several metals and equipment to find the best result. We experimented with Titanium, Tantalum, Copper and Gold using two machines: electron canon evaporation and a sputtering cluster. The result of this experimentation shows that a thickness of 1000/2000 \AA of either titanium/copper (Ti/Cu) or titanium/gold (Ti/Au) produces a uniform, void free 3D seed layer. This result is valid for both evaporation and sputtering techniques, with an advantage for the later ones when the dielectric layer contains hollows for vias implementation. It is also possible to apply SLE on 500/1000 \AA thick evaporated Ti/Cu and reach a homogenous seed layer (Fig. 4). For this test, two SU-8 layers with a total thickness of 90 μm have been used.

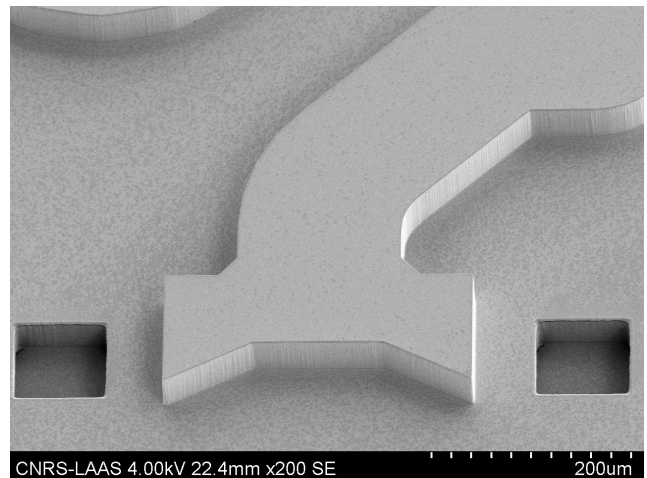


Fig. 4. 3D Ti/Cu seed layer with applied SLE over two SU-8 layers.

After successful deposit of 3D seed layer, the next step of the process consists of creating molds for copper electroplating. Compared to TSV technologies, this step poses a greater challenge due to the presence of the dielectric pillars at the surface of the substrate. Therefore, in our case, the photoresist used for mold formation should present the following abilities:

- high thicknesses: the photoresist must present a thickness larger than the sum of the dielectric and copper thicknesses. For example, if the dielectric is 90 μm thick and the required copper thickness is

10 μm , the thickness of the mold should be greater than 100 μm .

- high resolution: the photoresist must have a high aspect ratio in order to allow integration of narrow interconnects. It must be noticed, as well, that the required resolution leads to a trade-off on the photoresist thickness.

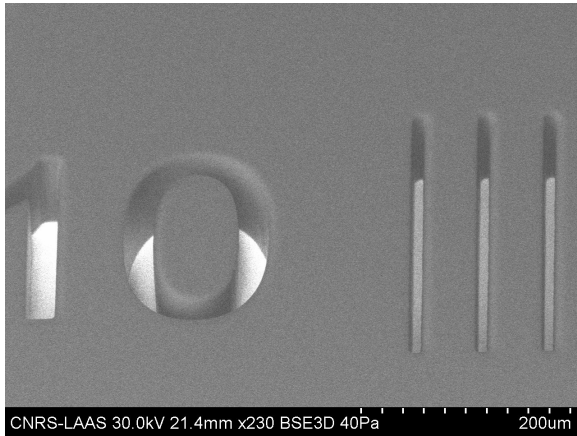


Fig. 5. SEM micrograph showing the high aspect ratio of BPN.

Unfortunately, since the process is intended to be used for a wide range of dielectric thicknesses (10 to > 150 μm), few mold photoresists are capable of fulfilling these requirements. Throughout those choices are the SU-8 and the BPN photoresist. The BPN photoresist offers a better alternative to the SU-8 for mold formation since it can be easily stripped using an *N*-methyl pyrrolidinone (NMP) type-based stripper [12]. The stripper, heated at 50 $^{\circ}\text{C}$, selectively dissolves the BPN without damaging the surrounding materials. However, this photoresist is commercialized with a relatively low aspect ratio (2:1) specification. After a process optimization [13], the resolution of the BPN fortunately reaches an aspect ratio as high as 16:1 (Fig. 5).

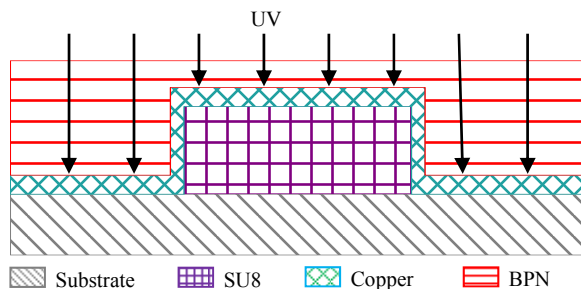


Fig. 6. Illustration of BPN lithography exposure difficulty.

The BPN lithography process is made of four steps: 1/ spin-coating of the resist, 2/ pre-exposure bake, 3/ UV exposure, 4/ development. The main difficulties consist in finding all proper annealing temperature and time, UV dose and development time, since the presence of pillars and hollows creates several different thicknesses for insulation and etching (Fig. 6). To obtain 100 μm thick BPN layer, the following process is used:

1. Spin coat: 8 ml of BPN 65A at 750 RPM for 30 s.
2. Pre-exposure bake: 3 min at 65 $^{\circ}\text{C}$ then 3 min 30 at 120 $^{\circ}\text{C}$.

3. Exposure: 1350 mj/cm^2 .

4. Development: 6 min using TMAH.

Once electroplating molds are formed, an optimized copper electroplating process is used to grow multi-level copper three-dimensionally. Although previous process steps are crucial to obtain the 3D shape, the electroplating process itself is of equal importance, since it must be capable of properly filling the vias and forming interconnects simultaneously. The electroplating requirements are similar to those of TSV technologies. Therefore, extensive work has been done to set properly all electroplating parameters, like electrolytic bath concentration, current density, electroplating temperature...

Fig. 7 shows a cross-sectional view of 3D copper electroplated. One can notice the good filling of the vias and the electrical continuity among all metal levels.

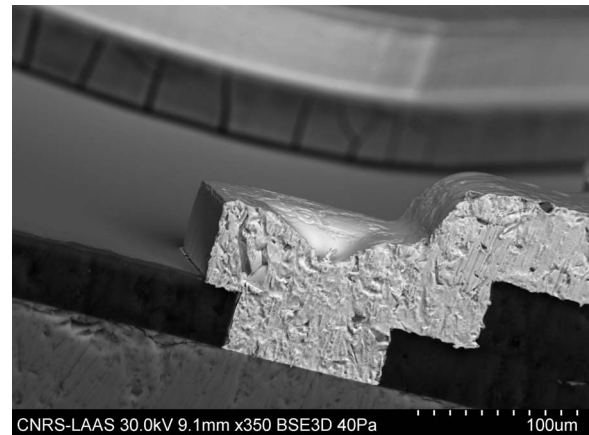


Fig. 7. Cross sectional SEM micrograph of 3D electroplated copper in a pillar/hollow configuration.

To resume previous steps, achieving multilevel 3D electroplating involves four prerequisites which are: 1/ the deposit and the selective patterning under specific locations of a dielectric polymer on top of the substrate; 2/ the deposit of a void free 3D seed layer; 3/ the deposit of a high aspect ratio thick photoresist mold for 3D copper electroplating; 4/ the optimization of copper electroplating process for 3D metal filling.

Experimental Results

After validation of each technological step, 3D interconnects with two SU-8 thicknesses (45 and 90 μm) were fabricated using the proposed process. For both SU-8 thicknesses, the same thickness of BPN (100 μm) was used. In the case of 45 μm thick SU-8 (Fig. 8a), 20 μm thick copper was electroplated. However, for 90 μm thick SU-8 (Fig. 8b) and due to the small thickness difference with 100 μm thick BPN, only 10 μm copper was electroplated. For this implementation, the following technological steps are performed:

1. Deposit and patterning of 45 or 90 μm thick SU-8 layer
2. Evaporation of a 1000/2000 \AA thick Ti/Cu seed layer
3. Deposit of a 100 μm thick BPN layer and mold lithography
4. 10 or 20 μm thick copper electroplating
5. BPN dissolution and seed layer etching

Only two lithography masks were needed.

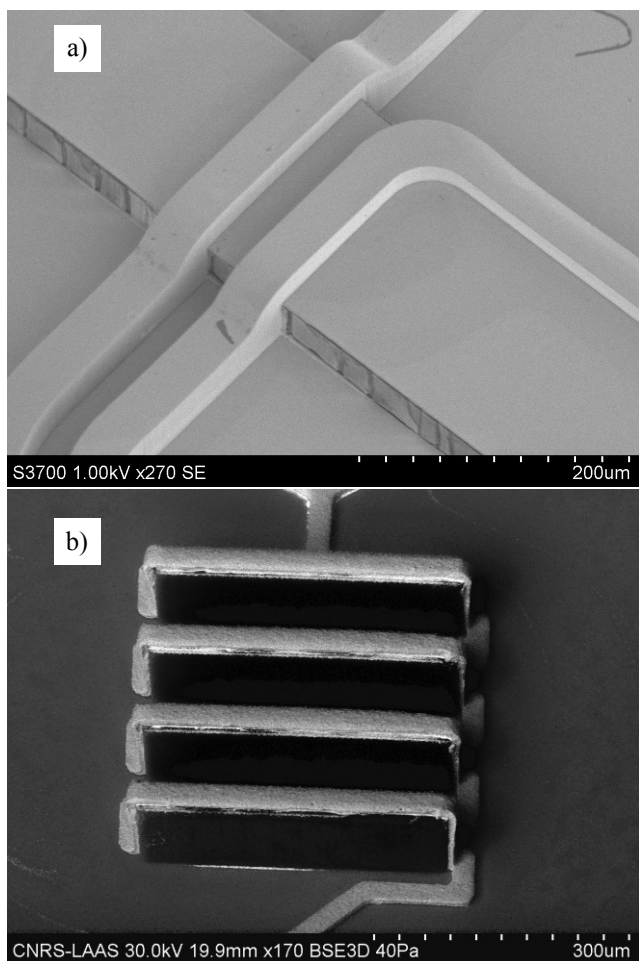


Fig. 8. SEM micrographs of multi-level 3D interconnect fabricated using the process: a) 45 μm thick SU-8. b) 90 μm thick SU-8.

Fig. 8 shows the good metallization continuity between all levels, from substrate to the upper metal level. It illustrates, as well, the process ability to step over a dielectric vertical wall. Fig. 8b show a solenoid inductor integrated using a single electroplating step. Therefore, it can be stated that the realization of these test structures validates the process.

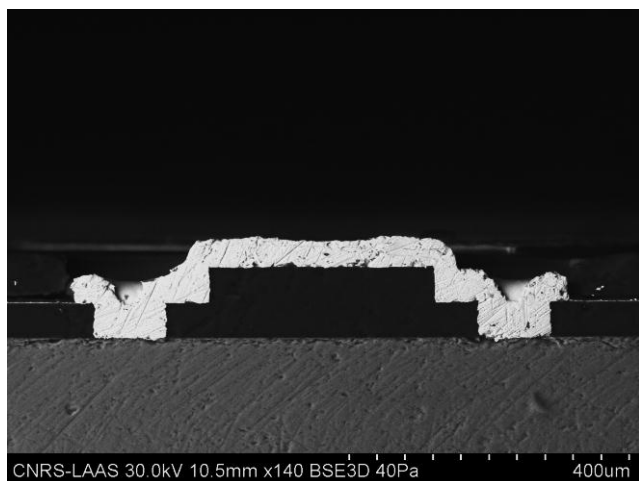


Fig. 9. Cross sectional SEM micrographs of 3D electroplated copper.

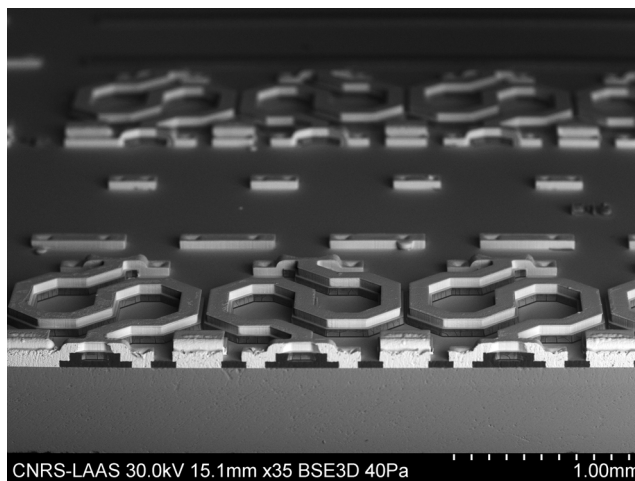


Fig. 10. 3D interconnected inductors integrated above a 50 W LDMOS transistor.

After the validation of the process, 3D interconnected high-Q inductors are designed and integrated above 50 W LDMOS transistors as pre-matching components. Three inductors were designed to have an initial value of $0.75 \text{ nH} \pm 0.05 \text{ nH}$ ($L_1 = 0.7 \text{ nH}$, $L_2 = 0.75 \text{ nH}$, $L_3 = 0.8 \text{ nH}$). For these inductors, two SU-8 layers were used (90 μm total thickness) with the first layer kept on the overall wafer surface and the second patterned under the inductor (pillar/hollow combination). The aim of this combination is to demonstrate the full process ability of managing 3D transitions since copper electroplates with currents in upward and downward directions simultaneously.

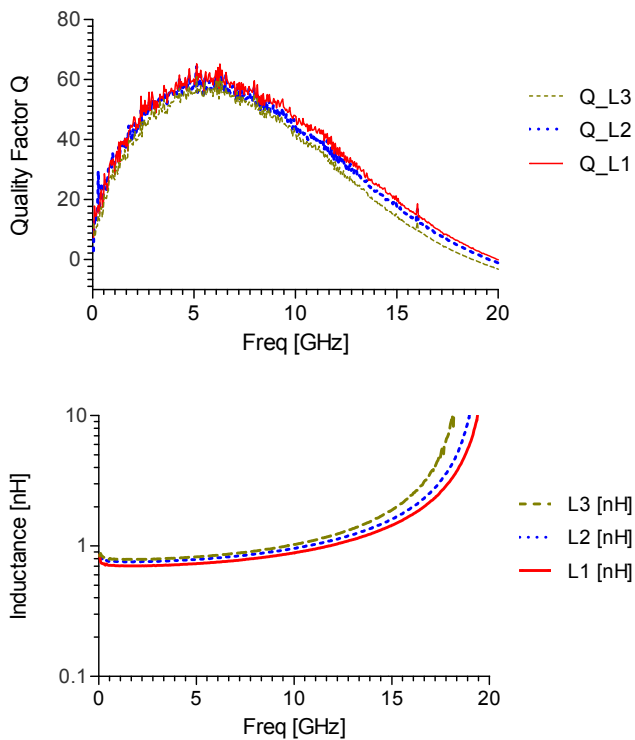


Fig. 11. Measured inductors Q-Factor and inductance values versus frequency.

Fig. 9 shows cross section view of the single step 3D electroplated copper. One can notice the good metallic

structure continuity, as well as the good filling of vias. Fig. 10 presents the inductors as applied above the 50 W LDMOS transistor, as well as the cross sectional view of the interconnection between inductors and transistors.

On-wafer measurements of these inductors exhibit a maximum Q value of 60, 58 and 55 at 6 GHz for a total inductance value of 0.71 (L1), 0.75 (L2) and 0.79 (L3) nH respectively (Fig. 11). The good agreement between measurements and simulations (Fig. 12) must be pointed out, which validates both our inductor optimization and the technological process control.

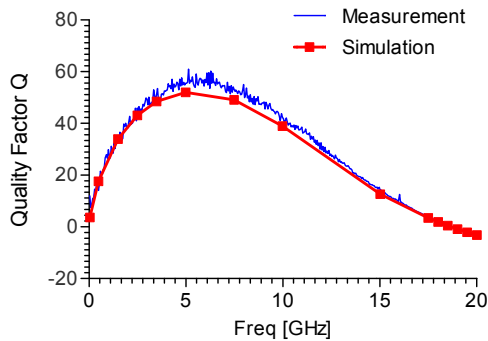


Fig. 12. Measurement and simulation of the inductor's Q factor and inductance value versus frequency

At a 1.85 GHz frequency, load-pull measurements of the pre-matched RF LDMOS transistors yield a maximum output power ($P_{out, max}$) of 48.5 dBm, a maximum gain ($G_{T, max}$) of 14.75 dB and a maximum efficiency (η_{max}) of 54 %. Only a 5% loss has been noticed on efficiency value compared to the bond wired version of the transistors. This small decrease has been traced and appears to be caused by a higher source resistance due to back metal processing. Then, we are able to conclude that inductors integrated with the process we propose exhibit performances which are similar to those of bondwires.

Conclusion

In this paper, a low cost 3d multilevel interconnects integration for RF and microwave applications is presented. The process allows above-IC integration of multi-level 3D interconnects using Through Polymer Vias. It relies on four main steps: patterning of the SU8 based dielectric at specific locations, 3D deposit of a void free and homogenous seed layer on all surfaces and sidewalls, formation of thick molds using the BPN photoresist, and finally 3D copper electroplating. 3D interconnects have been realized on 45 and 90 μm thick SU-8 layers using a single electroplating step. An example of this process application is demonstrated by integrating a 3D solenoid inductor using only two lithography masks. Furthermore, high-Q power inductors using a hollow/pillar configuration are integrated above a 50 W power LDMOS to replace bond-wires of pre-matching circuits. An excellent electroforming of the 3D copper ribbons has been pointed out, and inductor measurements show a Q of 60 at 6 GHz. Load-pull measurements of these transistors yield comparable results to wire-bonded version. Consequently, this technology appears to be very promising for passive device manufacturing since it is able to fit a large range of

applications, like on-chip antenna integration, 3D packaging, 3D baluns/transformers... It is also fully compatible with standard IC manufacturing equipment.

Acknowledgment

The authors would like to thank Jean Marie Boulay and Gerard Bouisse from Freescale Semiconductors for supplying LDMOS wafers. The authors would like to thank also the TEAM group of LAAS-CNRS for his support.

References

- [1] T. Kaho, Y. Yamaguchi, and K. Uehara, "A compact K/Ka-band transceiver MMIC using GaAs 3D-MMIC technology," in *Microwave Conference Proceedings (APMC), 2010 Asia-Pacific*, 2010, pp. 822-825.
- [2] T. Wei, Z. Haiying, and H. Zhirun, "A 3D multilayered Si MMIC left-handed metamaterial bandpass filter," in *Radio-Frequency Integration Technology, 2009. RFIT 2009. IEEE International Symposium on*, 2009, pp. 137-139.
- [3] K. Hettak, K. Elgaid, I. G. Thayne, G. A. Morin, and M. G. Stubbs, "3D MMIC compact semi-lumped loaded CPW stubs for spurious suppression fabricated with a standard air bridge process," in *Microwave Symposium Digest, 2009. MTT '09. IEEE MTT-S International*, 2009, pp. 1033-1036.
- [4] Q. Sun, L. Krishnamurthy, V. T. Vo, and A. A. Rezagadeh, "Compact 3D MMIC spiral baluns using multilayer CPW technology," in *High Frequency Postgraduate Student Colloquium, 2005*, 2005, pp. 87-90.
- [5] S. Pozder, R. Chatterjee, A. Jain, H. Zhihong, R. E. Jones, and E. Acosta, "Progress of 3D Integration Technologies and 3D Interconnects," in *International Interconnect Technology Conference, IEEE 2007*, 2007, pp. 213-215.
- [6] A. Ghannam, *et al.*, "Dielectric microwave characterization of the SU-8 thick resin used in an above IC process," in *Microwave Conference, 2009. EuMC 2009. European*, 2009, pp. 1041-1044.
- [7] T. Ohba, *et al.*, "Thinned wafer multi-stack 3DI technology," *Microelectronic Engineering*, vol. 87, pp. 485-490, 2010.
- [8] A. Yu, *et al.*, "Three dimensional interconnects with high aspect ratio TSVs and fine pitch solder microbumps," in *Electronic Components and Technology Conference, 2009. ECTC 2009*, 59th, 2009, pp. 350-354.
- [9] L. Mirkarimi, *et al.*, "3D interconnects for dense die stack packages," in *3D System Integration, 2009. 3DIC 2009. IEEE International Conference on*, 2009, pp. 1-5.
- [10] M. Saadaoui, *et al.*, "New Front To Back-side 3D Interconnects Based High Aspect Ratio Through Silicon Vias," in *Electronics Packaging Technology Conference, 2008. EPTC 2008. 10th*, 2008, pp. 219-223.
- [11] R. Beica, *et al.*, "Advanced Metallization for 3D Integration," in *Electronics Packaging Technology Conference, 2008. EPTC 2008. 10th*, 2008, pp. 212-218.
- [12] <http://www.microresist.de/produkte/dupont/pdf/wbr2000series.pdf>
- [13] D. Bourrier, *et al.*, "Comparisons of the new thick negative resist to Su8 resist", *SPIE Advanced lithography* San Jose 12 -16 February 2011