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# Fabricate An 8.35-GHz Frequency Synthesizer

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**Abstract:** By developing a low-noise frequency synthesizer at 2 GHz and applying a pair of doublers, it is possible to achieve low-phase-noise outputs past 8 GHz for digital microwave radios.

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Frequency synthesizers are vital components in communications systems, with a wide range of frequencies required for applications ranging from low-cost cellular telephones to millimeter-wave radios. Digital microwave radios (DMRs) have their own sets of demanding requirements for frequency synthesizers, since they typically rely on advanced digital modulation such as quadrature-amplitude-modulation (QAM) and quadrature-phase-shift-keying (QPSK) formats. Fortunately, the authors have developed a frequency synthesizer from 7.6 to 8.6 GHz ideally suited for digital microwave radios that rely on QAM and QPSK modulation formats. The design strategy for synthesizer is outlined here, along with measurements using a commercial spectrum analyzer, showing how the source can deliver signals with low phase noise even close to the carrier.

Frequency synthesizers are frequently used in wireless communication applications. For example, they can be used in transmitting high-definition TV (HDTV) over a wide frequency range.<sup>1</sup> They can also enhance the data resolution in military radar applications and transmit data at rates exceeding 1 Gb/s over a range of several meters.<sup>2</sup> Bandwidth, noise, speed, frequency resolution, acquisition range, dynamic range, stability, and frequency accuracy are all important characteristics for a frequency synthesizer to be used in such communications applications.<sup>3,4</sup> In microwave devices, dual-loop synthesizers and frequency multiplication of an L- or s-band synthesizer are widely used techniques to achieve stable outputs with low noise levels at higher frequencies.<sup>5-7</sup> In the current design, an s-band frequency synthesizer with low phase noise was initially designed; by frequency multiplication, an X-band frequency synthesizer was then designed, fabricated, and evaluated with the aid of a commercial spectrum analyzer.

**Figure 1** shows a simplified block diagram for a phase lock loop (PLL). In the frequency synthesizer, the PLL acts as a stable oscillator with a great deal more flexibility and frequency stability than a stable single-frequency crystal source.

**Figure 2** offers insights into the two methods used to achieve low-phase-noise performance at 8 GHz.

The first method is as follows: With the aid of a programmable counter following the crystal and prior to the loop filter, the output frequency can be maintained at the same frequency stability as the input frequency. Hence, if R is a divider's division ratio and  $F_r$  and  $F_o$  are the respective input and output frequencies, the following relationship can be written:

$$F_o = (1/R)F_r = F_i \quad (1)$$

The second method relies on the aid of a programmable frequency divider, with M in the feedback loop as shown in [Fig. 2](#). In this case, the following relationship can be written:

$$F_o = (N/R)F_r = M \times F_i \quad (2)$$

By choosing a large integer value for M, any frequency is achievable. In addition, higher frequencies with the frequency stability of a crystal reference can be achieved. [Figure 2](#) shows the simplified block diagram for this PLL, including the use of two dividers.

[Figure 3](#) shows the basic block diagram for the 8.35-GHz frequency synthesizer. A 2-GHz PLL is employed to produce a stable frequency with low phase noise. The output of this lower-frequency synthesizer is then converted to 8.35 GHz using frequency multiplier blocks. In [Fig. 3](#), the temperature-compensated crystal oscillator (TCXO) is used to generate a 12-GHz reference signal. The TCXO chip selected for this purpose has good phase-noise and frequency-stability characteristics. [The table](#), "Tracking TCXO phase noise," shows its phase noise at various offset frequencies, including at offset frequencies as close as 1 Hz.

Tracking TCXO phase noise	
Offset from carrier (Hz)	Phase noise (dBc/Hz)
1	-70
10	-100
100	-130
1000	-145
10,000	-150

In [Fig. 3](#), parameters  $f_r$  and  $f_{in}$  are labeled as the reference frequency and the frequency sample of the VCO output signal, respectively. The phase-detection (PD) chip consists of a phase/frequency detector (PFD) and internal M and R digital frequency dividers.

The voltage-controlled oscillator (VCO) used in the 8-GHz frequency design is a monolithic-microwave-integrated- circuit (MMIC) commercially available VCO with broad tuning range. It tunes by means of a 0-to-20-V voltage tuning range.<sup>8</sup> Its DC bias voltage and supply current are +5 VDC and 10 mA, respectively. The output signal frequency of the VCO at pin number 1 is applied to the phase detector input, as illustrated in [Figure 3](#), [Figure 4](#) and [Figure 5](#).

In the fabricated example of the frequency synthesizer, the values of R and M are equal to 16 and 2783, respectively. Thus, the output signal frequency of the PLL is obtained by Eq. 3 for the locked loop state:

$$F_1 = (M/R)F_r \quad F_2 = 2087.25 \text{ MHz} \quad (3)$$

Signal  $F_2$  is passed through two frequency multiplier blocks to produce the required output frequency. The essential components for the frequency doubler circuit block are shown in [Fig. 4](#). The frequency of the final output signal can be found from:

$$F_{\text{out}} = 4 \times F_1 = 8349 \text{ MHz} \quad (4)$$

The circuit schematic of the proposed synthesizer is shown in [Fig. 5](#). It provides great detail for all the passive circuit elements (capacitors and resistors), as well as all the inputs, outputs, power-supply, and control connections for the frequency synthesizer. A photograph of the fabricated 8.35-GHz frequency synthesizer is shown in [Fig. 6](#). The VCO phase noise is equal to -96 dBc/Hz offset 10 kHz from the carrier frequency. The phase noise of the TCXO is -150 dBc/Hz. Thus, its effect on output signal is equal to:

$$(PN_{\text{out}})_{\text{ref}} = PN_{\text{ref}} + 10\log M = -150 + 10\log(4 \times 2783) = -109.5 \text{ dB/Hz} \quad (5)$$

As can be seen in Eq. 5, the numerical spectral purity of the VCO (its phase noise) dominates the calculation of the noise performance of the frequency synthesizer's output signals.<sup>9</sup> The frequency synthesizer's output phase noise is a bit less than that of the VCO, since the noise of the synthesizer's oscillator has been increased by frequency multiplications as well as by passing through other parts of the PLL circuitry.<sup>10</sup> To evaluate the performance of the 8-GHz frequency synthesizer and how it might impact a typical DMR application, it was measured using a model HP 8563A spectrum analyzer from Hewlett-Packard Co. (now [Agilent Technologies](#)). This measured performance is shown in [Fig. 7](#).

The spectrum analyzer's frequency span was set to 50 kHz, while the resolution-bandwidth and video-bandwidth filters were set to 10 kHz and 10 Hz, respectively, to choose appropriate parameters for displaying the carrier as well as its noise sidebands. The display has been set to show 10 dB/div with a reference level of +10 dBm and attenuation of 20 dB, with a center frequency of 8.3499 GHz and a relatively slow sweep speed of 13 s across the 50-kHz display bandwidth. The 55.67-dB power differential between the carrier and the amplitude offset 10 kHz from the carrier leads to the output phase noise of the frequency synthesizer signal as:

$$PN_{\text{overall}} = -55.67 = 10\log(\text{RBW}) = -85.67 \text{ dBc/Hz} \quad (6)$$

This measurement result has good agreement with the phase-noise-performance predicted previously for the 8.35-GHz frequency synthesizer. [Figure 7](#) shows the carrier at a center frequency of 8.34994533 GHz and frequency span of 50 kHz, with extremely well-behaved phase-noise and spurious noise behavior as clear evidence of stable frequency synthesizer performance.

In summary, this report explored the design and fabrication of an 8.35-GHz frequency synthesizer well suited for DMR applications. The design process first involved realizing a 2-GHz frequency synthesizer with phase noise of -98 dBc/Hz offset 10 kHz from the carrier. The outputs of this source were multiplied by means of two frequency doublers, thus achieving the desired 8.35-GHz output frequency and causing some degradation in the final phase-noise performance as a result of the frequency multiplication of the carrier. The phase-noise performance of the final output was reduced by  $20\log 4$  due to frequency multiplication

and the final measured phase noise for the experimental 8.35-GHz frequency synthesizer was -85.67 dB/Hz offset 10 kHz from the carrier, showing good correlation between the initial predicted phase-noise performance levels for the 8.35-GHz frequency synthesizer and the actual measured phase noise performance levels.

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