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Julien Juyon, Ioan Burciu, Teddy Borr, Stéphane Thuries, Éric Tournier. A Low Spurious Level Fractional-N Frequency Divider Based on a DDS-like Phase Accumulation Operation. MIXDES, Jun 2011, Gliwice, Poland. pp.417-421. hal-00714094

HAL Id: hal-00714094

<https://hal.science/hal-00714094>

Submitted on 3 Jul 2012

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A low spurious level fractional-N frequency divider based on a DDS-like phase accumulation operation

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Abstract—This paper presents a novel architecture of a low spurious level fractional-N frequency divider. It has already been shown in previous work that the use of a direct digital synthesizer (DDS) represents a promising solution to the mitigation of the fractional spurs that appear at the output of fractional frequency dividers, but with the drawback of causing a non-linear control of the division ratio. The DDS-based architecture proposed in this paper recovers the benefit of having a linear tuning of the division ratio, while still having similar performance in terms of fractional spurs.

Index Terms—Phase accumulator; fractional-N frequency divider; phase error; frequency division ratio; Direct digital synthesis.

I. INTRODUCTION

The Phase Lock Loop (PLL) structure implements a feedback loop technique that forces the phase of a generated signal to follow the phase of a reference signal. In the radio-communication domain, the major advantage of implementing this technique relies on the improvement of the phase noise (PN) performance of a voltage controlled oscillator (VCO). Studies show that the PN of a VCO based frequency synthesizer is significantly improved when using PLL architecture in order to lock the phase of the VCO to that of the output of a low frequency reference [1].

Moreover, in order to be able to take profit of the low frequency reference PN at a high frequency, the PLL architecture acts as a frequency multiplier by including a frequency divider in the feedback loop (Figure 1). The phase of the signal present at the divider output is then compared with the one of the reference signal by the Phase Frequency Detector (PFD).

The polarity of the phase difference measured by the PFD is used to charge and discharge the filter with the Charge Pump (CP). This amount of charge is proportional to the phase difference measured by the PFD and will turn into voltage that controls the VCO. When the loop reaches the lock conditions, the phase of the VCO output signal will be the same than that of the reference signal. In order to obtain a frequency tuning of the VCO output, the commonly used solution relies on the use of a frequency divider with a programmable division ratio.

When speaking of Integer-N Frequency synthesizer, the programming of the frequency divider is done only by using integer values for the division ratio. As a consequence, the synthesizable frequencies will be multiples of the frequency of the reference signal. The main constraint of the integer-N synthesizers is the fact that the minimum frequency step

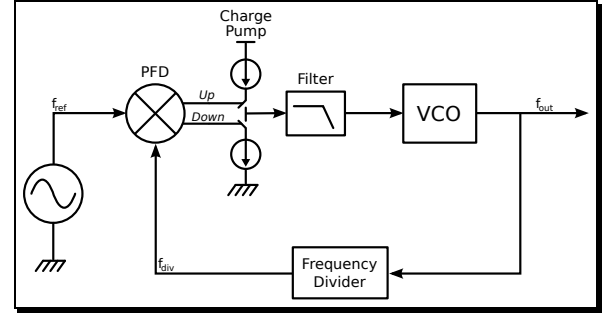


Figure 1. Phase-locked loop

size is equal to the frequency of the reference signal. In order to improve frequency resolution of PLL based frequency synthesizers, we have two types of solutions:

- lowering the frequency of the reference signal while using an integer-N frequency divider in the feedback loop.
- keeping constant the frequency of the reference signal while using a fractional-N frequency synthesizer in the feedback loop [2].

Each of these two solutions has its drawbacks. The decrease of the reference signal frequency implies an increase of the PLL lock time, while the use of fractional-N frequency synthesizers generates parasitic spurs (also called fractional spurs) in the output signal of the CP that will automatically degrade the PN of the global frequency synthesizer [3], [4].

In this paper we are assessing the conception and the design of frequency fractional dividers as well as the impact that these can have on the global performance of a PLL. In the second section, a presentation of different types of fractional frequency dividers will be made. The third section will be dedicated to a novel architecture we propose in order to realize a fractional frequency divider based on a DDS-like phase accumulator operation. In the fourth section, we present several simulation results that were done in order to validate the theoretical study concerning the novel architecture we propose. Finally, conclusions about this study are drawn and the follow-up to this work is provided.

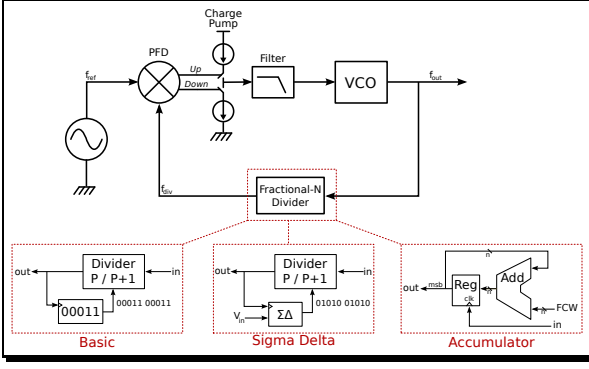


Figure 2. Fractional-N frequency Synthesiser and the different existing fractional frequency divider architectures.

II. FRACTIONAL-N FREQUENCY DIVIDERS

A. Digital Fractional-N Frequency Synthesis

One of the most common used methods for achieving a digital fractional N-frequency synthesis is based on division ratio averaging over time. In order to obtain a fractional frequency division ratio, an output signal is generated from an input signal by alternating two or more integer division ratio over time. The global division ratio is therefore a non-integer which value depends on the ratios used and on their appearance duration as shown in:

$$N.F = N_1P_1 + N_2P_2 + \dots + N_kP_k \quad (1)$$

Where $N.F$ denotes the average division ratio, and N_i and P_i are each integer division ratio and their appearance duration.

The upper part of the schematic presented in Figure 2 shows the architecture of a digital fractional-N frequency divider based PLL. In the lower part we present different architectures that are commonly used in order to implement the digital fractional-N frequency divider.

For the first two implementation scenario, the fractional frequency divider architecture is based on a technique that involves the use of a multiple modulus integer frequency divider. The division ratio is dynamically switched over time through the use of a simple modulus controller. The implementation of this block varies depending on the number of integer division ratios that can be used. In fact, a simple digital phase accumulator (first order sigma delta modulator) can be used for a scenario where the division ratio can vary between only two integer values [1]. If the scenario implies the use of several integer division ratios, the most suited modulus controller architecture is considered to be that of a high order (superior to one) Sigma Delta Modulator (SDM) [5].

The third type of architecture that allows implementing the fractional-N frequency divider relies only on the use of an accumulator. The accumulator is clocked by the input signal while the output is generated by the register Most Significant

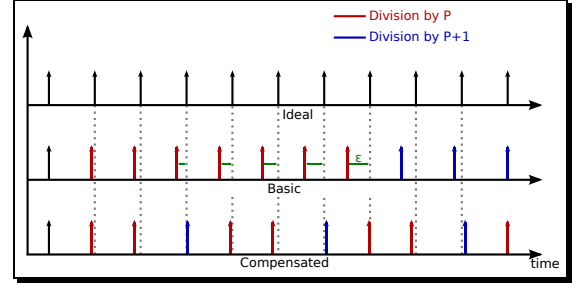


Figure 3. Temporal evolution of the phase error for three different scenarios depending on the implemented fractional frequency divider architecture.

Bit (MSB) [6]. The frequency control word (FCW) imposes the increment step. As shown in [6], if the value chosen for the FCW is not a power of two, the time between two successive overflows of the register is not constant over time. As a consequence, the output signal will have a “period” that varies between two values. Therefore, this accumulator based architecture is naturally switching over time the frequency division ratio between two integer values. The averaged frequency of the output signal f_{out} is defined by:

$$f_{out} = f_{in} \cdot \frac{2^n}{FCW} \quad (2)$$

Where f_{in} is the frequency of the input signal, n is the number of bits used for the register design and FCW is the control word.

B. Fractional Spurs

If the division ratio is constant over time for the ideal fractional frequency divider scenario, the averaging technique used to implement the fractional-N frequency divider imposes a variable frequency division ratio. The period of the output is therefore oscillating between two consecutive multiples of the input signal’s period. As a consequence, a phase error appears when comparing the divider’s output and the ideal divided signal. The schematics shown in Figure 3 show the evolution of this error over time: each of the arrows represent the end of a period of the divider’s output. The phase error signal is represented by the evolution over time of the ε quantity. For an ideal fractional frequency divider this phase error is constantly equal to zero while it evolves for an average technique based divider.

From the PLL point of view, the phase error signal in the output signal of the fractional frequency divider is detected by the PFD. As a consequence, this phase error gives rise to a parasitic current signal at the output of the CP. This parasitic current is transformed into a voltage parasitic signal by the loop filter. If a periodicity characterizes the phase error waveform, the parasite voltage waveform will share this periodicity. Therefore, the spectrum of the VCO input signal will contain parasitic components that depend on the phase error periodicity.

Consequently, spurs appear in the PLL output as the VCO

is modulated periodically. The magnitude of the periodic waveform is large compared to random jitter in the divider based on the average technique. As presented in [3], the fractional spurs generated by the phase error are yielding at typical values of 20 or 30 dBc. Various methods of mitigating the influence of this phase error have been proposed [4]. Three types of correction can be mentioned: current injection based fractional compensation, sigma delta noise shaping and use of Interpolation Zero Crossing method applied to a DDS output.

The current compensation of the phase error is realized by injecting a current pulse train to the integrating capacitor in the loop filter [7]. This current pulse train has the same width but opposite sign than the current signal generated by the phase error. This method is accurate but sensitive to the temperature variation.

The sigma delta noise shaping correction is based on a spread of the energy in the low frequency of the phase error signal towards higher frequency. This noise shaping is realized by destroying the periodicity of the phase error when using a high order sigma delta modulator in order to switch the division ratio between several integer values. As a consequence, the loop filter will be able to filter easily the frequency components present in the noise shaped phase error waveform as they are rejected at high frequency [5].

Finally, the third method of realizing a spur compensated fractional frequency division is based on the integration of a phase accumulator like in direct digital synthesizer architecture. This method is developed in [6]: the phase information generated by the accumulator is converted into an waveform by using a predefined table and a digital to analog converter (DAC). The analog signal is then filtered by a low pass filter. As a consequence, the amplitude of the phase error signal at the output of this component is greatly reduced.

III. DIGITAL N-FRACTIONAL FREQUENCY DIVIDER BASED ON A DIRECT SIGNAL GENERATION

As mentioned in the previous section, one promising solution of realizing a high frequency resolution PLL relies in the use of a DDS based fractional frequency divider. Nevertheless, if this solution offers a better performancecomplexity trade-off compared with PLL using sigma delta compensated dual modulus divider, its major drawback relies in a non-linear evolution of the PLL output frequency depending on the evolution of the FCW injected at the input of the DDS. As mentioned in [6], when implementing a phase accumulator fractional frequency divider, the division ratio (DR) depends on the number N of the accumulator's bits and on the FCW as follows:

$$DR = \frac{f_{clk}}{f_{out}} = \frac{2^n}{FCW} \quad (3)$$

Where f_{out} is the frequency of the output signal and f_{clk} is the frequency of the signal that is driving the accumulator. The control of the division ratio is realized by changing the

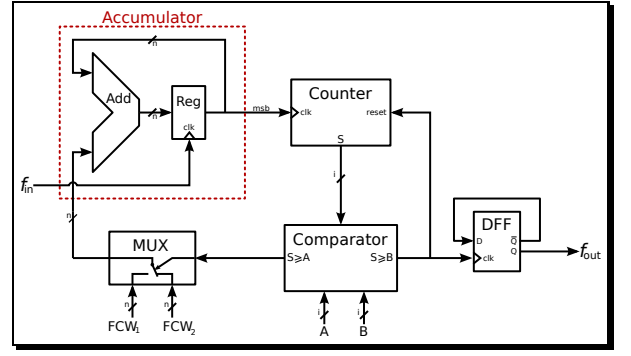


Figure 4. Phase accumulator based architecture

FCW. When the PLL reaches the lock conditions, the output frequency f_{PLLout} of the VCO will be equal to the reference frequency f_{ref} multiplied by the fractional division ratio:

$$f_{PLLout} = f_{ref} \cdot DR = f_{ref} \cdot \frac{2^n}{FCW} \quad (4)$$

Knowing that the reference frequency and the number of bits of the accumulator are constant, it becomes obvious that the evolution of the output frequency of the PLL is not linear depending on the evolution of the FCW.

In order to tackle this linearity evolution issue, this paper aims at proposing and at assessing a novel phase accumulator based fractional frequency divider architecture. The authors consider that this architecture is meant to replace the single phase accumulator of the DDS used to realize a frequency divider similar to that presented in [6].

Figure 4 shows the phase accumulator based architecture that is proposed in order to obtain a linear evolution of the DR.

The main innovation of this proposed architecture is the fact that the FCW that controls the phase accumulator is no more constant over time but is switching between two FCW. The control of this switching operation is realized by implementing a loop through a counter, a comparator and a switch.

As shown in the schematic model, the clock input of the counter is driven by the MSB of the phase accumulator. This corresponds to a counting of the phase accumulator overflow.

The output of the counter is tied to the input of the dual comparator. Depending on the result of the comparisons between the value forwarded by the counter and the A and B values, the two outputs of the comparator will be enabled. As long as the counter output exceeds the A or B value, the comparator will enable the output corresponding to A or B , respectively. While the output corresponding to the comparison with B is used to drive the reset input of the counter, the output that corresponds to the A value comparison is used to drive the switch between two FCW.

Based on the number of the phase accumulator's overflows, the FCW that controls the step increment of this block is changed over time. Moreover, the global system output is generated using the comparison with the B value through the use of a flip-flop.

When analyzing the output signal of the proposed architecture, the evaluation of its period's mean value has to take into account the fact that the FCW injected into the phase accumulator is switched twice during this period. As a consequence, when evaluating the time between two consecutive overflows of the phase accumulator, two scenarios appear depending on the value of the FCW that is injected.

As long as the comparison between the number of overflows doesn't exceed the A value, the mean value of the time between two consecutive overflows of the phase accumulator can be evaluated as DR_1 periods of the input signal. Based on (3), the DR_1 is defined by:

$$DR_1 = \frac{2^n}{FCW_1} \quad (5)$$

In a similar way, as long as the counter outputs a number between the A and B value, the mean value of the time between two consecutive overflows of the phase accumulator can be evaluated as DR_2 periods of the input signal, where:

$$DR_2 = \frac{2^n}{FCW_2} \quad (6)$$

Therefore, based on (5) and (6), the mean global frequency division ratio can be defined by:

$$DR_{GLOBAL} = 2 \left[A \cdot \frac{2^n}{FCW_1} + (B - A) \frac{2^n}{FCW_2} \right] \quad (7)$$

For the proposed fractional frequency divider the tuning of the division ratio is controlled through the A input signal; the B , FCW_1 and FCW_2 input signals are constant over time. It can be observed that the DR evolution becomes linear, at the opposite of the simple phase accumulator architecture.

Therefore, the resolution of the division ratio is defined by the relation shown in (8). This is realized by incrementing A and by developing the difference between the two DR thus obtained:

$$\Delta DR_{GLOBAL} = 2^{n+1} \cdot \left[\frac{FCW_2 - FCW_1}{FCW_1 \cdot FCW_2} \right] \quad (8)$$

IV. RESULTS

In order to validate the results of these theoretical studies, simulations were done using realistic models of a "classical" phase accumulator, and the proposed phase accumulation dedicated architecture. The software used in order to realize these simulations is the Cadence system simulation and analysis [8]. Moreover, the implementation of the two compared structures is modeled by using the IBM BiCMOS 0.13 μm technology.

The first series of simulations aims at validating the linear division ratio evolution regarding the control value. The different parameters characterizing the design of the electronic component and the test set-up are shown in Table

Table I
DIVISION RATIO EVOLUTION TEST PARAMETERS USED TO MODEL THE PROPOSED PHASE ACCUMULATION DEDICATED STRUCTURE

Number of bits of the accumulator	9
FCW_1	50
FCW_2	51
A	64
B	1 to 64
Frequency of the input signal	10 GHz

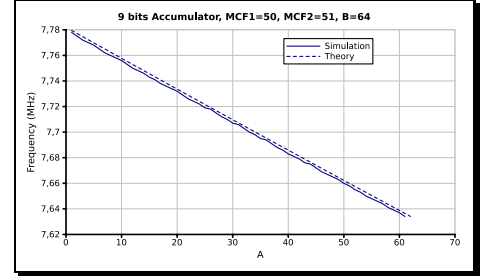


Figure 5. Evolution of the frequency at the output of the proposed structure depending on the evolution of the control value A . The frequency of the input signal is equal to 10 GHz.

I.

The Figure 5 shows that the evolution of the output frequency is linear and that the frequency resolution is equal to 2 kHz for the considered scenario.

Table II
DESIGN AND TEST PARAMETERS OF THE PROPOSED PHASE ACCUMULATION DEDICATED STRUCTURE THAT WAS CHOSEN TO BE COMPARED TO A EQUIVALENT SINGLE ACCUMULATOR STRUCTURE

Number of bits of the accumulator	8
FCW_1	40
FCW_2	41
A	64
B	1 to 64
Frequency of the input signal	10 GHz

Concerning the proposed phase accumulation dedicated structure, the parameters used during the modeling stage are presented in Table II. A second fractional frequency division structure with a single 20 bits accumulator was chosen. This accumulator size of 20 bits is chosen in such a manner that the division ratio performance is similar to those obtained when using the proposed architecture. The value of the FCW injected in this simple phase accumulator was chosen to be equal to 3753. For both compared structures, the frequency of the input signal is equal to 10 GHz. The output signal's frequency is of 35.7891 MHz and 35.7914 MHz for the implementation scenario of the proposed architecture and the single 20 bits accumulator respectively.

The phase error signals generated when using each of the two phase accumulation dedicated architectures are cosimulated by Cadence/Matlab. The time difference is evaluated between the rising edges of the output signals of each of the two fractional frequency dividers and reference signals having

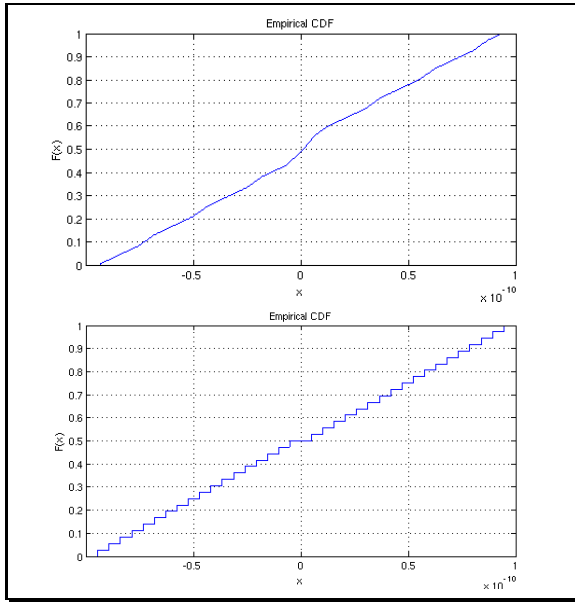


Figure 6. CDF of the phase error corresponding to a use of the simple 20 bits phase accumulator (up) and to the proposed phase accumulation dedicated structure (down).

constant frequencies of 35.7891 MHz and 35.7914 MHz respectively. The phase error is analyzed by using a probabilistic approach and by a comparative study of the frequency spectrums. The probabilistic approach is done by evaluating the Cumulative Distribution Function (CDF) realized over a large population of phase error values. The CDF function can be therefore defined by:

$$F(x) = CDF(err) = Probability(err < x) \quad (9)$$

where err represents the phase error variable.

The graphics of Figure 6 show the CDF of phase error populations issued of implementation scenarios of the two analyzed fractional frequency dividers.

It can be seen that the time evaluated values of the phase error are linearly distributed between the same levels for the two implementation scenarios.

Moreover, the frequency spectrums of the signals corresponding to the phase error generated by the use of each of the two frequency dividers are presented by the charts of Figure 7. It can be seen that the power levels of the spurs generated by the phase error are similar for the two scenarios.

V. CONCLUSION

This paper presents a novel DDS-based fractional frequency divider with a phase accumulation dedicated structure. Unlike a single accumulator architecture that is commonly implemented in the DDS structure in order to realize the phase accumulation operation, the integration of this block allows a linear control of the division ratio when using the DDS as a fractional frequency divider. It has been

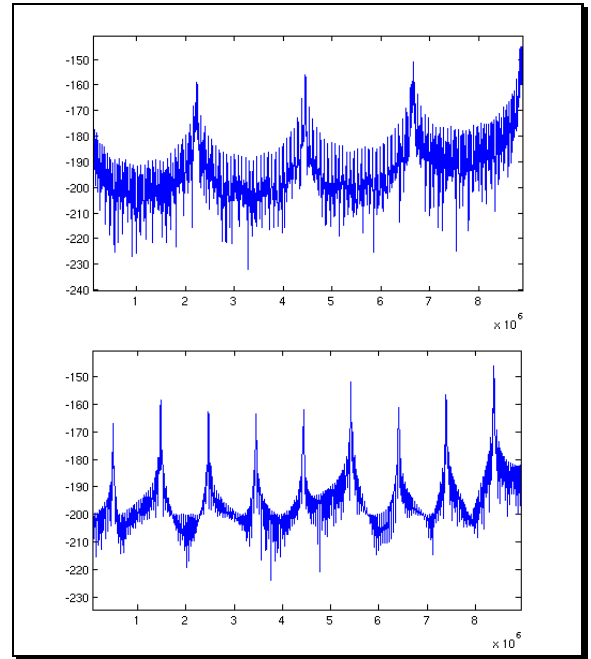


Figure 7. Frequency spectrums of the phase error corresponding to a use of the simple 20 bits phase accumulator (up) and to the proposed phase accumulation dedicated structure (down).

shown that the performance of the proposed architecture is similar to that of a single accumulator structure but with a significantly reduced complexity. It can be concluded that the proposed architecture offers a much better performance-complexity-power consumption trade-off when compared to a single accumulator structure.

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