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A both Gaussian and sinusoidal phase-to-amplitude converter for low-power ultra-high-speed direct digital synthesizers

Teddy Borr, Julien Juyon, Éric Tournier

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PAC presented in this paper, in a similar approach, adds the possibility to generate also a gaussian shape through a simple reconfiguration technique. A DDS with a 9-bit pipeline PA, a 2×4 -bit plus 1-bit accumulator scheme, a 8-bit current-steering linear DAC, and this new PAC has then been designed in a 3-stage Emitter-Coupled-Logic.

III. PHASE-TO-AMPLITUDE CONVERTER

The Gaussian/Sinus Phase-to-Amplitude Converter (G/S-PAC) proposed on fig. 3 is made up of two differential pairs of bipolar transistors (Q_1, Q_2) and (Q_3, Q_4), both biased at the same current (I_p) and with the same voltage reference (V_a).

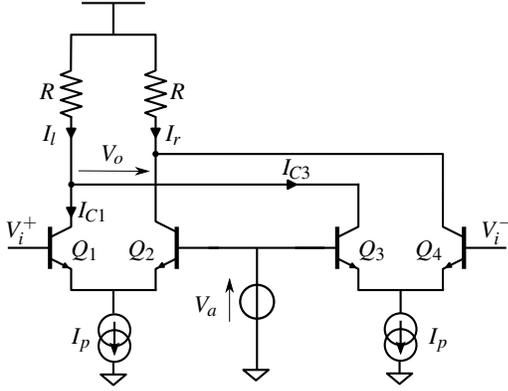


Fig. 3: Schematic of the G/S-PAC

The G/S-PAC is driven in large-signal conditions with a differential triangular signal ($V_i^+ - V_i^-$) generated by the DDS. The circuit is biased and routed in such a way that a positive (negative) gaussian pulse is generated at G/S-PAC output for the positive (negative) part of the triangular input signal (fig. 4).

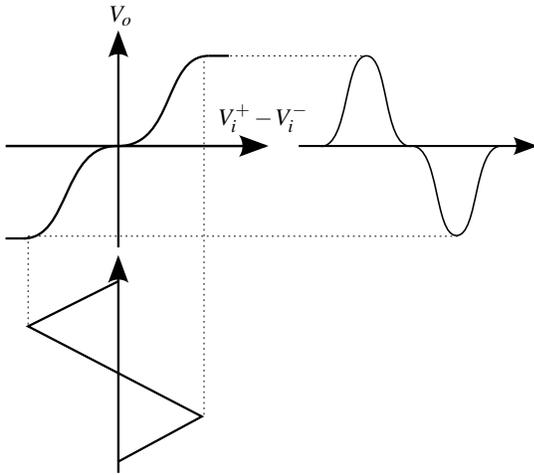


Fig. 4: Principle of the triangle-to-gaussian conversion

According to Kirchoff law, the left branch current I_l of the G/S-PAC circuit is

$$I_l = I_{C1} + I_{C3} \quad (1)$$

As a first approximation, we can assume Ebers-Moll model for bipolar transistors. With a forward gain $\alpha_F = 1$, equation (1) becomes

$$I_l = \frac{I_p}{2} \left[2 + \tanh\left(\frac{V_i^+ - V_a}{2U_T}\right) + \tanh\left(\frac{V_a - V_i^-}{2U_T}\right) \right] \quad (2)$$

In the same way, the right branch current I_r is

$$I_r = \frac{I_p}{2} \left[2 - \tanh\left(\frac{V_i^+ - V_a}{2U_T}\right) - \tanh\left(\frac{V_a - V_i^-}{2U_T}\right) \right] \quad (3)$$

Considering the differential output voltage V_o as the product between load resistor R and the differential current $I = I_l - I_r$, equations (2) and (3) give the sum of input/output relationships in large signal condition for differential amplifiers following hyperbolic tangent law

$$V_o = RI_p \left[\tanh\left(\frac{V_i^+ - V_a}{2U_T}\right) + \tanh\left(\frac{V_a - V_i^-}{2U_T}\right) \right] \quad (4)$$

Introducing variables

- $V_i = V_i^+ - V_i^-$ as differential mode input voltage,
- $V_c = (V_i^+ + V_i^-)/2$ as common mode input voltage,
- $a = 2(V_a - V_c)$,

and re-injecting these in equation (4) leads to the direct relation between differential output voltage V_o , input differential voltage V_i and the introduced parameter a

$$V_o = RI_p \left[\tanh\left(\frac{V_i - a}{4U_T}\right) + \tanh\left(\frac{V_i + a}{4U_T}\right) \right] \quad (5)$$

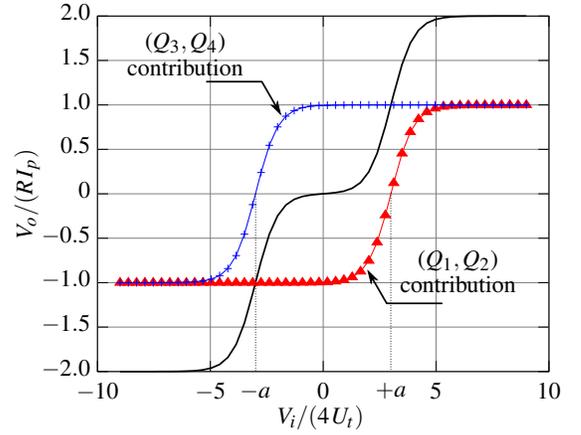


Fig. 5: Normalized input/output G/S-PAC's transfer characteristic.

Equation (5) and each of its tanh components showing two distinct saturation levels are plotted fig. 5. The proposed structure uses the "a" parameter to shift both tanh characteristics by $\pm a$ along the horizontal $V_i/(4U_T)$ axis. Thus, with "a" properly chosen, a positive differential input voltage sets up (Q_3, Q_4) in *positive* saturation while (Q_1, Q_2) pair imposes its tanh behavior. Likewise, a negative input voltage sets up (Q_1, Q_2) in *negative* saturation while (Q_3, Q_4) pair imposes its tanh behavior. Thereby, by applying a differential triangular input voltage, the positive (or negative) side gives a good

approximation of a gaussian pulse by hyperbolic tangent. Moreover, if "a" is chosen equal to zero, V_o can be rewritten as

$$V_o = 2RI_p \tanh\left(\frac{V_i}{4U_T}\right) \quad (6)$$

Thus, $a = 0$ (i.e. $V_a = V_c$) leads to a pure tanh behavior for the G/S-PAC. With amplitude of V_i properly chosen, the differential triangular input voltage is curved, following tanh law, to approximate a sine wave.

IV. SIMULATIONS AND RESULTS

In order to properly set up the amplitude of the triangular input voltage applied by the DDS to the G/S-PAC, an *ideal* triangular signal generator has been used to drive the G/S-PAC in optimization simulations. The well-known bell shaped frequency spectrum of generated gaussian pulses is plotted fig. 6 for various amplitude of G/S-PAC input voltage.

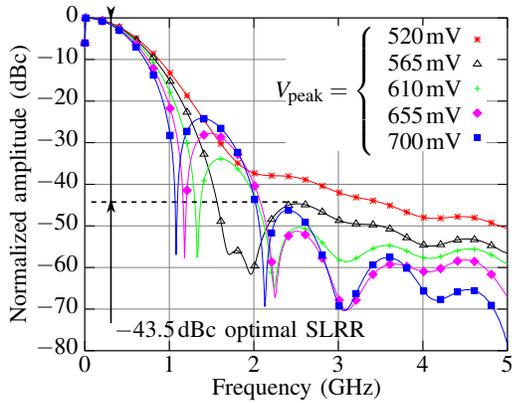


Fig. 6: Frequency spectrum of gaussian shaped pulses for various peak amplitudes from an ideal generator.

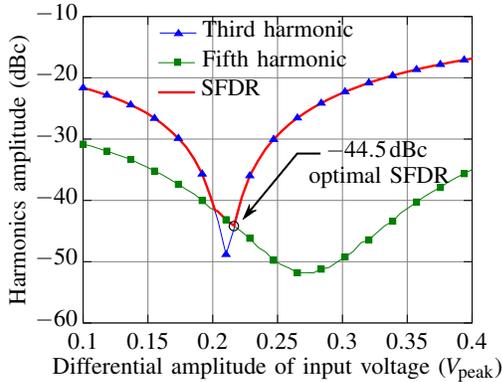


Fig. 7: Sinus' harmonics and resulting SFDR versus peak amplitude of input voltage from an ideal generator.

The tanh approximation introduces side-lobes that can be minimized to a Side Lobes Rejection Ratio (SLRR) of -43.5 dBc for an input peak amplitude voltage of 565 mV obtained with $V_c = 1.59$ V and $V_a = 1.77$ V. The same optimisation is made for the sinus-mode. The third and the fifth harmonics of the generated sinus are plotted fig. 7 versus the

triangle amplitude. An optimal Spurious Free Dynamic Range (SFDR) of -44.5 dBc can be reached for a peak amplitude voltage of 220 mV obtained with $V_c = V_a = 1.79$ V.

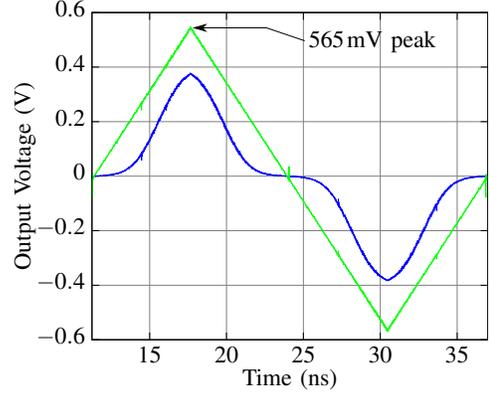


Fig. 8: Transient simulation for gaussian-mode G/S-PAC driven by a DDS with phase increment of 1 and $F_{clk} = 20$ GHz

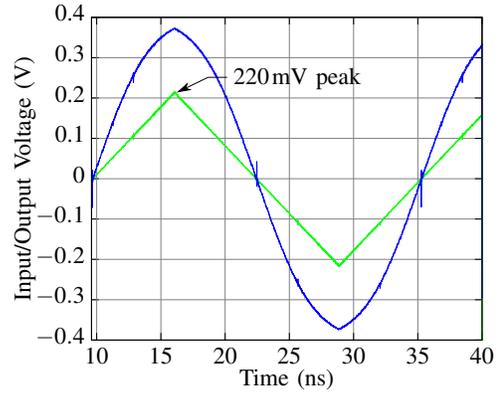


Fig. 9: Transient simulation for sinus-mode G/S-PAC driven by a DDS with phase increment of 1 and $F_{clk} = 20$ GHz

The G/S-PAC proposed in this paper has been used to design a first version of a 9-bit ROM-less DDS in the IBM $0.13\mu\text{m}$ BiCMOS SiGe process. This technology provides high-performance HBT with f_i/f_{max} of $200/250$ GHz. Obviously, our G/S-PAC require a calibration phase. In order to reach optimal performances in future measurements, the DAC of the DDS architecture has been designed with a voltage controlled output amplitude. Since SFDR and SLRR depend on DAC linearity and matching of components, the analog part of the circuit's layout has been focused on these two main constraints.

The full circuit has been simulated with BSIM4 model for MOS transistors and VBIC model for HBT with process parameters filled from the BiCMOS8HP design kit to Spectre simulator under Cadence 5.1.41. The DDS has been simulated at a maximum operating clock frequency of 20 GHz and consumes only 585 mW (209 mA under 2.8 V). Such a consumption should be considered low for DDS and can be compared to those of others in tab. I, in which our DDS exhibit a high FOM. Further optimizations should improve this consumption.

TABLE I: Comparison of different ultra high-speed DDS

Ref.	Technology process	f_i NPN (GHz)	Clock freq. (MHz)	Acc. size (bit)	Accumulator decomposition	Power (mW)	Die area (mm ²)	FOM $\frac{\text{MHz} \times \text{bit}}{\text{mW} \times \text{mm}^2}$	FOM $\frac{\text{MHz}}{\text{mW}}$
[11]	0.35 μm SiGe	60	1700	32		3000	24	0.76	0.57
[12]	0.35 μm CMOS		2000	8		820	3.99	4.89	2.44
[13]	1 μm bipolar	22	2500	31	1 \times 31	5000	20	0.78	0.5
[14]	0.35 μm SiGe	47	5000	8	8 \times 1	2000	2	10	2.5
[15]	Bipolar InP	137	9200	8	8 \times 1	15000	40	0.12	0.61
[5]	Bipolar InP	300	13000	8	1 \times 8	5420	3.92	4.90	2.4
[16]	Bipolar InP	300	32000	8	4 \times 2	9450	3.92	6.91	3.39
[6]	0.25 μm SiGe	70	6000	9	1 \times 9	308	1	175.32	19.48
[17]	0.09 μm CMOS		1300	24	6 \times 4	350	2	44.6	3.71
[18]	0.35 μm SiGe	200	15000	8	4 \times 2	366	1.16	282.76	40.98
This work (simulated)	0.13 μm SiGe	200	20000	9	1 + 2 \times 4	585	1.32	233.02	34.19

Triangular signals provided by the DDS for a phase increment of 1 and the corresponding G/S-PAC output voltages are plotted fig. 8 and fig. 9.

V. CONCLUSION

A novel phase-to-amplitude converter offering gaussian shape capability together with the more classical sinusoidal shape extends low-cost low-power and high-speed DDS panel of waveform. Our G/S-PAC exhibit an optimal simulated SLRR of -43.5 dBc in gaussian mode, a SFDR of -44.5 dBc in sinus mode, and has allowed the design of an ultra-high-speed 20 GHz simulated DDS with a 9-bit frequency resolution, an 8-bit amplitude resolution, on an IBM 0.13 μm BiCMOS SiGe technology.

REFERENCES

- [1] J. Tierney, C. Rader, and B. Gold, A digital frequency synthesizer, *Audio and Electroacoustics, IEEE Transactions on*, vol. 19, pp. 48 – 57, mar 1971.
- [2] X. Geng, F. Dai, J. Irwin, and R. Jaeger, 24-Bit 5.0 GHz Direct Digital Synthesizer RFIC With Direct Digital Modulations in 0.13 μm SiGe BiCMOS Technology, *Solid-State Circuits, IEEE Journal of*, vol. 45, pp. 944 –954, may 2010.
- [3] X. Geng, X. Yu, F. Dai, J. Irwin, and R. Jaeger, An 11-bit 8.6GHz direct digital synthesizer MMIC with 10-bit segmented nonlinear DAC, in *Proc. 34th European Solid-State Circuits Conference ESSCIRC 2008*, pp. 362–365, 15–19 Sept. 2008.
- [4] G. Chen, D. Wu, Z. Jin, and X. Liu, An ultra-high-speed direct digital synthesizer MMIC, in *Microwave and Millimeter Wave Technology (ICMMT), 2010 International Conference on*, pp. 217 –220, 8-11 2010.
- [5] S. Turner and D. Kotecki, Direct Digital Synthesizer With Sine-Weighted DAC at 32-GHz Clock Frequency in InP DHB Technology, *IEEE Journal of Solid-State Circuits*, vol. 41, pp. 2284–2290, Oct. 2006.
- [6] S. Thuries, É. Tournier, A. Cathelin, S. Godet, and J. Graffeuil, A 6-GHz Low-Power BiCMOS SiGe:C 0.25 μm Direct Digital Synthesizer, *Microwave and Wireless Components Letters, IEEE*, vol. 18, pp. 46–48, Jan. 2008.
- [7] B. Laemmle, C. Wagner, H. Knapp, H. Jaeger, L. Maurer, and R. Weigel, A Differential Pair-Based Direct Digital Synthesizer MMIC With 16.8-GHz Clock and 488-mW Power Consumption, *Microwave Theory and Techniques, IEEE Transactions on*, vol. 58, pp. 1375 –1383, may 2010.
- [8] S. Thuries and É. Tournier, A DDS-oriented phase-to-amplitude converter using a SiGe:C bipolar transistors differential pair, in *Proc. IEEE International Workshop on Radio-Frequency Integration Technology: Integrated Circuits for Wideband Communication and Wireless Sensor Networks*, pp. 211–214, 30 Nov.–2 Dec. 2005.
- [9] R. Meyer, W. Sansen, and S. Peeters, The differential pair as a triangle-sine wave converter, *Solid-State Circuits, IEEE Journal of*, vol. 11, pp. 418–420, Jun 1976.
- [10] J. Gerrits and J. Farserotu, Wavelet generation circuit for UWB impulse radio applications, *Electronics Letters*, vol. 38, pp. 1737 – 1738, 5 2002.
- [11] K.-H. Baek, E. Merlo, M.-J. Choe, A. Yen, and M. Sahriling, A 1.7GHz 3V direct digital frequency synthesizer with an on-chip DAC in 0.35 μm SiGe BiCMOS, in *Solid-State Circuits Conference, 2005. Digest of Technical Papers. ISSCC. 2005 IEEE International*, pp. 114–587 Vol. 1, 2005.
- [12] X. Yu, F. Dai, Y. Shi, and R. Zhu, 2 GHz 8-bit CMOS ROM-less direct digital frequency synthesizer, *Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on*, pp. 4397–4400 Vol. 5, May 2005.
- [13] P. H. Saul and D. G. Taylor, A high-speed direct frequency synthesizer, *Solid-State Circuits, IEEE Journal of*, vol. 25, no. 1, pp. 215–219, 1990.
- [14] F. Dai, L. Chimakurthy, D. Yang, J. Huang, and R. Jaeger, A low power 5 GHz direct digital synthesizer designed in SiGe technology, in *Proc. Digest of Papers Silicon Monolithic Integrated Circuits in RF Systems 2004 Topical Meeting on*, pp. 21–24, 8–10 Sept. 2004.
- [15] A. Gutierrez-Aitken, J. Matsui, E. Kaneshiro, B. Oyama, D. Sawdai, A. Oki, and D. Streit, Ultrahigh-speed direct digital synthesizer using InP DHB technology, *IEEE Journal of Solid-State Circuits*, vol. 37, pp. 1115–1119, Sep 2002.
- [16] S. Turner and D. Kotecki, Direct digital synthesizer with ROM-Less architecture at 13-GHz clock frequency in InP DHB technology, *IEEE Microwave and Wireless Components Letters*, vol. 16, pp. 296–298, May 2006.
- [17] H. C. Yeoh, J.-H. Jung, Y.-H. Jung, and K.-H. Baek, A 1.3-GHz 350-mW Hybrid Direct Digital Frequency Synthesizer in 90-nm CMOS, *Solid-State Circuits, IEEE Journal of*, vol. 45, pp. 1845 –1855, sept. 2010.
- [18] B. Laemmle, C. Wagner, H. Knapp, L. Maurer, and R. Weigel, A 366mW direct digital synthesizer at 15GHz clock frequency in SiGe Bipolar technology, in *Proc. IEEE Radio Frequency Integrated Circuits Symp. RFIC 2009*, pp. 415–418, 2009.