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# Evaluation of silver-sintering die attach

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## Abstract

Silver sintering die attach is a promising technology for high temperature power electronics packaging. In this paper, we evaluate its performances in terms of thermal resistance and high temperature stability. The thermal resistance is measured on test vehicles assembled under different conditions, using silver pastes from NBETech and Heraeus, with different process parameters. The stability test is performed by storing samples at an elevated temperature (300°C) in air, with a strong voltage bias (1100 V) for several hours.

## 1 Introduction

The development of power components based on silicon carbide (SiC) allows for the design of power converter operating at high temperature (above 200 or 300°C). SiC is a semiconductor material with a large band gap that is not only able to operate at temperatures exceeding 300°C but also offers fast switching speed, high voltage blocking capability and high thermal conductivity compared to silicon technology components.

The classical die attach technology uses high temperature solder alloys which melt at around 300°C. However, even a die attach with such high melting point can only operate up to a much lower temperature. A 0.8 ratio between the melting and operating temperatures (both expressed in Kelvin) is commonly accepted [1]. This means that the solder which melts at 300°C (573 K) can only operate at temperatures below 185°C (573 x 0.8 = 458 K). Alternative die attach solutions have recently been proposed: Transient Liquid Phase Bonding [2], soldering with higher melting point alloys such as ZnSn [3], or silver sintering [4, 5].

In this study, we will focus on assessing the electrical performance of this latter technique which is becoming mature. Indeed, silver sintering is a very interesting technology, as silver offers very good thermal conductivity (429W/m.K, better than copper), relatively inexpensive (compared to alternative solutions which often use gold), and has a very high melting point (961°C).

In particular, two aspects of the silver sintering technology will be investigated: the thermal conductivity of the die attach, and the possible formation of conductive silver filaments by migration. Of course, this constitutes only a partial evaluation of the technology, additional tests are needed, such as thermal cycling, to achieve a complete characterization.

## 2 Assessment of thermal resistivity

### 2.1 Description of the vehicle test assembly

In order to assess the influence of the silver joint on the overall thermal resistivity ( $R_{th}$ ), four preliminary test vehicles (TV) are assembled with different sintering process:

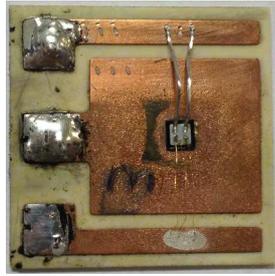
- Two using a paste based on silver micro particles (Heraeus, ref. 043-06P2)
- Two using a paste based on silver nano particles (NBE Tech, Nanotach)

Each TV is made with a silicon carbide diode chip (SICED 1200V/15A, 2.7x2.7 mm<sup>2</sup>) and DCB substrate (Al<sub>2</sub>O<sub>3</sub> with bare, 300 µm-thick copper metallization).

The silver paste is deposited on the DCB using a 100 micron-thick stainless steel screen. In addition to the variation of the paste (micro or nano) two other parameters are changed between the TVs: the pressure applied to the dies (1.3 or 6.4 MPa), and the moment the die is placed on the paste deposit (before or after drying). These parameters are summarized in Table 1, and the practical assembly process is described in [6]. After assembly, each chip is wire-bonded with 2 aluminium wires (Figure 1).

TV #	Silver paste	Chip location	Pressure [MPa]	Chip deposit
1	Micro	Side	6.4	Before paste drying
2	Micro	Center	6.4	After paste drying
3	Nano	Center	6.4	Before paste drying
4	Nano	Center	1.3	Before paste drying

**Table 1:** sintering process data. Micro: Heraeus paste; Nano: NBE Tech paste; side: die located near the edge of the substrate; center: die located at the center of the substrate



**Figure 1** : test vehicle, showing the SiC die (2.7x2.7 mm<sup>2</sup>), connected with 2 aluminium and 3 gold wire bonds . The dark area is due to oxidation of the copper during the sintering process.

## 2.2 Thermal Characterization

The thermal resistance measurement technique described here can be applied to most power semiconductor devices (MOSFETs, Thyristors, Diodes, IGBT). It is based on thermally sensitive electrical parameter used as a junction temperature indicator [7].

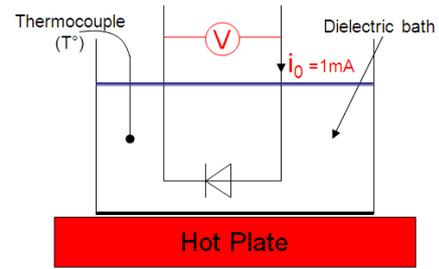
The measurements are performed using a thermal analyzer located at the IMS laboratory (Figure 2).



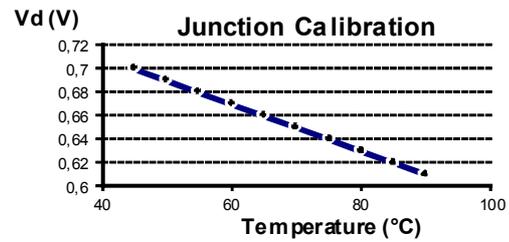
**Figure 2**: test bench for thermal resistance measurement

The test is divided into two steps: the first is the calibration, followed by the thermal resistance measurement.

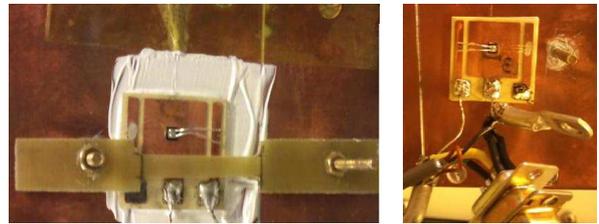
The calibration for each TV is necessary and consists in immersing the TV, which is connected to a low value current generator, in a temperature controlled dielectric bath (Figure 3). Several measurements of the resulting forward voltage are obtained at 5°C increments from 90°C down to 45°C. The initial temperature was the maximum temperature (90°C) then the temperature was decreased for the following measurement (Figure 4). It is more difficult to get an accurate measurement due to thermal overshoot in the opposite case (from cold to hot). A constant current “ $i_0$ ” of 1mA is injected into the diode producing a negligible self-heating of the chip. At the thermal equilibrium, the voltage drop across the diode and the junction temperature ( $T_j$ ) are measured. The relationship between the voltage and temperature is linear, with a slope of  $-2\text{mV} / ^\circ\text{C}$ .



**Figure 3**: The junction calibration setup



**Figure 4**: The junction calibration of the chip



**Figure 5** : Test vehicle #4 fixed on the cold plate with thermal grease (left) and test vehicle #3, attached using the double adhesive TIM layer (right)

Once the calibration is obtained, the sample is cleaned with acetone and dried in air before being connected to the thermal analyser to measure the  $R_{th}$  and attached to a cold plate as depicted in Figure 5 to control its thermal environment.

A thermocouple is placed between the controlled cold plate and a Thermal Interface Material (TIM) layer in order to measure the cold plate temperature  $T_{cold\ plate}$ . Adding a TIM allows to reduce the contact thermal resistance between the case and the cold plate. Different TIM are used to attach the test vehicle to the cold plate (Table 2). A double-sided TIM adhesive (ref-2 sided 3M 467 PSA), a thermal grease layer and a non-adhesive TIM layer were tested for the measurement. In the case of the TIM adhes-

Material	Reference	Thickness (mm)	Thermal Cond. (W/m.K)	$R_{th}$ (K/W)
Adhesive	2 sided 3M 467 p.s.a	0.15	1	0.2
Non-Adhesive	HF105-0.005-00-1212	0.14	0.9	0.21
Grease	HTC-Non Silicon Heat Transfer Compound	-	0.9	-

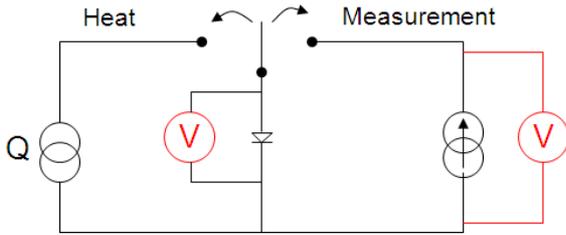
**Table 2**: Thermal properties of the TIM layers

ive layer, an un-controlled pressure is applied by pressing manually on the entire sample. For the two others layers, we use a torque screwdriver to fix the sample.

The adhesive TIM was chosen because its constant thickness and homogeneous bonding capability makes it possible to achieve a controlled thermal performance without applying a pressure during the measurement (this is not the case with the two other TIMs).

The measurement is performed automatically by the Anatech Phase 10 analyzer, and can be explained with two steps (Figure 6) :

- In the first step, the device under test is connected to a high (several amps) current source (left source in Figure 6). This results in an increase of the junction temperature of the diode,
- The power source is then rapidly (a few microseconds) disconnected, and a low value current source is connected to the diode. This current value is identical to that used during calibration, which means the calibration curve in Figure 4 can be used to determine the junction temperature reached by the diode from its forward voltage.



**Figure 6:** Schematic description of the steps of the thermal resistance measurement

The dissipated power in the component is calculated from the voltage and current measurements:

$$Q = P = V \times I \quad [W]$$

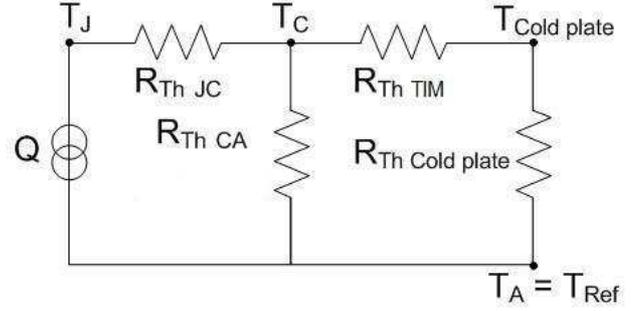
With:

- Q: the heat dissipated by the chip
- P: the dissipated power
- V: the voltage across the diode
- I: the injected current

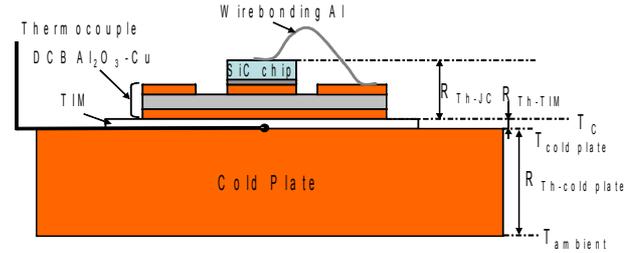
As the most of the heat is transferred by conduction, the convection (and radiation) mechanisms can be neglected. The thermal resistance of the assembly is the sum of all thermal resistances Figure 7:

- $R_{Th-JC}$  is the thermal resistance between the junction of the die and bottom side of the DCB substrate
- $R_{Th-coldplate}$  is the thermal resistance within the cold plate
- $R_{th-TIM}$  is the thermal resistance of the TIM layer
- $R_{Th-CA}$ , the thermal resistance between the junction and the air, due to convection, which is considered negligible here.

The equation for measuring the thermal resistance in steady state is written as follows:



**Figure 7:** Thermal equivalent circuit of the assembly in Figure 8



**Figure 8** Schematic description of the thermal resistance measurement method ( $R_{th}$ )

$$R_{Th} = \frac{\Delta T}{Q} = \frac{T_J - T_A}{Q} \quad [K/W]$$

### 2.3 Experimental Results

The thermal equilibrium is achieved with a 3.8 amps injected current load, resulting in heat dissipation of about 4.5 Watts (Table 3). TV1 has the highest thermal resistance value which can be explained by the location of the chip on the DCB substrate. (Table 1)

The  $R_{Th}$  measured includes the  $R_{Th}$  of the TIM layer that we used to fix the TV on the cold plate.

Another set of measurements was made with a thermal equilibrium achieved with a 5 amps current load. The results are summarized in Table 4, showing that the previous applied power (4.5 W) was high enough for the measurement.

TV #	Size grain	Thermal layer	$P_D$ [W]	$T_J$ [°C]	$T_A$ [°C]	$R_{Th}$ [K/W]
1	micro	Adh.	4.44	41	28.5	2.83
1	micro	grease	4.44	38.3	26.5	2.67
2	micro	Adh.	4.56	37	27.6	2.06
2	micro	grease	4.56	37.4	28.8	2.11
2	micro	N-adh	4.6	58.6	26.8	6.9
3	Nano	Adh	4.47	35.9	26.7	2.07
3	Nano	grease	4.47	38.5	30.6	1.76
3	Nano	N-adh	4.48	48.6	27.4	4.72
4	Nano	Adh.	4.41	37.2	28	2.08
4	Nano	N-adh	4.45	46.5	26.6	4.46

$P_D$ : Dissipated Power,  $T_J$ : Junction Temperature,  $T_A$ : Ambient Temperature,  $R_{Th}$ : Thermal Resistance, Th.layer: Thermal layer, N-adh: Non-adhesive layer

**Table 3:** Thermal resistance measurement of the test vehicles wirebonding, with 3.8 amps current load.

TV	Size grain	Thermal layer	P <sub>D</sub> [W]	T <sub>J</sub> [°C]	T <sub>A</sub> [°C]	R <sub>TH</sub> [K/W]
1	micro	adh.	6.29	49.3	30.5	2.98
1	micro	grease	6.23	43.6	27	2.66
1	micro	N-adh	6.35	66.5	30.7	5.64
2	micro	adh.	6.44	41.9	27.4	2.25
2	micro	grease	6.45	43.5	29	2.25
2	Nano	N-adh	6.6	71.5	27.3	6.7
3	Nano	adh.	6.29	40.5	27.2	2.11
3	Nano	grease	6.31	43.9	32.5	1.79
3	Nano	N-adh	6.37	58.5	28.2	4.75
4	Nano	adh.	6.26	42.9	27.4	2.48
4	Nano	N-adh	6.3	56.3	27	4.64

P<sub>D</sub>: Dissipated Power, T<sub>J</sub>: Junction Temperature, T<sub>A</sub>: Ambient Temperature, R<sub>TH</sub>: Thermal Resistance, Th.layer: Thermal layer, N-adh: Non-adhesive layer

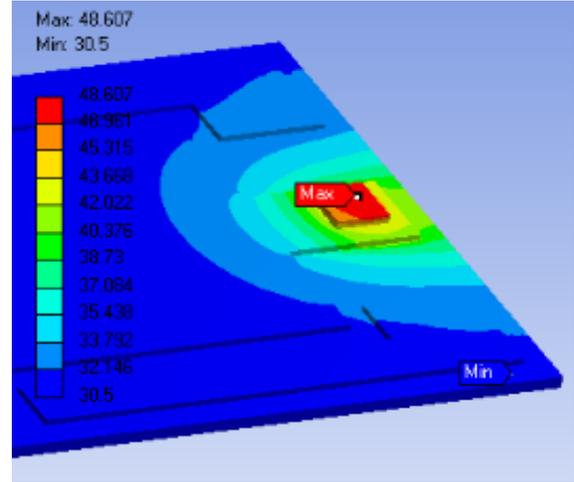
**Table 4:** Thermal resistance measurement of two types of test vehicle using the micro- and nano-silver particles for the die-attach and aluminium wirebonding, with 5 amps current load.

In most cases, the results in Table 3 and Table 4 are comparable (less than 10% variation). However, it must be noticed that for a given TV, the thermal resistance changes a lot with the nature of the TIM. And for a given TIM, the results are widely different between the TVs. In fact, the adhesive TIM gives the most consistent result. The grease gives very different results between the TVs. This is due to the un-controlled thickness of the grease deposit, and a better dispersing solution should be used (screen printing).

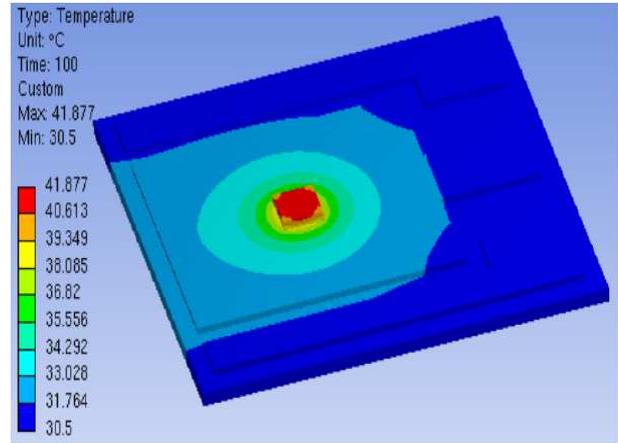
In Table 3, for an adhesive TIM, TV1 exhibits a much higher R<sub>th</sub> value (2.83 K/W vs 2.06, 2.07, 2.08 K/W for TV2, 3, and 4 respectively). This is because the die in TV1 was bonded close to the edges of the DCB, whereas it was bonded in the center for all other TVs. As a consequence, when comparing TV2, 3 and 4, we can consider that the effect of the silver on the total R<sub>th</sub> is negligible, even if the silver joints were obtained for very different process parameters.

A thermal dissipation simulation was made with ANSYS multiphysics software. The junction temperature obtained by simulation is close to the experimental test. To simulate the junction temperature evolution, we used the ambient temperature and power dissipation we already obtained from the experimental test as inputs. We can see in Figure 9 and Figure 10 two simulation results obtained for two different locations of the chip (on the edge, as with TV1, and on the center of the substrate, as with all other TVs).

Using the simulation tool, we were able to confirm that the TIM layer is the main component of the total R<sub>th</sub> (Figure 11). The simulation also showed that the location of the chip is much more important than the silver joint thickness (Figure 12).



**Figure 9:** Heat dissipation of the test vehicle 1 with a 50 μm silver joint thickness and 6.29 Watts power dissipation in the chip and the double sided thermal adhesive properties. (Corresponding to the first line in Table 4)



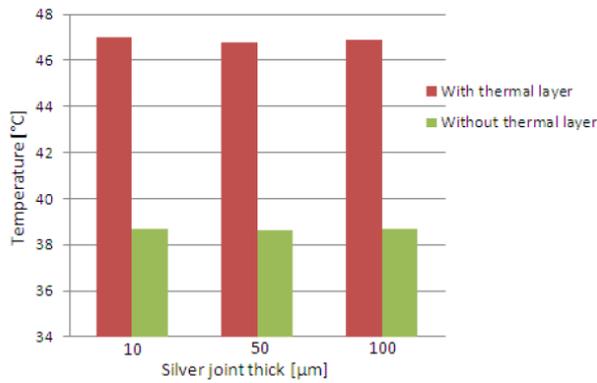
**Figure 10:** Heat dissipation of the test vehicle 2 with a 50 microns silver joint thickness and 6.29 Watts power dissipation in the chip localised in the middle of the DCB substrate and the double sided thermal adhesive properties.

## 3 Thermal stability of the sintered silver

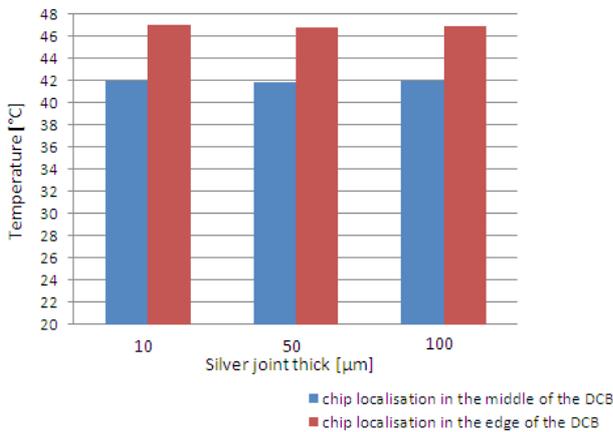
### 3.1 Description of the issue

Although sintered silver is a very attractive material for high temperature applications, due to its very high melting point, some authors have highlighted the risk of silver migration [8,9,10].

This phenomenon is the migration of silver ions from the anode to the cathode causing the formation of a conductive dendrite (Figure 13). This is an area where the random presence of silver can cause a short circuit between the electrodes. In particular, this was demonstrated in the case of silver electrodes on a ceramic substrate [10].



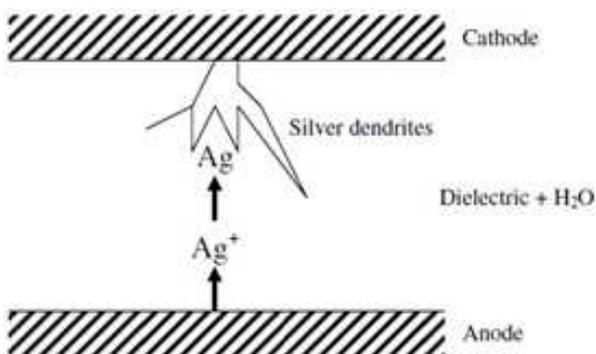
**Figure 11** Power dissipation of 6.29 Watts in the chip which is located in the edge of the DCB substrate



**Figure 12:** The junction temperature is influenced by the location of the chip on the DCB substrate

If we define the lifetime of a sample as the operating time before the short circuit appears [10], this lifetime is sensitive to three parameters :

- An increase in the electric field applied to the sample decreases his lifetime. Tests conducted by Yunhui Mei et al. showed that migration occurred at electric fields as low as 10 V/mm, with a strong reduction in lifetime for fields reaching 100 V/mm.
- The lifetime of the sample decreases with increasing temperature. In the same way as for the potential, Yunhui et al. investigated the effect of temperature from 250 to 400°C. Silver



**Figure 13:** Classical process of silver migration [9]

migration was observed for all temperature, with lifetime following an Arrhenius law.

- The lifetime of the sample decreases with increasing oxygen partial pressure. Oxygen is shown to be required for the migration to occur [10].

The results presented in the literature use electrodes entirely made out of silver. In the case of our system, silver is only used as the die-attach material. Therefore, there is a need to assess the risk of silver migration in this case.

### 3.2 Description of the test vehicle

Three sets of test vehicles have been built:

- a set has been etched in DCB, with the copper metallization left as is (no plating applied to the copper), using the layout visible in Figure 14. A 3x3 mm<sup>2</sup> silver pad (heraeus material) has then been screen-printed on the copper, and sintered without pressure during sintering nor die on top of the silver deposit.
- another identical, but with a nickel/gold finish on top of the copper, to prevent oxidation
- the last set was obtained by screen-printing silver paste on an alumina substrate (Figure 15).



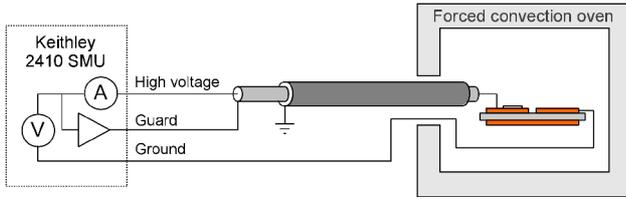
**Figure 14:** The test vehicle etched in a DCB substrate with a nickel finish (before gold plating). The gap between electrodes is 2 mm, and the sample size is 34x10 mm<sup>2</sup>.



**Figure 15:** Image of the screen-printed silver electrodes after sintering, with a 2 mm gap.

### 3.3 Operating mode

The test vehicles are connected to a high-voltage Source and Measure Unit (SMU Keithley 2410). This equipment can source up to 1100V, and measure current with a resolution of 10 pA. Care has been taken in the connexion to avoid current leakage. In particular, we used a triaxial cable for the high potential (Figure 16). The cable is connected to the test vehicle using HMP (High



**Figure 16:** Schematic description of the silver migration test bench. A garded measurement is used to prevent current leakage in the interconnections.

Melting Point, lead based) solder, with a ring of kapton adhesive to improve the mechanical strength.

The test vehicle is placed in a forced-convection oven, at an ambient temperature of 300°C. Such a high temperature made the use of standard triax cable impossible. In consequence, we built a high-temperature triax cable by using a high-temperature coax (Omerin Siliflam THS1200) shielded with a copper braid. As a result, the leakage current is found to be around 70 pA at 300°C.

During the test, a voltage bias of 1100 V is applied to the test vehicles using the SMU.

### 3.4 Results and discussion

The results are summarized in Table 5. It can be seen that the leakage current measurements vary widely between test vehicles (from 186.6 to 1.7 nA). This is probably due to the sample preparation: for both DCB test vehicles, the electrodes were etched in the copper layer of a plain DCB board. Any residual copper left after the etching step would increase the leakage current.

However, for a given test vehicle, we found no evidence of silver migration: the leakage current only changed by a few nano-amperes, over periods reaching 10 days.

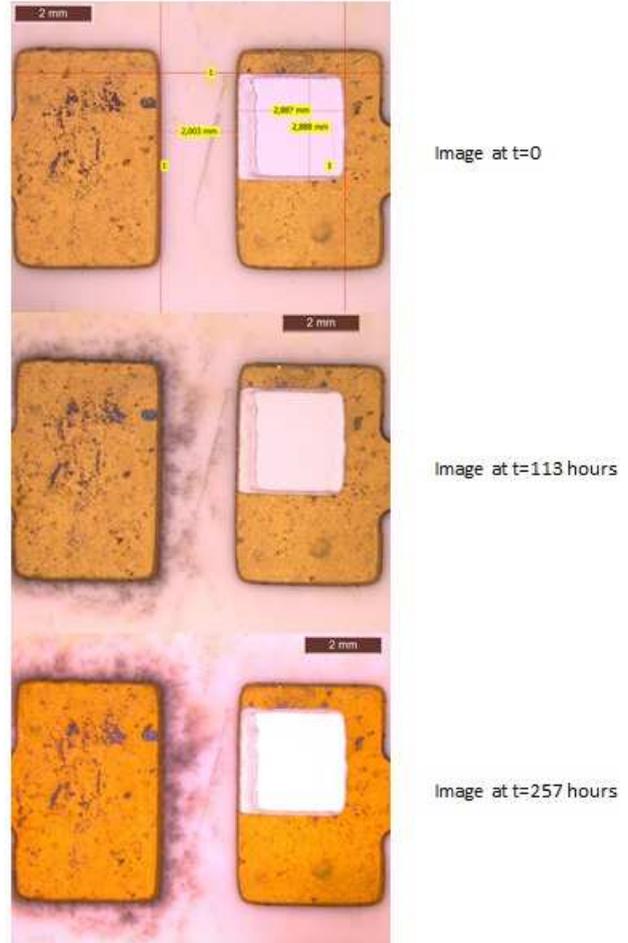
For the bare-copper sample, the tests were stopped after a few days, as we suspected that the oxide layer that formed over the copper would form an electrical insulation.

For the gold-plated test vehicle, although no silver dendrite can be observed, it must be noticed that a black deposit developed around the cathode (Figure 17). The composition of this deposit is unknown, but it has no effect on the leakage current (Table 5). Investigation is ongoing to determine its nature.

In order to have an estimation of the electrical field experienced by the silver deposit on the DCB test vehicles, a finite-elements simulation has been performed (Figure 18). It shows that the copper electrodes provide a shielding effect, with an electrical field decreasing rapidly a few hundreds of microns away from the gap. However, for a silver deposit located as close to the gap as in Figure

17, the silver deposit experiences electrical fields in excess of 1 kV/mm (Figure 18). This is much more intense than studied in [10] and should result in the migration of silver particles.

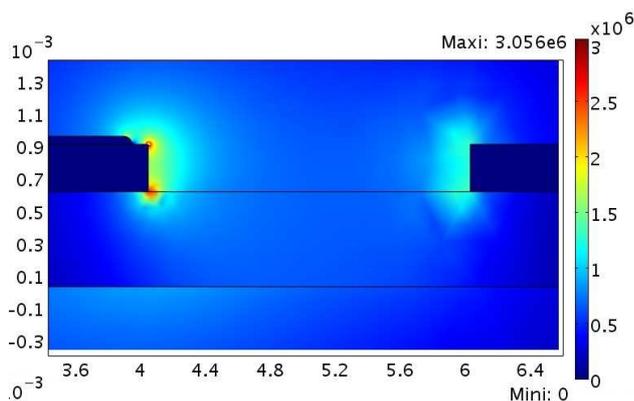
Regarding the screen-printed silver test vehicle, no migration has been detected yet. This is surprising, as the model proposed in [10] would predict a lifetime of 8 hours in this configuration (2 mm gap between electrodes, 550 V/m electrical field).



**Figure 17:** Pictures of the inter-electrodes space, for the gold-plated sample, after 0, 113 and 257 h at 300°C. The clear square corresponds to the silver deposit. The apparent change in color for the gold is due to the camera settings, and is not an actual change. A black deposit formed around the cathode (left electrode) during the test.

Test vehicle	Initial	1 day	3 days	10 days	Remark
DCB/bare copper	186.6	180.0	160.0		Test stopped due to copper oxidation
DCB Ni/Au plating	15.8		9.8	9.8	
Screen-printed Silver	1.7	2.4	2.3		Test ongoing

**Table 5:** Leakage current measured on the test vehicles with time, for a 1100 V bias and 300°C ambient temperature. Current values are expressed in nano-amperes.



**Figure 18:** 2-D Simulation (Comsol Multiphysics) of the electrical field experienced by the test vehicle (Figure 14), with a 2 mm gap. The picture represents two copper conductors (dark blue), one with the silver deposit (left), on an alumina substrate, in air.

## 4 Conclusion

For the study of the thermal resistance, and although die attaches were sintered in very different conditions, no difference could be demonstrated among the silver joints. This proves that the silver sintering technology produces die-attaches with excellent thermal performances, well above that of the TIM layers or of the alumina substrate. New test vehicles are being assembled to follow the thermal resistance evolution during thermal cycling ageing.

No evidence of silver migration was found, which is in contradiction with the results available in the literature. This is surprising, and further investigations are needed. Future tests will include test vehicles with a narrower gap, to increase the electrical field and reduce the dendrite length required to produce a short circuit. This will constitute a worst-case configuration that will help proving (or disproving) the risk of silver migration. In any case, the present results show that power modules should be able to operate for relatively long periods of time at milder temperatures (up to 200°C) without any risk of silver migration.

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