# Low Complexity Frequency Domain Hybrid–ARQ Chase Combining for Broadband MIMO CDMA Systems

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**Abstract**

In this paper, we consider high-speed wireless packet access using code division multiple access (CDMA) and multiple-input–multiple-output (MIMO). Current wireless standards, such as high speed packet access (HSPA), have adopted multi-code transmission and hybrid–automatic repeat request (ARQ) as major technologies for delivering high data rates. The key technique in hybrid–ARQ, is that erroneous data packets are kept in the receiver to detect/decode retransmitted ones. This strategy is refereed to as *packet combining*. In CDMA MIMO-based wireless packet access, multi-code transmission suffers from severe performance degradation due to the loss of code orthogonality caused by both interchip interference (ICI) and co-antenna interference (CAI). This limitation results in large transmission delays when an ARQ mechanism is used in the link layer. In this paper, we investigate efficient minimum mean square error (MMSE) frequency domain equalization (FDE)-based iterative (turbo) packet combining for cyclic prefix (CP)-CDMA MIMO with Chase-type ARQ. We introduce two turbo packet combining schemes: i) In the first scheme, namely *"chip-level turbo packet combining"*, MMSE FDE and packet combining are jointly performed at the chip-level. ii) In the second scheme, namely *"symbol-level turbo packet combining"*, chip-level MMSE FDE and despreading are separately carried out for each transmission, then packet combining is performed at the level of the soft demapper. The computational complexity and memory requirements of both techniques are quite insensitive to the ARQ delay, i.e., maximum number of ARQ rounds. The throughput is evaluated for some

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representative antenna configurations and load factors (i.e., number of orthogonal codes with respect to the spreading factor) to show the gains offered by the proposed techniques.

**Index Terms**

Code division multiple access (CDMA), multi-code transmission, broadband multiple-input–multiple-output (MIMO), automatic repeat request (ARQ), packet combining, frequency domain methods.

## I. Introduction

Space-time (ST) multiplexing oriented multiple-input–multiple-output (MIMO) and hybrid–automatic repeat request (ARQ) are two core technologies used in the emerging code division multiple access (CDMA)-based wireless packet access standards [1]. In ST multiplexing architectures, independent data streams are sent over multiple antennas to increase the transmission rate [2]. In hybrid–ARQ, erroneous data packets are kept in the receiver to help decode the retransmitted packet, using *packet combining* techniques (e.g. see [3] and references therein).

To support heterogeneous data rates in CDMA systems, multiple spreading codes can simultaneously be allocated to the same user if he requests a high data rate [4]. This method is often refereed to as "*multi-code transmission,*" and has been considered in the high speed packet access (HSPA) system [5]. In MIMO CDMA systems, multi-code transmission offers a spectrum efficiency that linearly increases in the order of the number of spreading codes and transmit antennas. This is achieved by assigning the same spreading code group to all transmit antennas. However, in severe frequency selective fading wireless channels, the performance of this scheme can dramatically deteriorate due to co-antenna interference (CAI) and inter-chip interference (ICI). This results in a large delay (due to multiple transmissions) when an ARQ protocol is used in the link layer. Motivated by this limitation, we investigate efficient hybrid–ARQ receiver schemes that allow to reduce the number of ARQ rounds required to correctly decode a data packet in MIMO CDMA ARQ systems with multi-code transmission.

Recently, cyclic-prefix (CP) aided single carrier (SC) CDMA transmission with chip-level minimum mean square error (MMSE)-based frequency domain equalization (FDE) has been introduced [6]. It is a transceiver scheme that allows to achieve attractive performance with affordable computational complexity cost. Turbo MMSE-FDE for CP-CDMA has then been proposed to cope with severe ICI [7]. In [8], MMSE FDE has been applied to perform packet combining for multi-code CP-CDMA

systems with ARQ operating over severe frequency selective fading channels. It has recently been demonstrated that ARQ presents an important source of diversity in MIMO systems [9]. Interestingly, it has been shown in [9] that for both short and long-term static [1] ARQ channel dynamics, multiple transmissions improve the diversity order of the corresponding MIMO ARQ channel. The case of block-fading MIMO ARQ, i.e., multiple fading blocks are observed within the same ARQ round, has been reported in [10]. Information rates and turbo MMSE packet combining strategies for frequency selective fading MIMO ARQ channel have been investigated in [11]. Turbo MMSE packet combining for broadband MIMO ARQ systems with co-channel interference (CCI) has recently been reported in [12] and [13] using time and frequency domain combining methods, respectively.

In this paper, we consider Chase-type ARQ with multi-code CP-CDMA MIMO transmission [2] over broadband wireless channel. We propose two iterative (turbo) packet combining schemes where, at each ARQ round, the data packet is decoded by iteratively exchanging soft information in the form of log-likelihood ratios (LLRs) between the soft-input–soft-output (SISO) packet combiner and the SISO decoder. In the first turbo packet combining scheme, we exploit the fact that both the CP chip-word and data packet are retransmitted at each ARQ round. This allows us to view each transmission as a group of virtual receive antennas, and build up a virtual MIMO channel that takes into account both multi-antenna and multi-round transmission. We therefore perform combining of multiple transmissions jointly with chip-level soft MMSE FDE. This scheme is called *chip-level packet combining*. In the second scheme, both chip-level soft MMSE FDE and despreading are separately carried out for each transmission. Combining is then performed at the level of the soft symbol demapper. We analyze both the computational complexity and memory required by the proposed techniques, and show that they are less sensitive to the ARQ delay, i.e., maximum number of ARQ rounds. Finally, we evaluate and compare the throughput performance of the proposed schemes for some representative load factors (i.e., number of parallel codes with respect to the spreading factor) and antenna configurations.

Throughout this paper, $(.)^{\top}$ and $(.)^{\mathrm{H}}$ denote the transpose and transpose conjugate of the argument, respectively. $\mathrm{diag}\left\{\mathbf{x}\right\} \in \mathbb{C}^{n\times n}$ and $\mathrm{diag}\left\{\mathbf{X}_1,\cdots,\mathbf{X}_m\right\} \in \mathbb{C}^{mn_1\times mn_2}$ denote the diagonal matrix and block diagonal matrix constructed from $\mathbf{x} \in \mathbb{C}^n$ and $\mathbf{X}_1,\cdots,\mathbf{X}_m \in \mathbb{C}^{n_1\times n_2}$, respectively. For $\mathbf{x} \in$

[1]The short-term static ARQ channel dynamic corresponds to the case where two consecutive ARQ rounds observe independent channel realizations. In long-term static channels, all ARQ rounds corresponding to the same data packet observe the same channel realization.

[2]In this MIMO CDMA ARQ transmission scheme, the chip packet is completely retransmitted at each ARQ round.

$\mathbb{C}^{TN}$, $\mathbf{x}_f$ denotes the discrete Fourier transform (DFT) of $\mathbf{x}$, i.e. $\mathbf{x}_f = \mathbf{U}_{T,N}\mathbf{x}$, with $\mathbf{U}_{T,N} = \mathbf{U}_T \otimes \mathbf{I}_N$, where $\mathbf{I}_N$ is the $N \times N$ identity matrix, $\mathbf{U}_T$ is a unitary $T \times T$ matrix whose $(m,n)$th element is $(\mathbf{U}_T)_{m,n} = \frac{1}{\sqrt{T}} e^{-j(2\pi mn/T)}$, $j = \sqrt{-1}$, and $\otimes$ denotes the Kronecker product. The rest of this paper has the following structure. In Section II, we present the CP-CDMA MIMO ARQ transmission scheme then provide its corresponding communication model. In Section III, we derive the two iterative soft MMSE FDE-aided packet combining schemes we propose in this paper. Section IV, analyzes the complexity and memory size required by both schemes, then focuses on the comparison of their throughput performances. The paper is concluded in Section V.

## II. System Description

### A. CP-CDMA MIMO ARQ Transmission Scheme

We consider a single user multi-code CP-CDMA transmission scheme over a broadband MIMO channel with an ARQ protocol in the upper layer, where the ARQ delay is $K$ (index $k = 1, \cdots, K$). An information block is first encoded using a $\rho$-rate encoder, then interleaved with the aid of a semi-random interleaver $\Pi$, and spatially multiplexed over $N_T$ transmit antennas (index $t = 1, \cdots, N_T$) to produce the coded and interleaved frame $\boldsymbol{b}$ which is *serial-to-parallel* converted to $N_T$ sub-streams $\boldsymbol{b}_1, \ldots, \boldsymbol{b}_{N_T}$ , where

$$\mathbf{b}_t \triangleq [b_{t,0,1}, \cdots, b_{t,j,m}, \cdots, b_{t,T_s-1,M}] \in \{0,1\}^{MT_S}. \tag{1}$$

$T_s$ denotes the length of the symbol block transmitted over each antenna (index $j = 0, \cdots, T_s - 1$). Each sub-stream is then symbol mapped onto the elements of constellation $\mathcal{S}$ where $|\mathcal{S}| = 2^M$. For each antenna, the symbol block is passed through a *serial-to-parallel* converter and a spreading module which consists in $C$ orthogonal codes. The same spreading matrix

$$\mathbf{W} \triangleq \left[\mathbf{w}_1^\top, \cdots, \mathbf{w}_C^\top\right] \in \left\{\pm 1/\sqrt{N}\right\}^{N \times C} \tag{2}$$

is used for each transmit antenna, where

$$\mathbf{w}_n \triangleq [w_{1,n}, \cdots, w_{N,n}], \ n = 1, \cdots, C, \tag{3}$$

is a Walsh code of length $N$ (i.e., spreading factor), and $C \leq N$ is the number of multiplexed codes. The rate of this space-time code (STC) is therefore

$$R = \rho M N_T C. \tag{4}$$

The $C$ parallel chip-streams on each antenna are then added together to construct a block of $T_c = T_s\frac{N}{C}$ chips (index $i = 0, \cdots, T_c - 1$). The chips at the output of the $N_T$ transmit antennas are arranged in the $N_T \times T_c$ matrix

$$\mathbf{X} \triangleq \begin{bmatrix} x_{1,0} & \cdots & x_{1,T_c-1} \\ \vdots & & \vdots \\ \underbrace{x_{N_T,0}}_{\mathbf{x}_0} & \cdots & \underbrace{x_{N_T,T_c-1}}_{\mathbf{x}_{T_c-1}} \end{bmatrix}, \tag{5}$$

where

$$x_{t,i} \triangleq \sum_{n=1}^{C} s_{t,n,i} w_{p,n}, \quad p = i \bmod N + 1, \tag{6}$$

and $s_{t,n,i}$ denotes the symbol transmitted by antenna $t$ at channel use (c.u) $i$ using Walsh code $\mathbf{w}_n$. Transmitted chips are independent (infinitely deep interleaving assumption), and the chip energy is normalized to one, i.e., $\mathbb{E}\left[|x_{t,i}|^2\right] = 1$ . A CP chip-word of length $T_{CP}$ is appended to $\mathbf{X}$ to construct the $N_T \times (T_c + T_{CP})$ chip matrix $\mathbf{X}'$ to be transmitted. We consider Chase-type ARQ: When the decoding outcome is erroneous at ARQ round $k$, the receiver feeds back a negative acknowledgment (NACK) message, then the transmitter completely retransmits chip-matrix $\mathbf{X}'$ in the next round. A successful decoding incurs the feed back of a positive acknowledgment (ACK) message. The transmitter then stops the transmission of the current frame and moves on to the next frame. Fig. 1 depicts the considered CP-CDMA MIMO transmission scheme with ACK/NACK.

### *B. Communication Model*

The broadband MIMO propagation channel connecting the $N_T$ transmit and the $N_R$ receive antennas is composed of $L$ chip-spaced taps (index $l = 0, \cdots, L-1$). We assume a quasi-static block fading channel, i.e., the channel is constant over an information block and independently changes from block to block. The $N_R \times N_T$ channel matrix characterizing the $l$th discrete tap at ARQ round $k$ is denoted $\mathbf{H}_l^{(k)}$, and is made of zero-mean circularly symmetric complex Gaussian random entries. The average channel energy per receive antenna is normalized as

$$\sum_{l=0}^{L-1}\sum_{t=1}^{N_T} \mathbb{E}\left[\left|h_{r,t,l}^{(k)}\right|^2\right] = N_T, \ r = 1, \cdots, N_R, \tag{7}$$

where $h_{r,t,l}^{(k)}$ is the $(r,t)$th element of $\mathbf{H}_l^{(k)}$.

At the receiver side, after removing the CP-word at ARQ round $k$, a DFT is applied on received signals. This yields $T_c$ frequency domain components grouped in block

$$\mathbf{y}_f^{(k)} \triangleq \left[\mathbf{y}_{f_0}^{(k)^\top}, \cdots, \mathbf{y}_{f_{T_c-1}}^{(k)^\top}\right]^\top, \tag{8}$$

which can be expressed as,

$$\mathbf{y}_f^{(k)} = \mathbf{\Lambda}^{(k)}\mathbf{x}_f + \mathbf{n}_f^{(k)}, \tag{9}$$

where vectors

$$\mathbf{x}_f \triangleq \left[\mathbf{x}_{f_0}^\top, \cdots, \mathbf{x}_{f_{T_c-1}}^\top\right]^\top \in \mathbb{C}^{T_c N_T \times 1}, \tag{10}$$

$$\mathbf{n}_f^{(k)} \triangleq \left[\mathbf{n}_{f_0}^{(k)^\top}, \cdots, \mathbf{n}_{f_{T_c-1}}^{(k)^\top}\right]^\top, \tag{11}$$

group the DFTs of transmitted chips and thermal noise at round $k$, respectively, and $\mathbf{n}_f^{(k)} \sim \mathcal{N}(\mathbf{0}, \sigma^2\mathbf{I}_{T_c N_R})$. The channel frequency response (CFR) matrix $\mathbf{\Lambda}^{(k)}$ at ARQ round $k$ is given by

$$\begin{cases} \mathbf{\Lambda}^{(k)} \triangleq \operatorname{diag}\left\{\mathbf{\Lambda}_0^{(k)}, \cdots, \mathbf{\Lambda}_{T_c-1}^{(k)}\right\}, \\ \mathbf{\Lambda}_i^{(k)} = \sum_{l=0}^{L-1} \mathbf{H}_l^{(k)} e^{-j(2\pi i l/T_c)}. \end{cases} \tag{12}$$

## III. Iterative Receivers for CP-CDMA MIMO ARQ

In this section, we present two efficient algorithms for performing turbo packet combining for CP-CDMA MIMO ARQ systems : i) chip-level turbo packet combining, and ii) symbol-level turbo packet combining. In both schemes, signals received in multiple ARQ rounds are processed using soft MMSE FDE. Transmitted data blocks are decoded, at each ARQ round, in an iterative fashion through the exchange of soft information, in the form of LLR values, between the soft packet combiner, i.e., soft–over ARQ rounds equalizer and demapper, and SISO decoder.

### *A. Chip-Level Turbo Packet Combining*

To exploit the diversity available in received signals $\mathbf{y}_{f_0}^{(1)}, \cdots, \mathbf{y}_{f_{T_c-1}}^{(k)}$, we view each ARQ round $k$ as an additional group of virtual $N_R$ receive antennas. The MIMO ARQ system can therefore be considered as a point-to-point MIMO link with $N_T$ transmit and $kN_R$ receive antennas, where the $T_c k N_R \times 1$ chip-level virtual received signal vector $\underline{\mathbf{y}}_f^{(k)}$ is constructed as,

$$\underline{\mathbf{y}}_f^{(k)} \triangleq \left[\mathbf{y}_{f_0}^{(1)^\top}, \cdots, \mathbf{y}_{f_0}^{(k)^\top}, \cdots, \mathbf{y}_{f_{T_c-1}}^{(1)^\top}, \cdots, \mathbf{y}_{f_{T_c-1}}^{(k)^\top}\right]^\top. \tag{13}$$

The frequency domain communication model after $k$ rounds is then given as,

$$\underline{\mathbf{y}}_f^{(k)} = \underline{\mathbf{\Lambda}}^{(k)}\mathbf{x}_f + \underline{\mathbf{n}}_f^{(k)}, \tag{14}$$

where

$$\underline{\mathbf{\Lambda}}^{(k)} \triangleq \mathrm{diag}\left\{\begin{bmatrix}\mathbf{\Lambda}_0^{(1)}\\ \vdots \\ \mathbf{\Lambda}_0^{(k)}\end{bmatrix}, \cdots, \begin{bmatrix}\mathbf{\Lambda}_{T_c-1}^{(1)}\\ \vdots \\ \mathbf{\Lambda}_{T_c-1}^{(k)}\end{bmatrix}\right\} \in \mathbb{C}^{T_c k N_R \times T_c N_T}, \tag{15}$$

and

$$\underline{\mathbf{n}}_f^{(k)} = \left[\mathbf{n}_{f_0}^{(1)^\top}, \cdots, \mathbf{n}_{f_0}^{(k)^\top}, \cdots, \mathbf{n}_{f_{T_c-1}}^{(1)^\top}, \cdots, \mathbf{n}_{f_{T_c-1}}^{(k)^\top}\right]^\top. \tag{16}$$

Soft ICI cancellation and frequency domain MMSE filtering are jointly performed over all ARQ rounds. We call this concept "*chip-level turbo packet combining*". This requires a huge computational cost since the complexity of computing MMSE filters is cubic in the order of the ARQ delay. In addition, the required receiver memory size linearly scales with the ARQ delay because all CFRs $\mathbf{\Lambda}_0^{(1)}, \cdots, \mathbf{\Lambda}_{T_c-1}^{(k)}$ are required at round $k$ [14]. In the following, we introduce an efficient turbo MMSE implementation algorithm for chip-level combining where both receiver complexity and memory requirements are quite insensitive to the ARQ delay.

Let $\tilde{\mathbf{x}}$ and $\sigma_{t,i}^2$ denote the conditional mean and variance of $\mathbf{x}$ and $x_{t,i}$, respectively. Soft MMSE processing can be written in a compact forward-backward filtering structure as in [15]. By using the matrix inversion lemma [16], we can express soft MMSE chip-level packet combining at round $k$ as,

$$\mathbf{z}_f^{(k)} = \mathbf{\Gamma}^{(k)}\tilde{\underline{\mathbf{y}}}_f^{(k)} - \mathbf{\Omega}^{(k)}\tilde{\mathbf{x}}_f, \tag{17}$$

where $\mathbf{\Gamma}^{(k)} = \mathrm{diag}\left\{\mathbf{\Gamma}_0^{(k)}, \cdots, \mathbf{\Gamma}_{T_c-1}^{(k)}\right\} \in \mathbb{C}^{T_c N_T \times T_c N_T}$, and $\mathbf{\Omega}^{(k)} = \mathrm{diag}\left\{\mathbf{\Omega}_0^{(k)}, \cdots, \mathbf{\Omega}_{T_c-1}^{(k)}\right\} \in \mathbb{C}^{T_c N_T \times T_c N_T}$ denote the forward and backward filters at round $k$, respectively, and are given by,

$$\begin{cases} \mathbf{\Gamma}_i^{(k)} \triangleq \frac{1}{\sigma^2}\left\{\mathbf{I}_{N_T} - \underline{\mathbf{D}}_i^{(k)}\mathbf{C}_i^{(k)^{-1}}\right\}, \\ \mathbf{C}_i^{(k)} = \sigma^2\tilde{\mathbf{\Xi}}^{-1} + \underline{\mathbf{D}}_i^{(k)}, \end{cases} \tag{18}$$

$$\begin{cases} \mathbf{\Omega}_i^{(k)} \triangleq \mathbf{\Gamma}_i^{(k)} \underline{\mathbf{D}}_i^{(k)} - \mathbf{\Upsilon}^{(k)}, \\ \mathbf{\Upsilon}^{(k)} = \frac{1}{T} \sum_{i=0}^{T-1} \mathbf{\Gamma}_i^{(k)} \underline{\mathbf{D}}_i^{(k)}. \end{cases} \tag{19}$$

$\tilde{\mathbf{\Xi}}$ is the $N_T \times N_T$ unconditional covariance of transmitted chips, and is computed as the time average of conditional covariance matrices $\mathbf{\Xi}_i \triangleq \text{diag}\left\{\sigma_{1,i}^2, \cdots, \sigma_{N_T,i}^2\right\}$. Variables $\underline{\tilde{\mathbf{y}}}_f^{(k)}$ and $\underline{\mathbf{D}}_i^{(k)}$ are computed according to the following recursions,

$$\begin{cases} \underline{\tilde{\mathbf{y}}}_f^{(k)} = \underline{\tilde{\mathbf{y}}}_f^{(k-1)} + \mathbf{\Lambda}^{(k)^H} \mathbf{y}_f^{(k)}, \\ \underline{\tilde{\mathbf{y}}}_f^{(0)} = \mathbf{0}_{T_c N_T \times 1}, \end{cases} \tag{20}$$

$$\begin{cases} \underline{\mathbf{D}}_i^{(k)} = \underline{\mathbf{D}}_i^{(k-1)} + \mathbf{\Lambda}_i^{(k)^H} \mathbf{\Lambda}_i^{(k)}, \\ \underline{\mathbf{D}}_i^{(0)} = \mathbf{0}_{N_T \times N_T}. \end{cases} \tag{21}$$

Note that recursions (20) and (21) present an important ingredient in the proposed chip-level combining algorithm since both complexity and memory requirements become less sensitive to the ARQ delay. These issues are discussed in detail in Section IV. The inverse DFT (IDFT) is then applied to $\mathbf{z}_f^{(k)}$ to obtain the equalized time domain chip sequence. After despreading, extrinsic LLR value $\phi_{t,j,m}^{(e)}$ corresponding to coded and interleaved bit $b_{t,j,m}$ $\forall\ t, j, m$ is computed as,

$$\phi_{t,j,m}^{(e)} = \log \frac{\sum_{s \in \mathcal{S}_1^m} \exp\left\{ \boldsymbol{\xi}_{t,j}^{(k)}(s) + \sum_{m' \neq m} \phi_{t,j,m'}^{(a)} \lambda_{m'}\{s\} \right\}}{\sum_{s \in \mathcal{S}_0^m} \exp\left\{ \boldsymbol{\xi}_{t,j}^{(k)}(s) + \sum_{m' \neq m} \phi_{t,j,m'}^{(a)} \lambda_{m'}\{s\} \right\}}, \tag{22}$$

where $\boldsymbol{\xi}_{t,j}^{(k)}(s) = \frac{\left| r_{t,j}^{(k)} - g_{t,j}^{(k)} s \right|^2}{\theta_{t,j}^{(k)^2}}$, with $r_{t,j}^{(k)}$, $g_{t,j}^{(k)}$, and $\theta_{t,j}^{(k)^2}$ are the despreading module output, gain, and residual interference variance, respectively. $\phi_{t,j,m'}^{(a)}$ denotes *a-priori* LLR value corresponding to $b_{t,j,m'}$. $\lambda_{m'}\{s\}$ is an operator that allows to extract the $m'$th bit labeling symbol $s \in \mathcal{S}$, and $\mathcal{S}_\beta^m$ is the set of symbols where the $m$th bit is equal to $\beta$, i.e. $\mathcal{S}_\beta^m = \{s : \lambda_m\{s\} = \beta\}$. The obtained extrinsic LLR values are de-interleaved and fed to the SISO decoder. The proposed low complexity algorithm is summarized in Table I.

### B. Symbol-Level Turbo Packet Combining

In this combining scheme, the receiver performs chip-level space-time frequency domain equalization separately for each ARQ round, then combines multiple transmissions at the level of the soft demapper. At each iteration of ARQ round $k$, soft ICI cancellation and MMSE filtering are performed similarly to (17) using communication model (9). Extrinsic information is computed using despreading module outputs corresponding to all ARQ rounds. This requires the inversion of the $k \times k$ covariance matrix of residual interference plus noise. By observing that despreading module outputs obtained at different transmissions are independent, extrinsic LLR value $\phi^{(e)}_{t,j,m}$ corresponding to coded and interleaved bit $b_{t,j,m}$ can be expressed as,

$$\phi^{(e)}_{t,j,m} = \log \frac{\sum\limits_{s \in \mathcal{S}_1^m} \exp\left\{ \overline{\boldsymbol{\xi}}^{(k)}_{t,j}(s) + \sum\limits_{m' \neq m} \phi^{(a)}_{t,j,m'} \lambda_{m'}\{s\} \right\}}{\sum\limits_{s \in \mathcal{S}_0^m} \exp\left\{ \overline{\boldsymbol{\xi}}^{(k)}_{t,j}(s) + \sum\limits_{m' \neq m} \phi^{(a)}_{t,j,m'} \lambda_{m'}\{s\} \right\}}, \tag{23}$$

where $\overline{\boldsymbol{\xi}}^{(k)}_{t,j}(s)$ is recursively computed according to the following recursion,

$$\begin{cases} \overline{\boldsymbol{\xi}}^{(k)}_{t,j}(s) = \overline{\boldsymbol{\xi}}^{(k-1)}_{t,j}(s) + \frac{\left| r^{(k)}_{t,j} - g^{(k)}_{t,j} s \right|^2}{\theta^{(k)^2}_{t,j}}, \\ \overline{\boldsymbol{\xi}}^{(0)}_{t,j}(s) = 0. \end{cases} \tag{24}$$

Note that this recursive implementation relaxes both the complexity and memory requirements. The proposed low complexity algorithm is summarized in Table II.

## IV. Complexity and Performance Analysis

### A. Complexity Evaluation

In this subsection, we briefly analyze both the computational cost and memory requirements of the proposed packet combining schemes. First, note that both algorithms have identical implementations. The only difference comes from steps Table. I. **1.1.**, and Table. II. **1.1.3.** Therefore, both techniques approximately have the same implementation cost. In the following, we focus on the number of arithmetic additions and memory required to perform recursions (20), (21), and (24).

The main idea in the proposed algorithms is to exploit the diversity available in multiple transmissions without explicitly storing required soft channel outputs (i.e., signals and CFRs) or

decisions (i.e., filter outputs), corresponding to all ARQ rounds. This is performed with the aid of recursions (20), (21), and (24), and translates into a memory requirement of $2T_cN_T\left(N_T+1\right)$ and $T_sN_T2^M$ real values for chip-level and symbol-level turbo combining, respectively. Note that in both schemes, the required memory size is insensitive to the ARQ delay. The number of rounds only influences the number of arithmetic additions required in the update procedures corresponding to recursions (20), (21), and (24). At each ARQ round, the chip-level turbo combining algorithm involves $2T_cN_T\left(N_T+1\right)$ arithmetic additions to update $\underline{\tilde{\mathbf{y}}}_f^{(k)}$ and $\underline{\mathbf{D}}_i^{(k)}$. The symbol-level turbo combining scheme requires $T_sN_TN_{\text{iter}}2^M$ arithmetic additions to update $\overline{\boldsymbol{\xi}}_{t,j}^{(k)}(s)$ at each round, where $N_{\text{iter}}$ denotes the number of turbo iterations.

Table III summarizes the maximum number of arithmetic additions and memory size required by both schemes. Note that the number of additions does not have a great impact on receiver computational complexity. The required memory size is the major implementation constraint to take into account when choosing between chip-level and symbol-level combining. In the case of low-order modulations (i.e., $M \leq 2$), symbol-level has less memory requirements than chip-level combining independently of the spreading factor $N$, number of codes $C$, and number of transmit antennas $N_T$. For high-order modulations, (i.e., $M \geq 3$), the required memory size mainly depends on system parameters. For instance, when $M=4$, $N_T=4$, and the system is fully loaded, (i.e., $N=C$), chip-level combining offers less memory requirements than symbol-level combining. When the load factor is reduced to $50\%$, (i.e., $\frac{C}{N}=\frac{1}{2}$), symbol-level becomes more attractive than chip-level.

### *B. Performance Evaluation*

In this subsection, we evaluate the throughput performance of the proposed CP-CDMA MIMO ARQ turbo combining schemes. Following [17], we define the throughput as $\eta \triangleq \frac{\mathbb{E}[\mathcal{R}]}{\mathbb{E}[\mathcal{K}]}$, where $\mathcal{R}$ is a random variable (RV) that takes $R$ when the packet is correctly received or zero when the packet is erroneous after $K$ ARQ rounds. $\mathcal{K}$ is a RV that denotes the number of rounds used for transmitting one data packet. We use Monte Carlo simulations for evaluating $\eta$.

We consider a STC using a $\frac{1}{2}$-rate convolutional encoder with polynomial generators $(35,23)_8$, quadrature phase shift keying (QPSK) modulation, $N_T=2$ transmit antennas, and a spreading factor $N=16$. The length of the code bit frame is $1024$ bits including tails. We evaluate the throughput performance for the following loads: $25\%$ (i.e., $C=4$), $50\%$ (i.e., $C=8$), and $100\%$ (i.e., $C=16$),

which correspond to rates $R = 8$, $R = 16$, and $R = 32$, respectively. The ARQ delay is $K = 3$. The broadband MIMO channel has $L = 10$ chip-spaced equal power taps, and the CP length is $T_{CP} = 10$. The $E_c/N_0$ ratio appearing in all figures is the signal to noise ratio (SNR) per chip per receive antenna. We use Max-Log-maximum *a posteriori* (MAP) for SISO decoding. The number of turbo iterations is set to three. In all scenarios, we consider the matched filter bound (MFB) throughput performance of the corresponding CP-CDMA MIMO ARQ channel to evaluate the ICI cancellation capability achieved by the proposed techniques.

In Fig. 2, we report throughput performance curves for a balanced MIMO configuration, i.e., $N_R = N_T = 2$. We observe that both combining schemes have similar throughput performance for quarter and half loads. In the case of full load, chip-level combining outperforms symbol-level combining in the region of low SNR. For instance, the performance gap is around $0.6$dB at $\eta = 12.5$bit/s/Hz throughput. Also, note that for all configurations, the slopes of the throughput curves of both techniques are asymptotically similar to that of the MFB. Therefore, both combining schemes asymptotically achieve the diversity order of the corresponding CP-CDMA MIMO ARQ channel.

In Fig. 3, we provide throughput curves when only one receive antenna ($N_R = 1$) is used, i.e., unbalanced MIMO configuration. In this scenario, chip-level combining clearly outperforms symbol-level combining for half and full loads. The performance gap is about $3$dB at $\eta = 12.5$bit/s/Hz for a full load configuration. This suggests that chip-level turbo combining can be used for high speed downlink CDMA MIMO systems with high loads. Note that, both techniques fail to achieve the full diversity order in the case of half and full loads.

## V. Conclusions

In this paper, efficient turbo receiver schemes for multi-code CP-CDMA transmission with ARQ operating over broadband MIMO channel were investigated. Two packet combining algorithms were introduced. The chip-level technique performs packet combining jointly with chip-level MMSE FDE. The symbol-level scheme combines multiple transmissions at the level of the soft demapper. We analyzed the complexity and memory size required by both techniques, and showed that, from an implementation point of view, chip-level is more attractive than symbol-level combining for systems with high modulation order and load factor (number of codes with respect to the spreading factor). We also investigated the throughput performance. Simulations demonstrated that both techniques

approximately have similar performance for balanced MIMO configurations. In the case of unbalanced configurations (more transmit than receive antennas), chip-level combining outperforms symbol-level combining especially for full load factors.

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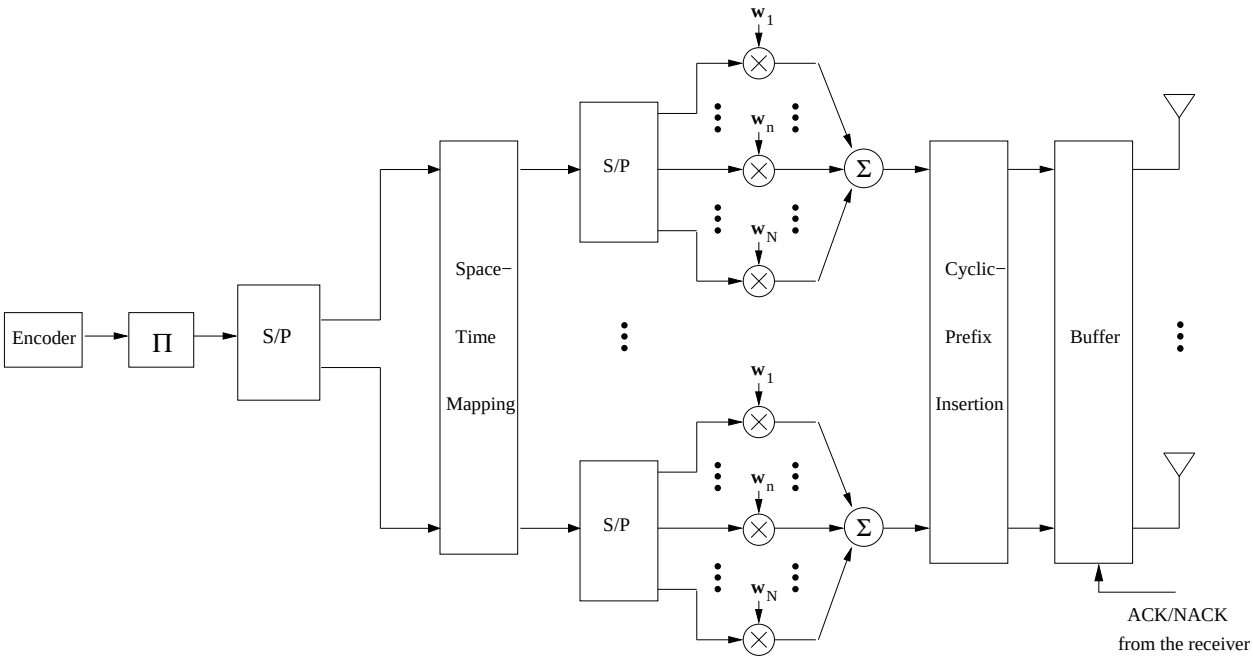


Fig. 1. CP-CDMA MIMO transmission scheme with ACK/NACK.

TABLE I

SUMMARY OF THE CHIP-LEVEL TURBO COMBINING ALGORITHM

**0. Initialization**

Initialize $\underline{\tilde{\mathbf{y}}}_f^{(0)}$ and $\underline{\mathbf{D}}_i^{(0)}$ with $\mathbf{0}_{T_c N_T \times 1}$ and $\mathbf{0}_{N_T \times N_T}$, respectively.

**1. Combining at round** $k$

**1.1.** Update $\underline{\tilde{\mathbf{y}}}_f^{(k)}$ and $\underline{\mathbf{D}}_i^{(k)}$ according to (20) and (21).

**1.2.** At each iteration,

**1.2.1** Compute the forward and backward filters using (18) and (19).

**1.2.2** Compute the MMSE estimate of $\mathbf{x}_f$ using (17).

**1.2.3** Compute extrinsic LLRs $\phi_{t,j,m}^{(e)}$ according to (22).

**1.3.** end **1.2.**

TABLE II

SUMMARY OF THE SYMBOL-LEVEL TURBO COMBINING ALGORITHM

**0. Initialization:**

Initialize $\overline{\boldsymbol{\xi}}_{t,j}^{(0)}(s)$ with $0$.

**1. Combining at round** $k$

**1.1.** At each iteration,

**1.1.1** Compute the forward and backward filters using (18) and (19) with $\underline{\mathbf{D}}_i^{(k)} = {\boldsymbol{\Lambda}_i^{(k)}}^H \boldsymbol{\Lambda}_i^{(k)}$.

**1.1.2** Compute the MMSE estimate on $\mathbf{x}_f$ using (17) and $\underline{\tilde{\mathbf{y}}}_f^{(k)} = {\boldsymbol{\Lambda}^{(k)}}^H \mathbf{y}_f^{(k)}$.

**1.1.3** Update $\overline{\boldsymbol{\xi}}_{t,j}^{(k)}(s)$ according to (24).

**1.1.4** Compute extrinsic LLRs $\phi_{t,j,m}^{(e)}$ using (23).

**1.3.** end **1.1.**

TABLE III

SUMMARY OF THE MAXIMUM NUMBER OF ARITHMETIC ADDITIONS, AND MEMORY SIZE

| | **Chip-Level Combining** | **Symbol-Level Combining** |
|---|---|---|
| **Arithmetic Additions** | $2T_c N_T (K-1)(N_T+1)$ | $T_s N_T (K-1) N_{\text{iter}} 2^M$ |
| **Memory** | $2T_c N_T (N_T+1)$ | $T_s N_T 2^M$ |

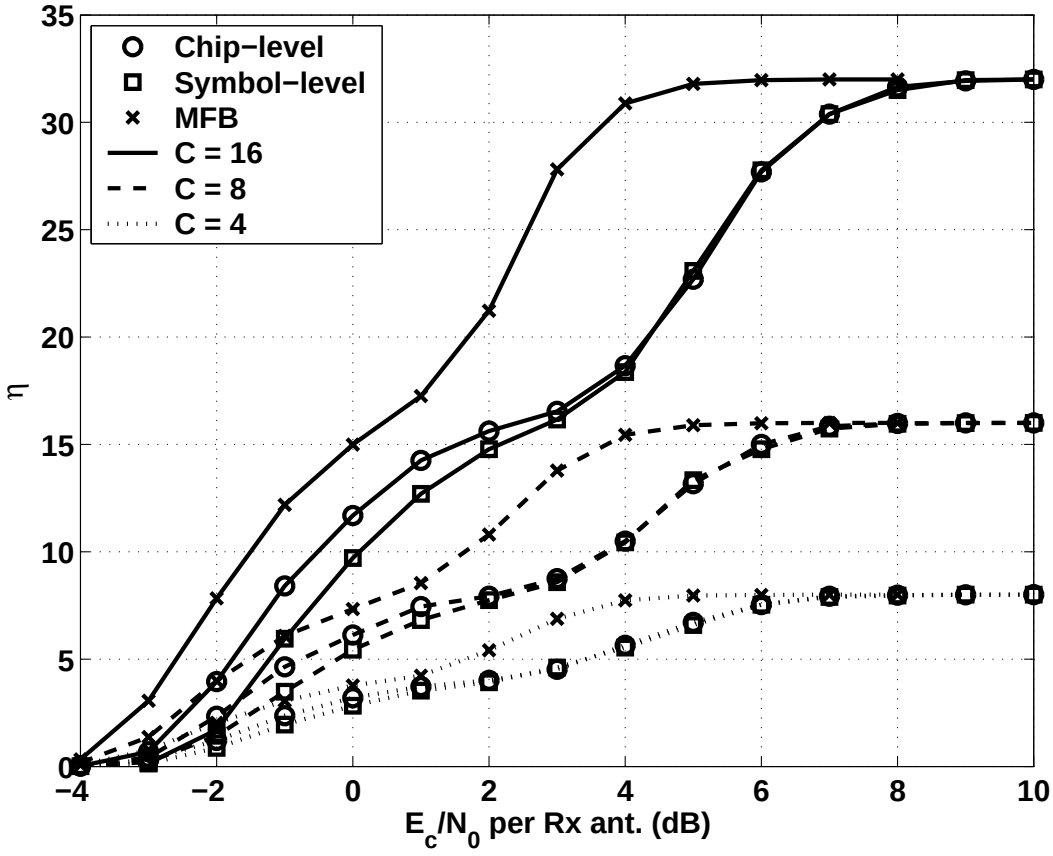


Fig. 2. Throughput performance with $N_T = 2$, $N_R = 2$, $L = 10$ equal power tap profile.

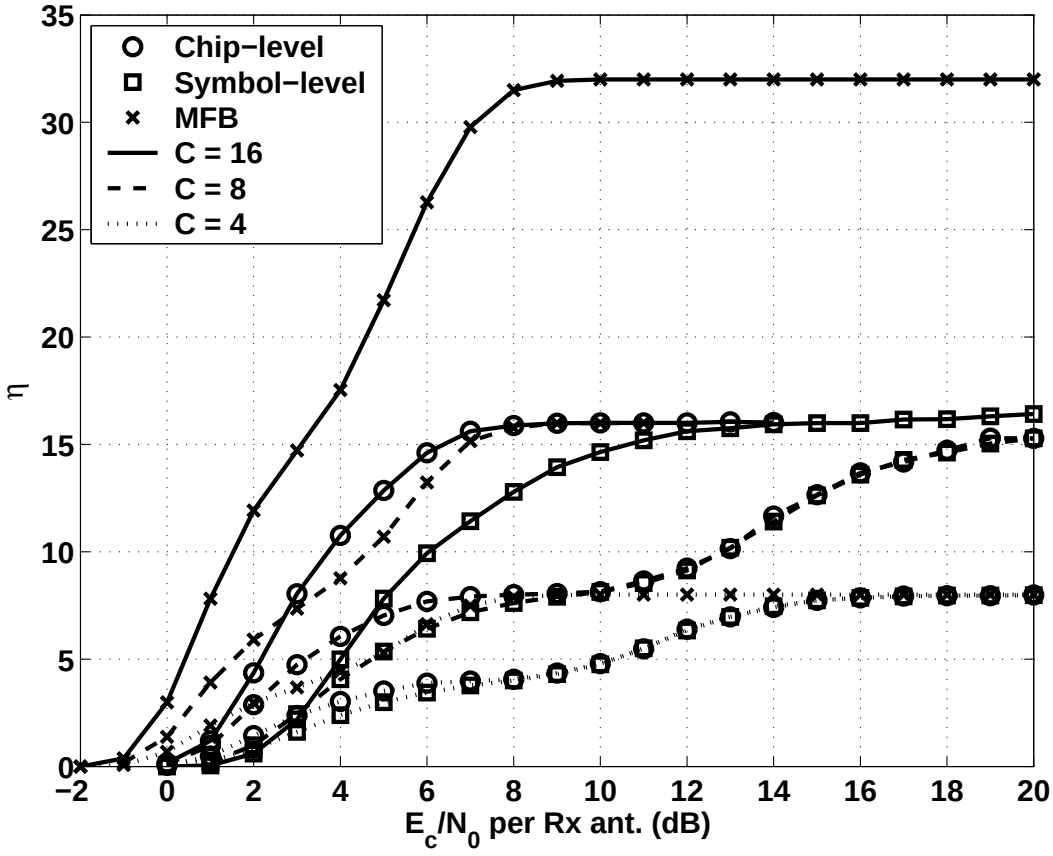


Fig. 3. Throughput performance with $N_T = 2$, $N_R = 1$, $L = 10$ equal power tap profile.