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## Single Phase AC Power Load Profile Emulator

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**Abstract.** This paper deals with the realization and design of a consumption profile emulator intended for the validation of different element energy models of a stand-alone wind and photovoltaic system, associated with electrochemical energy storage [1]. The emulator is designed to vary active power but in the near future it will also be used to load simulation with reactive power. Energy models are then inserted in a sizing optimization algorithm in order to minimize the Global Energy Requirement (GER) of the whole system [2]. Afterwards, we will focus on the emulator power part dimensioning and then its modelling in view of the stand-alone system controlled by an active power reference. Moreover, the digital profile generator is described. The impact on the DC bus capacitor current, caused by the frequency difference between the grid and the inverter, has also been tackled. Finally, experimental results are shown.

### Key words

Electric power, consumption profile emulator, stand-alone system, energy modelling, PWM converter.

### 1. Introduction

The sizing optimization of an electricity production system combined with storage is a very complex issue. Reliable and accurate energy models are required in order to simulate all of the energy flows in the whole system. Therefore, a power consumption profile emulator has been developed to load the system with a predefined consumption profile with the aim of experimentally validating the system's energetic elements and more specifically the storage element one (essential in such a system) [3] which remains the weak point of stand-alone systems.

### 2. Stand-alone system presentation

A diagram of the whole system is detailed on Fig. 1. The electricity is provided by two complementary production systems: a wind generator system with two 750 W nominal power wind turbines connected through power electronic converters to a 48 V DC voltage bus and photovoltaic (PV) generators supplying a maximum electric power of 2 kW. The PV generators are linked with the DC bus by MPPT DC/DC converters. Electrochemical accumulator is 15 kWh lead-acid batteries. Consumer loads are connected to DC bus

through a 4.5 kVA single phase reversible inverter (Xantrex-Trace Engineering).

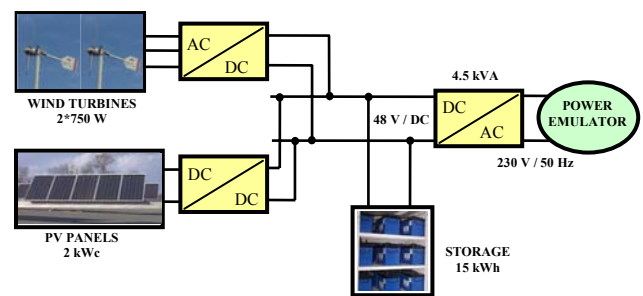


Fig.1. Experimental power production system with consumption profile emulator

### 3. The consumption profile emulator

The role of the emulator is to emulate various power consumption profiles representative of electric energy consumer behaviours. It is connected to the inverter in a stand-alone configuration. The emulator is made of two back-to-back PWM converters using IGBTs semiconductors [4]. For various reasons (flexibility, conservation of energy) we achieved a system able to send the used energy back to the existing grid on the experimental site. The reactive power and current harmonics influence are not concerned at this time, as the emulator absorbed current has to be sinusoidal and in phase with the voltage delivered by the reversible inverter of the system. Therefore, the emulator must be controlled with only an active power reference and thus, load the system with predefined power profile stored in a mass storage memory card (Multi-Media Card: MMC) as depicted on Fig. 2.

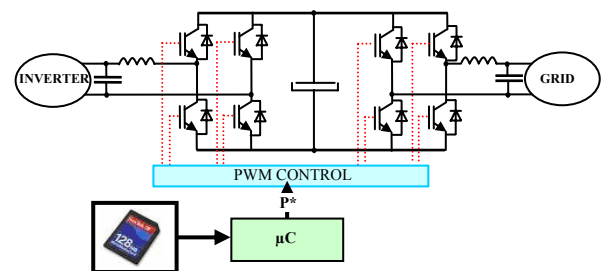


Fig.2. Structure of single phase consumption profile emulator

### 4. Power reference achievement

In order to obtain realistic cycles (see Fig.3) to assess the pertinence of the models, the system will be commanded with an active power reference over several months. The power consumption profile used to control the system can evolve from 0 to 4.5 kW each minute with a 15 W step. The MATLAB software is used to create the appropriate consumption profile. Due to the long duration of the profile, it will be stored in a mass storage memory. Each active power sample corresponds to an 8 bit digital word stored in the memory.

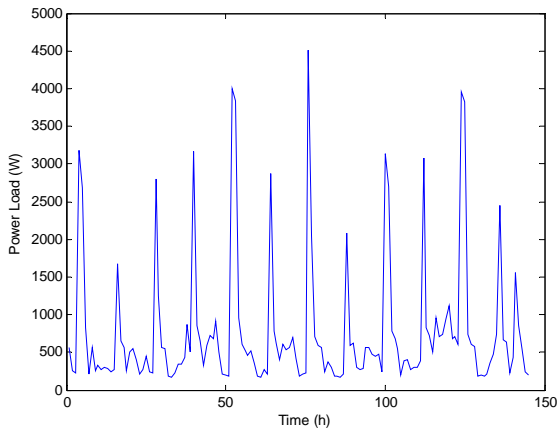


Fig.3. Realistic load cycles

The MMC interacts via a Serial Peripheral Interface bus (SPI) with a microcontroller (ADuc812). The microcontroller is programmed with the high-level language C++. Each minute the microcontroller is looking for the appropriate sample in the memory card. This sample is then converted with a Digital-to-Analog Converter (ADC) to elaborate the active power reference ( $P^*$ ) of the system for the current minute. Then the microcontroller will seek the following 8 bit word in the memory card. The Fig.4 represents the creation of the active power reference.

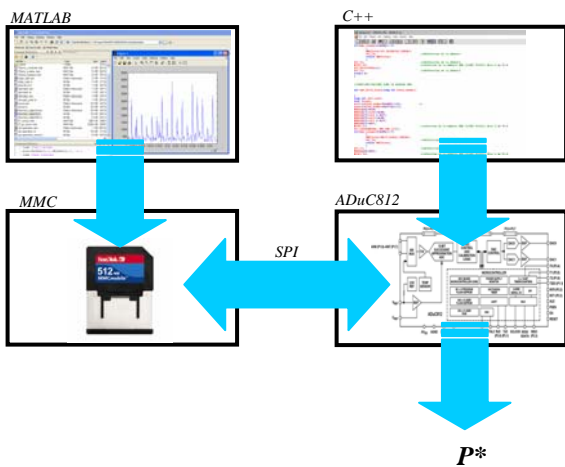


Fig.4: Active power reference achievement

### 5. Modelling and command

Considering the unidirectional power transfers (from the system to the grid) the converter on the inverter side will function as a PWM rectifier while the converter on the grid side will function as a PWM inverter. However, other direction transfer will be possible to simulate battery recharge from grid in grid connected cases.

#### A. System data

The maximum reference power is 4.5 kW which leads to a sine current with 28 A peak value. Maximum voltage value both on inverter and grid side is equal to 325 V. To obtain a good control of the two converters, DC bus voltage is chosen at 400 V. IGBT commutation frequency of the PWM converters ( $f$ ) is set to 15 kHz mainly to minimize inductor size. Fig. 4 shows a photograph of a PWM converter module.

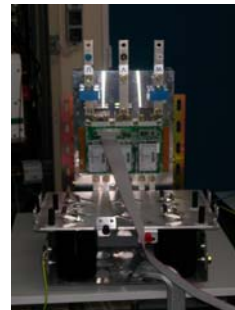


Fig.4. Photograph of one of the two PWM converters (inverter or rectifier)

#### B. Modelling of the PWM converter

The modelling of the two PWM converters is imperative with the perspective of the control of the whole system. The modelling is identical for both PWM converters. The different notations used in this modelling are shown on Fig. 5. Each PWM converter control is based on cascade loop architecture (current internal loop). The current through the inductance must be controlled for both PWM converters.

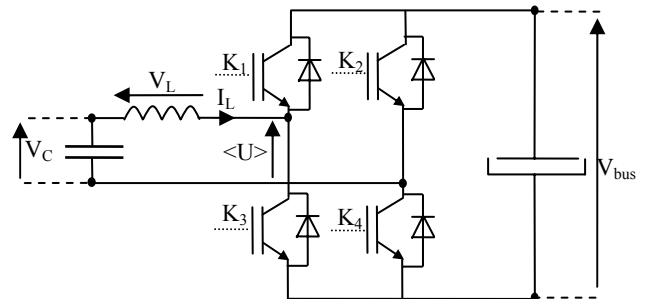


Fig.5. Modelling notations

$V_{BUS}$  is the tension of the DC bus,  $\langle U \rangle$  is the average value on a PWM period,  $I_L$  and  $V_L$  are respectively the current and the tension of the inductance  $L$ .  $V_C$  is the voltage of the capacitor  $C$ . The IGBT transistors are complementary commanded; this means that IGBTs

$K_1$  and  $K_3$  are both conductive at the same time while  $K_2$  and  $K_4$  are not (and vice versa). According to these notations, the following expressions can be found:

$$V_L(t) = V_C(t) - \langle U \rangle \quad (1)$$

$$V_L(t) = L \cdot \frac{dI_L(t)}{dt} + r \cdot I_L(t) \quad (2)$$

Where  $r$  is the parasitic resistance of the inductance  $L$ .

Furthermore the tension  $\langle U \rangle$  is linked with the tension  $V_{CMDE}$  which is in charge of elaborating the PWM commands.

$$\langle U \rangle = V_{CMDE} \cdot G \quad (3)$$

Where  $G$  is a constant gain.

The next diagram (Fig.6) represents the inductance current control in the Laplace space. It has been obtained using equations (1), (2) and (3).

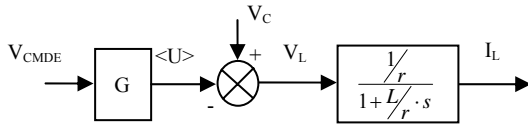


Fig.6. Inductance current control

The inductance current, which is sent back to the grid (for the PWM inverter) and the one which is extracting from the reversible inverter must be sinusoidal at a frequency of 50 Hz, here is the reason why the dynamic of the two current internal loops must be high enough to follow a 50 Hz sinusoidal reference.

Once the converter modelling has been carried out, the independent control of each converter can be envisaged.

C. PWM inverter control

This PWM converter must regulate DC voltage bus to 400 V whilst sending back a sinusoidal current in phase with the sinusoidal voltage grid. The other converter (PWM rectifier) can be modelled by a variable electric resistance dissipating an active power  $P$  under a DC voltage  $V_{bus}$  (Fig.7).

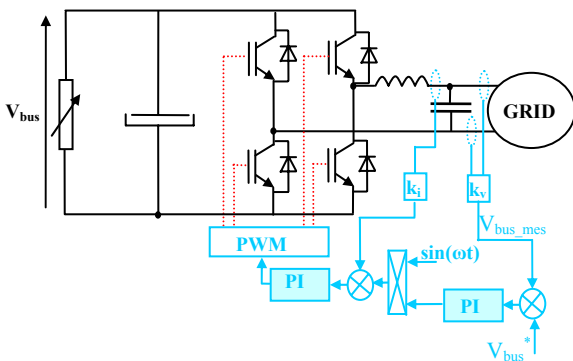


Fig.7. PWM inverter control architecture

The current internal loop permits to control the grid current. The grid current reference is elaborated by the

multiplication of the current amplitude (made by the external DC voltage loop) by the grid voltage phase ( $\sin(\omega t)$ ). Therefore the voltage and the current of the grid are sinusoidal and in phase. Each loop controller is chosen to obtain quasi-null static error.

D. PWM rectifier control

The PWM rectifier imposes the active power reference on the production/storage system while extracting sinusoidal current in phase with the sinusoidal output voltage of the reversible inverter. The PWM rectifier command is shown on Fig.8 (the PWM inverter and the grid are symbolized by 400 V DC voltage source).

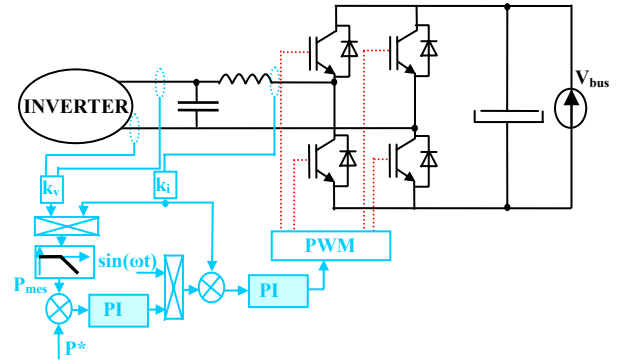


Fig.8. PWM rectifier control architecture

In order to control the active power required by the system, the real one must be measured (as depicted on the previous figure). Firstly, the instantaneous current and voltage are assessed with sensors and multiplied with each other to create the instantaneous power and then this power has to be filtered into a low-pass filter to isolate only the active power measurement.

The inverter current reference is achieved as well as the grid current reference (the amplitude reference comes from the external active power loop).

6. DC bus capacitor current

The output frequency of the system reversible inverter is not synchronized with the grid frequency. This frequency difference can create a high amplitude low frequency current into the 6600  $\mu$ F DC bus capacitor. This current must be quantified in order to achieve the dimensioning of this capacitor. The notations used for are shown on the Fig.10.

With:

$$v_1(t) = V_M \cdot \sin(\omega_1 \cdot t) \quad (4)$$

$$v_2(t) = V_M \cdot \sin(\omega_2 \cdot t)$$

$$i_1(t) = I_M \cdot \sin(\omega_1 \cdot t) \quad (5)$$

$$i_2(t) = I_M \cdot \sin(\omega_2 \cdot t)$$

Two separate frequency domains must be considered: the high frequency introduced by the PWM frequency (15 kHz) and the low frequency of the grid (50 Hz).

In order to express the capacitor current, the cyclic ratio of each PWM converter must be specified. For the first

PWM converter, it comes (considering low frequency variations):

$$v_L(t) = v_1(t) - \langle U \rangle_{LF}(t) \quad (6)$$

With the following evolution for the tension U (Fig.9):

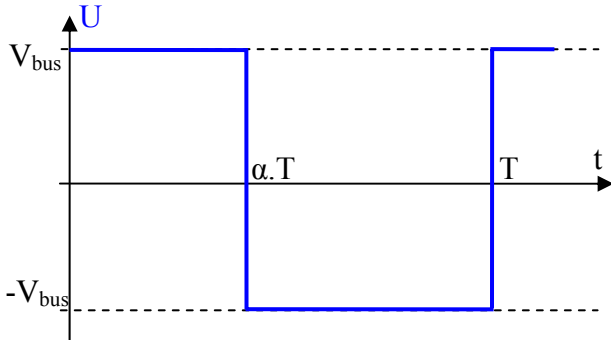


Fig.9. Evolution on a PWM period of the tension U

The average value, which evolves according to sinusoidal voltage of the grid frequency, on a PWM period, is equal to:

$$\langle U \rangle_{LF}(t) = (2 \cdot \alpha_1(t) - 1) \cdot V_{bus} \quad (7)$$

On the assumption that low frequency voltage drop into the inductance is negligible in view of the DC bus and the grid voltage:

$$\alpha_1(t) = \frac{1}{2} + \frac{V_M}{2 \cdot V_{bus}} \cdot \sin(\omega_1 \cdot t) \quad (8)$$

The reasoning is identical for the PWM converter which is connected to the grid:

$$\alpha_2(t) = \frac{1}{2} + \frac{V_M}{2 \cdot V_{bus}} \cdot \sin(\omega_2 \cdot t) \quad (9)$$

According to these notations, considering negligible losses in the system and focusing only on the low frequency (LF) variations of the currents, the DC bus capacitor current can be expressed:

$$i_{C_{LF}}(t) = i'_{1_{LF}}(t) - i'_{2_{LF}}(t) \quad (10)$$

$$i_{C_{LF}}(t) = \frac{I_M \cdot V_M}{2 \cdot V_{bus}} \cdot (\cos(2 \cdot \omega_1 \cdot t) - \cos(2 \cdot \omega_2 \cdot t)) \quad (11)$$

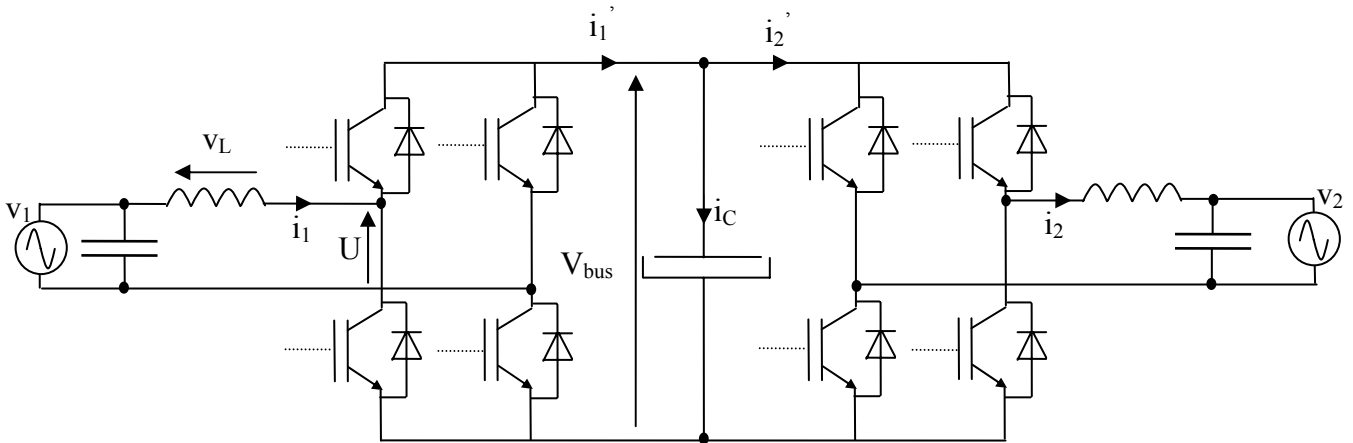


Fig.10. Notations used for the assessment of the capacitor current

The capacitor current in the worst case (maximum active power of 4.5 kVA corresponding to a 28 A peak current) is represented on Fig.11 (for this example  $f_1=47.5$  Hz and  $f_2=52.5$  Hz).

The RMS value of the capacitor current ( $I_C$ ) is given below ( $I'_1$  and  $I'_2$  are the RMS values of the currents  $i'_{1_{LF}}(t)$  and  $i'_{2_{LF}}(t)$ ):

$$I_C = \sqrt{I'^2_1 + I'^2_2} \quad (12)$$

$$I_C = \sqrt{2 \cdot \left( \frac{I_M \cdot V_M}{\sqrt{2} \cdot 2 \cdot V_{bus}} \right)^2} = \frac{I_M \cdot V_M}{2 \cdot V_{bus}} \quad (13)$$

The worst case leads to a value of 11.4 A<sub>RMS</sub>. This value does not lead to an excessive ageing of the capacitors.

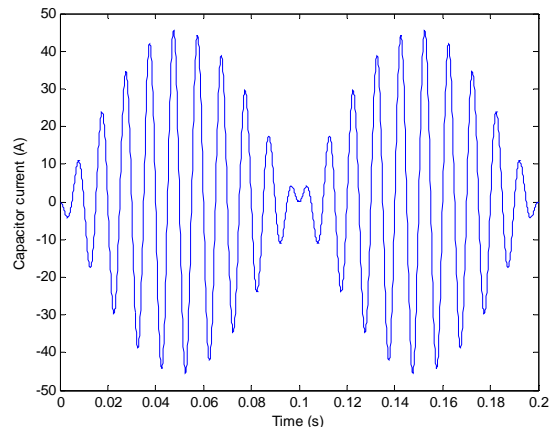


Fig.11. DC bus capacitor current

Once the low frequency capacitor current has been determined, its impact on the DC bus voltage must be assessed. Each component of the capacitor current causes

a voltage ripple on the DC bus. The RMS value of the DC bus voltage ripple is the following:

$$\Delta V_{bus} = \Delta V_{bus_1} + \Delta V_{bus_2} \quad (14)$$

Where  $\Delta V_{bus_1}$  is the ripple at  $\omega_1$  and  $\Delta V_{bus_2}$  the undulation at  $\omega_2$ .

$$\Delta V_{bus} = \frac{I_M \cdot V_M}{4 \cdot V_{bus} \cdot C \cdot \omega_1} + \frac{I_M \cdot V_M}{4 \cdot V_{bus} \cdot C \cdot \omega_2} \quad (15)$$

Always considering the worst case and the frequencies presented above, the maximum DC bus voltage ripple is equal to 5.5 V ( $\approx 1.37\%$  of 400 V).

## 7. Results

First we will focus on the PWM inverter results, and then the PWM rectifier results will be tackled.

### A. Inverter results

This PWM converter must control the current send back to the grid while regulating the DC bus voltage to the appropriate level. Fig.12 shows the grid voltage in green and the grid current in purple, the current is sinusoidal and in phase with the current except when the voltage grid is equal to zero because this is when the grid current undulation is the highest.

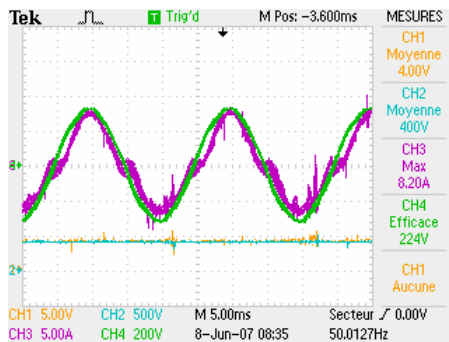


Fig.12. PWM inverter results

The DC bus voltage (in blue) is equal to 400 V as the command (in yellow) is 4 V, the static error is null.

### B. Rectifier results

This PWM converter control allows to extract a sinusoidal current from the reversible inverter while controlling the active power. Voltage (in purple) and current (in green) seem to be in phase but this current is rougher than the grid current.

With regards to the active power measurement (in blue) and reference (yellow), the static error seems to be null. The ripple at twice of power supply pulsation ( $2 \cdot \omega_2$ ) on the active power measurement is brought by the imperfect filtering of the low-pass filter.

The oscilloscope capture represented Fig.13 shows the PWM rectifier results:

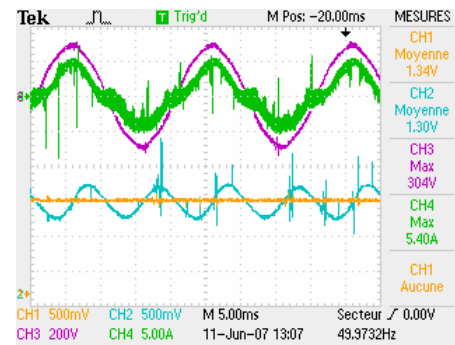


Fig.13. PWM rectifier results

## 8. Conclusion

The back-to-back converter used in order to realize a consumption profile emulator in such an application is at present innovative. The emulator currently allows us to run our experimental system with a long duration active power consumption profile stored in a MMC memory with the intention of validating experimentally our energy models of the different elements of the system on realistic situations. The difference between the grid frequency and the reversible inverter frequency does not lead to an unacceptable DC bus voltage ripple. We will continue our research by focusing specifically on reactive power loads in a very near future.

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