Characteristic impedance extraction of embedded and integrated interconnects

J. Roullard, S. Capraro, T. Lacrevaz, M. Gallitre, C. Bermond, A. Farcy, B. Fléchet

Characteristic Impedance of Integrated Interconnections: RF Experimental Extraction and Limit of Validity

J. Roullard[1], S. Capraro[1], T. Lacrevaz[1], M. Gallitre[1,2], C. Bermond[1], A. Farcy[2], B. Fléchet[1]

[1] Université de Savoie, IMEP-LAHC,UMR 5130, 73376 Le Bourget du Lac, France
[2] STMicroelectronics, 850 rue J. Monnet, 38926 Crolles cedex, France

Abstract: In this paper we extract the characteristic impedance of Back-End Of Line (BEOL) interconnections from radio frequency (RF) scattering parameter measurements. Quantification of the electric interconnection performance on a broad frequency band requires a good knowledge of the characteristic impedance Z_c and the propagation exponent γ. This propagation exponent is easily obtained by measuring two interconnections with different lengths. However, because of the complex test structure with mismatched ports where interconnections are embedded, the extraction of Z_c from scattering parameter measurements remains challenging. To solve this problem, we propose an approach based on the Winkel method without using simplified hypotheses generally applied. Limits of validity for our de-embedding procedure to extract characteristic impedance are also analyzed.

Key words: **Characteristic impedance, interconnections, de-embedding, impedance jump, transmission line.**

1. Introduction

Nowadays interconnections play a dominating part on integrated circuits performance of the new generations, as CMOS sub-65 nm nodes [1]. They are indeed at the origin of more than 40 % of the functioning circuit's time. New technological developments are thus necessary and one of the privileged ways is the integration of intermetallic insulators with a low permittivity, as SiOCH ($\varepsilon_r < 2.7$) porous oxide [2]. This low permittivity makes possible to reduce at once the capacities of the interconnections, crosstalk and delay.

To quantify performance of interconnects, as delay, rise time and crosstalk, propagation exponent and characteristic impedance of these transmission lines must be extracted. The major difficulty of such measurements comes from the surrounding of interconnects. Indeed they are embedded in a complicated stack inside the Back End Of Line (BEOL), with contact pads, vias or dummies. De-embedding procedures must be performed to avoid parasitic effects due to this surrounding and to extract intrinsic electrical performance of interconnects. De-embedding procedures to measure propagation exponent of interconnects are well known and rigorous [3,4]. Rigorous extraction of characteristic impedance for embedded transmission lines is mathematically unsolvable without a reference impedance used as calibration standard and this standard must be measured in the same surrounding of the interconnect under test. This standard calibration is not rigorously feasible. Many procedures have been proposed to extract the characteristic impedance of embedded interconnects without this embedded calibration standard [4-7] but they need hypotheses to solve the equations associated to each approach.

In this paper we propose to improve the method developed by Winkel [6,7] to extract the characteristic impedance of transmission lines and to adapt this method to interconnect integrated in BEOL. Accuracy of our method is analyzed and a study about limits of validity is performed.

2. Description of the de-embedding procedure

The objective is to determine the characteristic impedance of the under test interconnection zone, noted DUT in Fig. 1, using [S] scattering matrix measurements obtained with a vector network analyzer (VNA).

All de-embedding classics procedures require equivalent electric models, for "pads" and "access" zones, noted A and B in Fig. 1, leading to the DUT zone. These equivalent electric models are inevitably not perfectly rigorous and induce some approximations in extraction procedure.

On the other hand in T.M. Winkel works, two devices families (Fig. 2), allow to determine the interconnection characteristic impedance without using equivalent electric models for A and B zones.

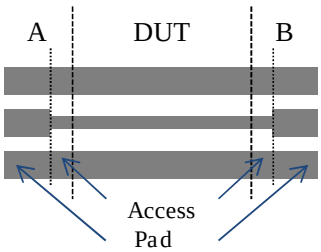
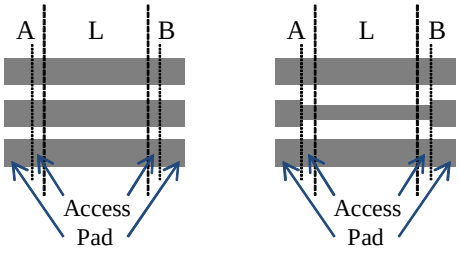


Fig. 1: Schematic top view of interconnection under test embedded inside pads and access lines.



(a) (b)

Fig. 2: Schematic top view of de-embedding devices
(a) Device for impedance characteristic determination of pads
(b) Device for impedance characteristic determination of DUT.

Each family requests several [S] scattering matrix measurements, for different devices lengths L. A previous OSTL calibration is performed in order to set a 50 Ω reference impedance at the probe tip.

Results from measurements of devices represented in Fig. 2a are used to determine the pad characteristic impedance Z_p. Next results from measurements of devices represented in Fig. 2b are used to extract the characteristic impedance Z_c of the interconnection under test.

The following section details the procedure of de-embedding to extract the characteristic impedance of the interconnection under test.

2.1 Determination of the pad characteristic impedance Z_P

2.1.1 Measurement stage

Measurements of the two [S] matrix for two different lengths L1 and L2 of transmission lines, obtained from the device presented in Fig. 2a, are necessary to extract the characteristic impedance of the pads (S_{m1} and S_{m2}). Each [S] matrix is expressed in [T] matrix. As each device can be broken up into three zones, noted A, L and B, the following relations are obtained:

$$T_{m1} = T_A . T_{L1} . T_B \quad (1)$$

$$T_{m2} = T_A . T_{L2} . T_B \quad (2)$$

T_A, T_L, T_B correspond respectively to the [T] matrices of A, L and B zones.

T_B can be eliminated by the operation:

$$T_{m2} . T_{m1}^{-1} = T_A . T_{L2} . T_{L1}^{-1} . T_A^{-1} \quad (3)$$

T_{L1} and T_{L2} matrices are easily known using the measurement of the propagation exponent γ of the device.

We note:

$$T_{m2} . T_{m1}^{-1} = T_{mp} \quad (4)$$

By transforming the T_{mp} matrix into ABCD matrix, noted A_{mp}, it is possible to define the XP coefficient:

$$XP = \sqrt{\frac{A_{mp12}}{A_{mp21}}} \quad (5)$$

Value of XP is known by measurements.

In the next paragraph, we are going to determinate the theoretical XP expression, according to Z_p, with a theoretical model. Then we are going to deduce Z_p by identifying both XP expressions.

2.1.2 Theoretical model

In this paragraph, expressions of the T_A matrix terms, given by equation (3), are established according to the pad characteristic impedance Z_p.

Zone A of the device represented in Fig. 2a can be decomposed as in Fig. 3:

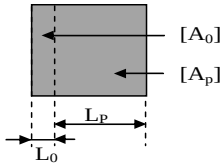


Fig. 3: Schematic decomposition of zone A of the device described in Fig. 2a.

The zone A can be decomposed into two elements: a reflection element noted A_0 (Length: L_0 and propagation exponent: γ_p) and a transmission element noted A_P (Length: L_p and propagation constant: γ_p). From this decomposition, the following relation can be obtained:

$$A_{AP} = A_{r1} . A_0 . A_P . A_{r2} \quad (6)$$

where A_{r1} and A_{r2} are the normalized matrices.

$$A_0 = \begin{bmatrix} 1 & 0 \\ \dfrac{\tanh(\gamma_p . L_0)}{Z_p} & 1 \end{bmatrix} \quad (7)$$

$$A_p = \begin{bmatrix} \cosh(\gamma_p . L_p) & Z_p . \sinh(\gamma_p . L_p) \\ \dfrac{\sinh(\gamma_p . L_p)}{Z_p} & \cosh(\gamma_p . L_p) \end{bmatrix} \quad (8)$$

From equations (6), (7) and (8) the A_{AP} matrix can be obtained according to Z_P. By transforming the A_{AP} matrix into T matrix (noted T_A), the following expression can be determined:

$$T_{Thp} = T_A . T_{L2} . T_{L1}^{-1} . T_A^{-1} \quad (9)$$

By transforming T_{Thp}, on ABCD matrix, noted A_{Thp}, the XP coefficient can be defined according to Z_P.

$$XP = \sqrt{\frac{A_{thp12}}{A_{thp21}}} \quad (10)$$

2.1.3 Identification

The following relation is obtained by using equations (5) and (10):

$$XP = \sqrt{\frac{A_{mp12}}{A_{mp21}}} = \sqrt{\frac{A_{thp12}}{A_{thp21}}} \quad (11)$$

A_{mp12} and A_{mp21} terms are known from measurements. A_{thp12} and A_{thp21} terms are expressed according to Z_P. Thanks to the identification of these four terms, Z_p can be deducted according to XP, γ_p and L_0 values:

$$Z_p = XP.Z_0.\sqrt{1-\tanh(\gamma_p.L_0)^2} \qquad (12)$$

2.2 Determination of the DUT interconnect characteristic impedance Z_c

The characteristic impedance Z_c determination of the interconnection under test is based on the same method as the extraction of the pad characteristic impedance.

Measurements of devices described in Fig. 2b allows to determine XL coefficient (equivalent for the interconnect of the XP coefficient for pads) which is identified to the theoretical XL expression, according to Z_c.

To obtain the theoretical XL expression, it is necessary to express the ABCD matrix of the zone A, named A_{AS}, of the device shown in Fig. 2b. This zone A is decomposed in three elements (Fig. 4): A_0 for the reflection part, A_P for the pad transmission part and A_S (Length: L_s and propagation constant: γ_s) for the interconnect transmission part.

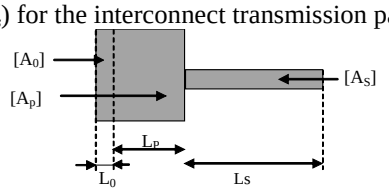


Fig. 4: Schematic representation of the zone A for the device described in Fig. 2b.

The following relation can be deducted for A_{AS}:

$$A_{AS} = A_{r1}.A_0.A_P.A_S.A_{r3} \qquad (13)$$

where A_{r1} et A_{r3} are the normalized matrices.

So, from this matrix and measurements made on devices shown in Fig. 2b, measured and theoretical XL coefficients are obtained. The first one is known and the second one is according to Z_c. Then by identification, the characteristic impedance expression of the DUT interconnect, Z_c, can be deducted.

$$Z_C = Z_P.\sqrt{\frac{num}{deno}} \qquad (14)$$

with:

$$num = Z_p^2.\sinh(\gamma_p.L_p)^2 + Z_0^2.XL^2. \left(\cosh(\gamma_p.L_p)+\sinh(\gamma_p.L_p).\tanh(\gamma_p.L_0)\right)^2 \qquad (15)$$

$$deno = Z_0^2.XL^2. \left(\sinh(\gamma_p.L_p)+\cosh(\gamma_p.L_p).\tanh(\gamma_p.L_0)\right)^2. Z_p^2.\cosh(\gamma_p.L_p)^2 \qquad (16)$$

3. Results of characteristic impedance extraction

3.1 Description of validation devices and results

Devices were designed with a simple technological stack, shown in Fig. 5, composed by a glass substrate and an aluminium metallic level. Two different widths interconnections, 40 µm and 100 µm, were realized.

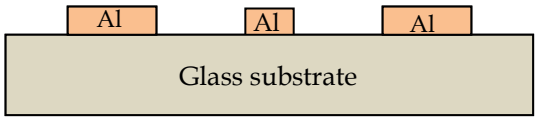
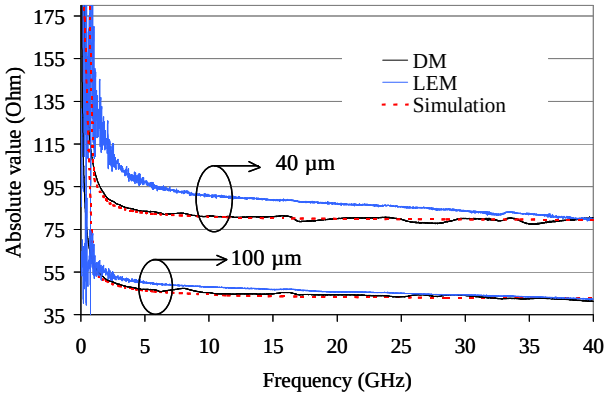
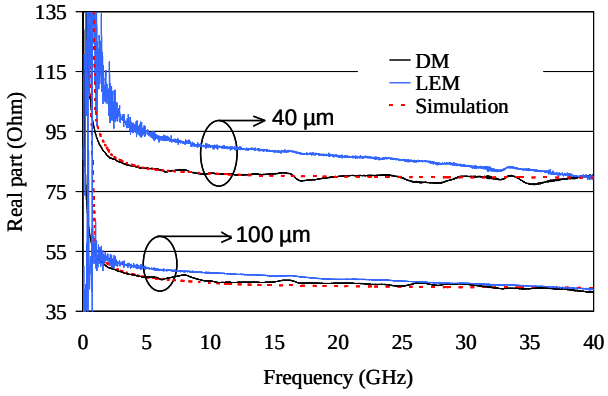


Fig. 5: Schematic cross section view of the device.

In order to validate this extracted characteristic impedance method, a comparison between the developed method (DM), a localized element method (LEM) and a 2D simulation (QUEST Silvaco) have been realized.



(a)



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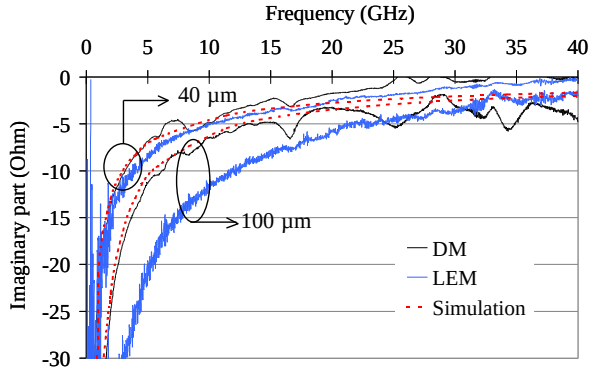
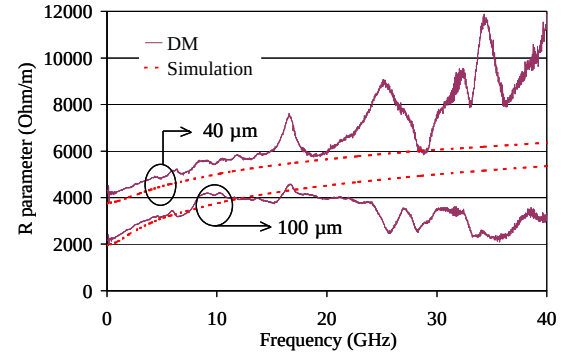


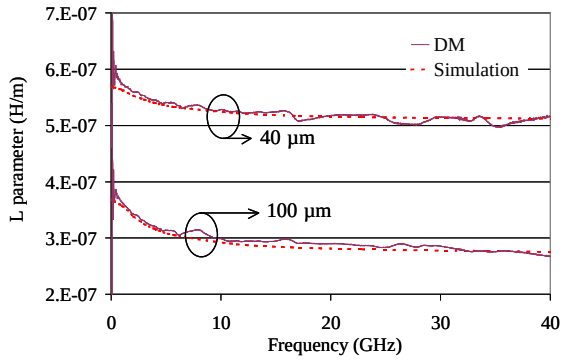
(c)

Fig. 6: Comparison between experimental and simulation results from two devices with different widths.
(a) Absolute value (b) Real part (c) Imaginary part of characteristic impedance

Fig. 6 shown that, the developed method is more precise than the localized element method. Indeed results extracted with this method are almost identical to those obtained by simulation on the broad frequency band, due to the consideration of the propagation phenomena in pads.



(a)



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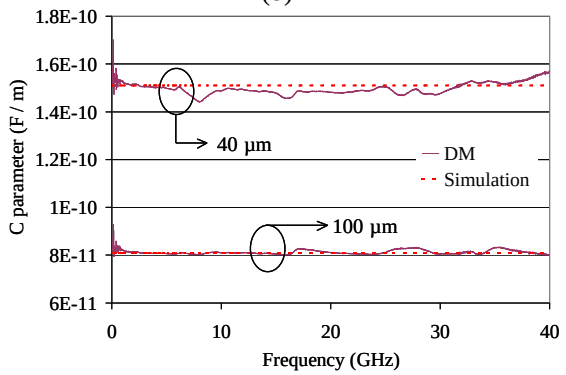

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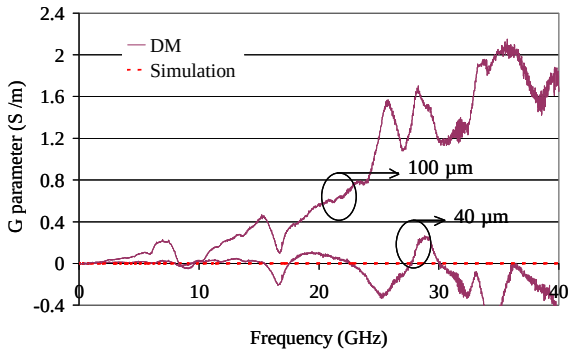

(d)

Fig. 7: Comparison between experimental and simulation results from two devices with different widths.
(a) R parameter. (b) L parameter. (c) C parameter. (d) G parameter.

According to Fig. 6, an higher value of real part of characteristic impedance at low frequency have been obtained due to the effect of metal loss. However high frequency stabilization of real and imaginary parts reflects a substrate without loss.
DUT interconnection characteristic impedance Z_c and the propagation exponent γ are enough to deduce the R, L, C, G parameters.

Fig. 7 presents results obtained by using Zc from the developed method and Zc from 2D electromagnetic simulation. Experimental extractions are stacked with the simulation for L and C parameters on the broad frequency band. Concerning R and G parameters, a light variation beyond 10 GHz was observed.
Resistance parameter increases with the frequency, which reflects the skin effect in the interconnection. At lower frequency, fields in metallization were observed by the increasing inductance. However C parameter remains stable, due to glass substrate. G parameter variation is due to a lack of precision in the extraction of primary parameters.

3.2 Description of microelectronics devices and results

Following the validation method, sub-micronics interconnections are characterized in a real environment of integrated circuits of the 45nm node where metallic lines are 450nm widths copper. This device, show in Fig. 8, are realized with a silicon substrate layer, a copper layer of 100nm thickness, then a 900nm silicon dioxide layer and a 220nm of BDIIx layer are deposited. On the last level metallization, interconnection and ground are obtained with a 140nm copper thickness and between metallization, a BDIII layer are deposited.

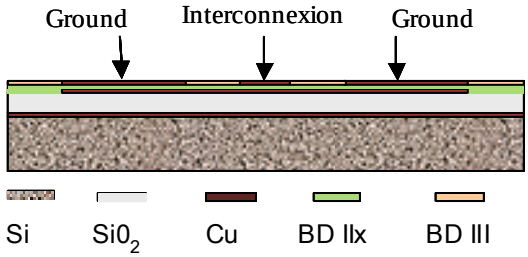

Fig. 8: Schematic cross section view of the device.

Fig. 9 compares the DUT interconnections characteristic impedance obtained with the developed method at those obtained with simulation, we can see a very good agreement on the broad frequency band.

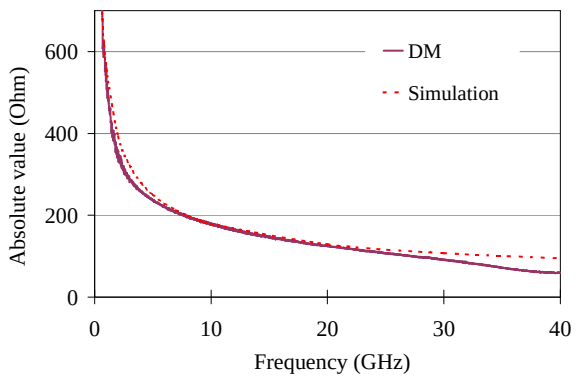

Fig. 9: Comparison of absolute characteristic impedance value, between experimental result and simulation for a 450 nm interconnection width.

4. Transitions considerations - Limit of validity

4.1 Theoretical model

For the DUT interconnection characteristic impedance determination, the transition between pads and lines is considered by a simple impedance jump, modelized by a reflection coefficient, equation 17, and a [S] matrix, noted $S_{t'}$, shown in matrix 18.

$$\Gamma = \pm \frac{(Z_p - Z_c)}{(Z_p + Z_c)} \qquad (17)$$

$$S_{t'} = \begin{bmatrix} |\Gamma| & \left|\sqrt{1-\Gamma^2}\right| \\ \left|\sqrt{1-\Gamma^2}\right| & |\Gamma| \end{bmatrix} \qquad (18)$$

However, to be more meticulous, this transition can be represented by a quadripole having a [S] matrix, noted S_t which is different to impedance jump [S] matrix $S_{t'}$, especially when the topology is marked.

In order to know the limit of validity of this method, we compare the $S_{t'}$ matrix at S_t matrix. We obtained $S_{t'}$ matrix from a double LRL calibration realized on the level of P and P' plans, on specific structures shown in Fig. 10.

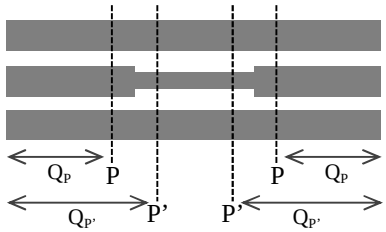

Fig. 10: Schematic top view of device for a double LRL calibration. The first calibration is performed on P level and the second calibration on P' level.

With this two calibration, we can deduice the [S] matrix of Q_P and $Q_{P'}$ quadripoles, respectively noted S_{QP} and $S_{QP'}$. The [T] matrix of the pad-interconnection transition,noted T_t can be determined with the equation 19 and by transforming previewsly [S] matrix into [T] matrix, respectively noted T_{QP} and $T_{QP'}$.

$$T_{QP'} = T_{QP} . T_t \qquad (19)$$

Once the [T] matrix known, the S_t matrix can be deducted and compared with the $S_{t'}$ matrix obtained by considered the transition like an impedance jump.

If S_t and $S_{t'}$ matrices are identical, the extraction procedure is valid and we can consider the transition like a simple impedance jump. In the contrary case, the transition between pad and interconnection does not behave as a simple impedance jump and the Z_c extraction obtained is falsified by the bad modelization of the transition.

4.2. Experimentation to find the limit of validity

Tested devices, show in Fig. 11, were realized from a technological stacking of integrated circuits composed of a silicon substrate, a thin SiO_2 layer and copper metal lines. Studies have been execute on devices having different widths.

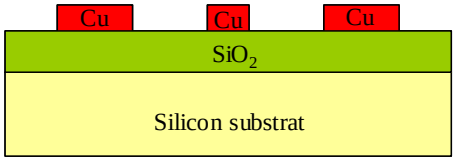

Fig. 11: Schematic cross section view of the device.

The configuration studied is composed by a 3 µm interconnection widths and 50 µm pads widths.

According to Fig 12, S_{11} and S_{21} parameters of the transition, between pads and interconnection, obtained by the double LRL calibration (noted Real Transition), are compared at the impedance jump S_{11} and S_{21} parameters.

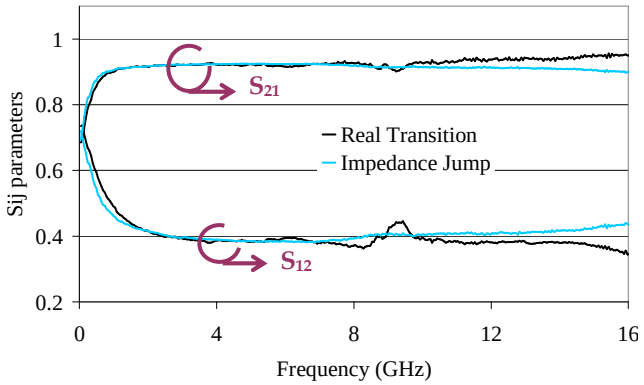

Fig 12: Comparison between transition S_{ij} matrix and an impedance jump S_{ij} matrix

The relative ratio δ (equation 20), between the both matrix can be deducted, by using S_{ij} matrix parameters of the transition. This value represent the error when we considered the transition like an impedance jump.

$$\delta = \frac{S_{t'} - S_t}{S_{t'}} \qquad (20)$$

In Fig. 13 it can be observed that the relative error increases in an exponential way according to the frequency. For example, a 3 µm width interconnection presents a relative error insignificant for frequency lower than 5 GHz. On the other hand for frequency above 5 GHz, the error made on the characteristic impedance can not be ignored because it reaches a little more than 5 % at 15 GHz.

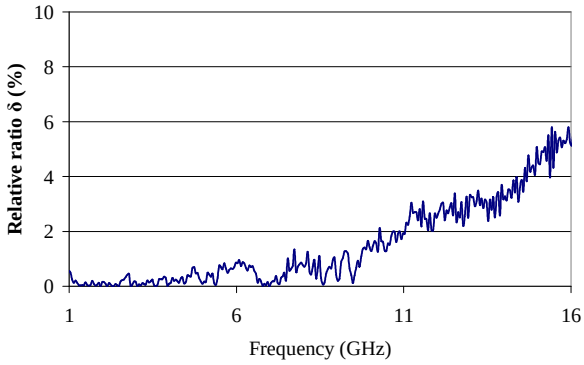

Fig. 13: Relative ratio for a 3 µm interconnection width.

In order to compare the error made by the developed method, extractions were realized on interconnections which widths varied between 3 and 25 µm at 15 GHz (Table 1).

Table 1: Relative error on S_{ij} parameter for different interconnections widths at 15 GHz, between our developed method and measurements.

Interconnection width (µm)	3	5	10	25
Relative error (%)	5.1	2.5	1.8	1.3

According to these results, the error made decreases when the interconnection width increases and gets closer to the pad width. Therefore, the modelling transition pad-nterconnection by a simple impedance jump will become hazardous for lowest interconnection width. In order to correct the transition effect, it will be necessary to carry out an iterative process on Z_c until obtaining the same S_{ij} matrix for the transition, between S_{ij} matrix obtained by measurement (S_t) and S_{ij} matrix obtained by the developed method ($S_{t'}$).

5. Conclusion

The extraction protocol of the characteristic impedance was validated on devices with a technological stack composed of a glass substrate and aluminium metallic lines then interconnections of advanced microelectronic circuits of the 45 nm node. The developed method allows to obtain results more precise than the localized method elements.

The double LRL calibration procedure allows to verify the consideration of the transition pad - interconnection and shows that the extraction is reliable when transitions are a small form factor.

The knowledge of the constant propagation and the characteristic impedance of the interconnection will enable to determine the R, L, C, G parameters which allow to determine the dielectric materials permittivity or the metallization conductivity of the interconnect network.

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