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# Thermal stability of silicon-carbide power diodes

Cyril Buttay, *Member, IEEE*, Christophe Raynaud, Hervé Morel, *Member, IEEE*, Gabriel Civrac, Marie-Laure Locatelli, Florent Morel, *Member, IEEE*

**Abstract**—Silicon carbide (SiC) power devices can operate at much higher junction temperature than those made of silicon. However, this does not mean that SiC devices can operate without a good cooling system. To demonstrate this, the model of a Merged PiN Schottky (MPS) SiC diode is presented, and its parameters are identified with experimental measurements. This model is then used to study the ruggedness of the diode regarding the thermal run-away phenomenon. Finally, it is shown that where a purely unipolar diode would be unstable, the MPS structure brings increased stability.

**Index Terms**—Silicon carbide, Power electronics, High temperature techniques, Schottky diodes, P-i-n diodes

## I. INTRODUCTION

WIDE BANDGAP power devices, especially those made using silicon carbide (SiC), offer very good performance regarding high temperature electronics. The ubiquitous silicon devices are indeed limited to 150 to 200 °C, depending on their breakdown voltage (see figure 1), whereas SiC devices successfully operating at much higher junction temperature have been reported. For example, an inverter operating at 250°C (resulting in an ever higher junction temperature) is described in [1]. In [2], the authors present a converter with a SiC JFET and a Schottky-Barrier Diode (SBD) operating at 450°C.

Applications of high-temperature power devices include aircraft, space, oil and gas exploration [3], where power systems are expected to operate in an elevated ambient temperature. These devices are also interesting in milder environments, because they should require less cooling. This latter approach is described in [4]: using a power module designed for 250°C in a 150°C environment allows for the use of a much smaller heatsink. Si-based devices indeed offer less headroom between the ambient and maximum junction temperatures, requiring very efficient cooling. This is of great importance, as the thermal management system is one of the bulkiest and heaviest parts of a converter.

However, a recent paper [5] has shown that SiC devices are sensitive to thermal runaway. The author claims that SiC devices could not be able to operate realistically above 200°C, and that they require an efficient cooling system. The paper shows theoretically that exceeding these limits results in an unstable situation, where temperature builds up in the device because the power dissipated is not properly removed. As the junction temperature of the device increases, its power

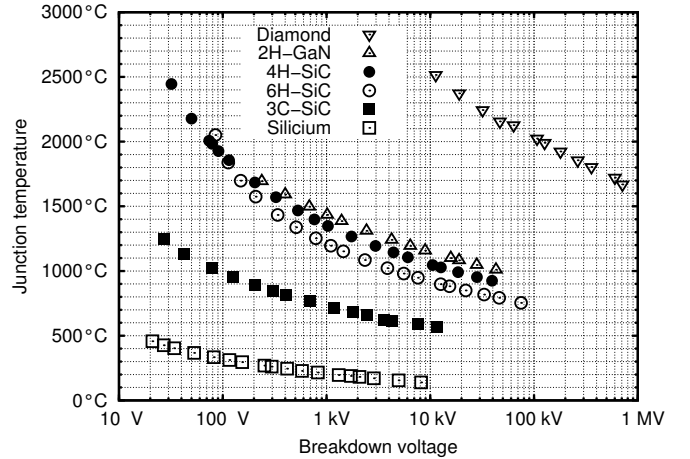


Fig. 1. Theoretical semiconductor runaway temperature as a function of the breakdown voltage, for various semiconductor materials [7]

TABLE I  
TEMPERATURE LIMITS FOR VARIOUS ELEMENTS OF A SiC DIE.

	material	max. temp.	cause
Semiconductor	SiC	2730°C	sublimation
Schottky metal	Ti	1668°C	melting point
Top metallization	Al	660°C	melting point
secondary passivation	polyimide	500-620°C	decomposition
contact anneal. [8]	Ti/Ni	350-500°C	solid state reaction

losses increase as well, eventually yielding to destruction. This phenomenon is called thermal runaway.

Some of the findings of [5] were confirmed in [6], for a SiC SBD operating in a room-temperature ambient. However, as new diode structures are now available on the market, and because these diodes could operate in a high-ambient temperature environment, it appears that further studies are needed to assess the extent of the issue on these structures. This is the object of the present paper.

The first section is dedicated to a presentation of the mechanisms that trigger the thermal runaway. Then, the device under study, a SiC diode, is presented along with its model. The experimental identification of the parameters of this model is described in the third section. Finally, using this model, the conditions of thermal runaway are investigated and discussed.

## II. THEORETICAL LIMITS

### A. Maximum Operating Temperature of Power Devices

Silicon Carbide remains solid up to 2730°C. However, the actual maximum operating temperature of a SiC device is much lower.

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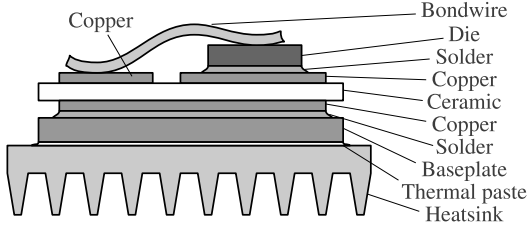


Fig. 2. Cross-section of a power module

One of the limits is the Semiconductor Thermal Runaway (STR) described in [7]: Above a certain temperature, the intrinsic carrier density becomes higher than the maximum doping level sustaining a given voltage. So at the STR, the material is no longer able to block its rated voltage. The device becomes more and more conductive as the temperature increases, and the temperature increases as more current flows through the device (runaway phenomenon). It can be seen from figure 1 that a 1200 V (4H-SiC) device has a maximum operating temperature of around 1500 K (1230°C).

Furthermore, a SiC-based device actually requires some other materials, such as metals for the contacts, and some passivating materials. For example, the device that is used in this paper has a thick layer (a few micrometers) of Aluminium on top of the anode for compatibility with the wirebonding process. It also uses polyimide for the secondary passivation. The maximum temperature these materials can sustain are summarized in Tab. I.

Finally, during the manufacturing process, the dies are submitted to a rapid thermal annealing step to improve the metal/semiconductor contact. Depending on the annealing temperature, either Schottky or ohmic contacts are formed: for example, it has been shown that a Ti/Ni Schottky contact (annealed at 350°C) can become ohmic if annealed at 500°C [8].

Therefore, it can be said that in the case of a Ti/Ni SiC-Schottky diode, the maximum operating temperature must be lower than 500°C. Note that this does not mean that some ageing phenomenon will not occur at a lower temperature. Mechanisms such as chemical species diffusion or polyimide degradation are known to be activated at a lower temperature [9], especially in presence of oxygen. This is confirmed by tests in our research group (to be published), which showed that the behaviour of a Ti/Ni Schottky diode degrades rapidly after being stored a few hours at 350°C, even under vacuum. However, it should be noticed that this does not constitute an intrinsic limitation of SiC devices, as other metals can be selected as the Schottky contact (such as tungsten [10]), or bipolar devices can be used instead of unipolar. Note that ageing phenomena are beyond the scope of this paper.

### B. Conditions of the Device Thermal Runaway

The cross-section of a power module is shown in figure 2. With such a module, the power dissipated by the semiconducting die (on top) is transferred through the various layers of the module to the heatsink (bottom) and then to the ambient

medium (in the case of figure 2, this is the surrounding air). For other packaging solutions (for example in the case of discrete components), the composition of the stack may differ, but the cooling technique is the same.

As stated by the first law of thermodynamics, the variation of the internal energy in the device ( $U$ ) is:

$$\frac{dU}{dt} = P - Q \quad (1)$$

Where  $P$  is the electrical power dissipated in the device and  $Q$  is the heat flux removed from the device.

At the electrical steady state, in conduction mode,  $P = I \times V$ , with  $V$ , the voltage across the device being a function of  $I$  and  $T_j$ , the junction temperature.  $I$  is the current flowing through the device. Therefore,  $P$  is itself a function of  $I$  and  $T_j$  only:

$$P = I \times V(I, T_j) = P(I, T_j) \quad (2)$$

At the thermal steady state,  $\frac{dU}{dt} = 0$ , so from (1)  $P = Q$ , which simply means that the cooling system removes all the energy supplied to the device. If we consider a very simple model for the cooling system, based on conduction only, the heat flux removed is equal to:

$$Q = \frac{T_j - T_A}{R_{Th}} = \frac{\Delta T}{R_{Th}} \quad (3)$$

With  $R_{Th}$  the thermal resistance between the junction of the device and its environment (ambient temperature), and  $T_A$  the ambient temperature.

If we consider slow thermal transients at the electrical steady state (quasi-static conditions), (1) can be rewritten using (2) and (3):

$$\frac{dU}{dt} = P(I, T_j) - \frac{T_j - T_A}{R_{Th}} \quad (4)$$

For a given, constant  $I$ , this equation can be expressed (in the neighbourhood of an initial temperature  $T_{j0}$ ) as the following linearization:

$$\frac{dU}{dt} = P(T_{j0}) + \frac{\partial P}{\partial T_j} (T_j - T_{j0}) - \frac{T_j - T_A}{R_{Th}} \quad (5)$$

$$\frac{dU}{dt} = P(T_{j0}) + \frac{\partial P}{\partial T_j} \varepsilon - \frac{T_{j0} - T_A}{R_{Th}} - \frac{\varepsilon}{R_{Th}} \quad (6)$$

with  $\varepsilon = T_j - T_{j0}$ . As stated above,  $T_{j0}$  corresponds to a steady state if  $\frac{dU(T_{j0})}{dt} = 0$ , that is, if

$$P(T_{j0}) = \frac{T_{j0} - T_A}{R_{Th}} \quad (7)$$

In figure 3, this corresponds to the intersects between the device (dashes) and cooling (plain) characteristics. This figure represents the power  $P(T_j)$  dissipated by an imaginary device (at a constant current) depending on its junction temperature, and the cooling capability ( $\frac{T_j - T_A}{R_{Th}}$ ) of its associated thermal management system.

$T_{j0}$  is a point of stable equilibrium if a small variation in junction temperature  $\varepsilon$  yields an opposite variation in internal energy (negative feedback), that is if

$$\text{sgn} \left( \frac{\partial P}{\partial T_j} \varepsilon - \frac{\varepsilon}{R_{Th}} \right) = -\text{sgn}(\varepsilon) \quad (8)$$

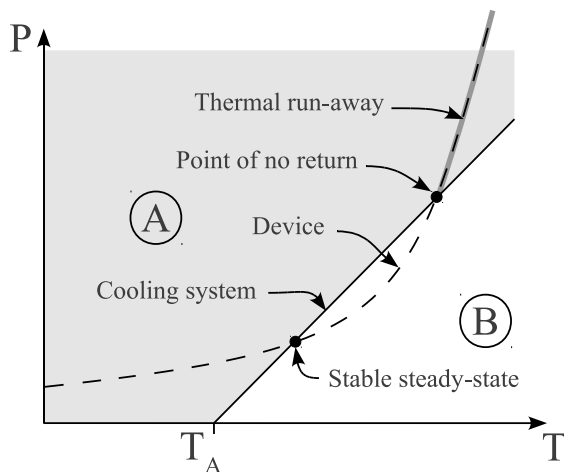


Fig. 3. Conditions of thermal equilibrium: when the device is in region A, it tends to heat up (because its power dissipation is higher than the cooling capabilities). When in region B, it tends to cool down.

In figure 3, this corresponds to the lower intersect only, the higher intersect being an unstable equilibrium.

Let us consider that the cooling system line divides the (P,T) domain in two regions (A and B). When a point of the device characteristic is located in region B (that is, under the cooling system line), that means that the device dissipates less power than the cooling system can extract. Therefore, the system tends to cool down. On the contrary, when a point is located in region A, the system tends to warm up. Graphically, that means that a point in region A will move along the device characteristic towards the right, until it reaches an intersect with the cooling system line (or until it fails), whereas it will move to the left if it is in region B.

Therefore, it must be noticed that both intersects in figure 3 have different properties: the lower one corresponds to a stable equilibrium (attractor). The higher intersect, in the opposite, is an unstable equilibrium. If the device experiences even a small cooling down, it will get attracted by the lower intersect. If it gets a bit hotter, it enters region A and will warm indefinitely (that is, until it fails due to the limits described in section II-A). This corresponds to the so-called device thermal runaway (DTR) [11]. As can be seen, a device is at risk of thermal runaway if its characteristics enters in region A as the temperature increases. This can happen either because the device characteristic is always above the cooling system line, in which case there is no equilibrium point at all, or as described in figure 3: here instability occurs only above a certain point (the “point of no return” in the figure).

From (3), it can be seen that the ambient temperature  $T_A$  corresponds to the x-intercept of the cooling system line in figure 3. This means that if  $T_A$  increases, the cooling system line shifts towards the right, as illustrated in figure 4(c). Eventually, one might end up in the situation where the device characteristic is completely in region A, meaning that there is no longer any stable equilibrium possible ( $T_{A3}$  in figure 4(c), which corresponds to figure 4(b)).

Finally, please note that the device characteristic is plotted in figure 3 for a given  $I$  only. As we will see below, it is

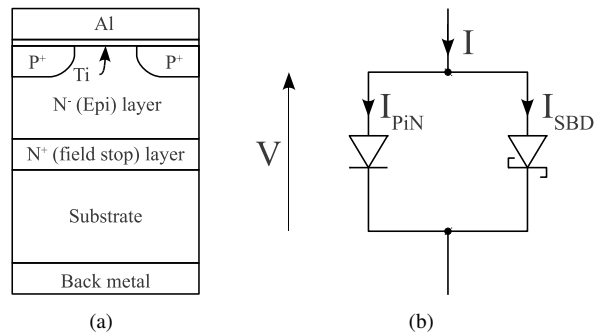


Fig. 5. Internal structure of the MPS diode, as described in [12] (a) (terminations not shown), and its equivalent model when forward-biased (b).

important to ensure that the system remains thermally stable, even if the device experiences an increase in current.

After this introduction to the DTR, we will present in the next section an analytical model for the SBD and MPS diodes. This model will then be used for a stability study.

### III. MPS DIODE MODELLING

Si-based diodes have to rely on a bipolar structure above 100 to 200 volts. In the opposite, due to the much better performance of their base material, SiC Schottky diodes can be designed for voltages up to several kilovolts [13]. The Schottky Barrier (unipolar) Diodes offer several advantages over their bipolar counterparts, such as very low switching losses or simple parallel-connection [12]. This explains why bipolar SiC diodes are only considered for very high voltage applications (several kilovolts) [14].

However, pure SBDs have shown a lack of ruggedness, especially when submitted to current overload or avalanche. Diodes based on a Merged PiN Schottky structure have been proposed [15], [16] to overcome this issue.

Compared to other PiN-Schottky mixed structures such as the JBS (Junction Barrier Schottky), the MPS diode is designed so that the bipolar features are not involved during normal operation [13]. They are only active during current or voltage overloads. Reliability is therefore improved without the large reverse recovery currents associated with bipolar diodes.

The MPS diodes are supposed to behave as pure SBDs (under normal conditions). Therefore, the existing models of these devices do not consider a simultaneous conduction of the Schottky and bipolar junctions [17]. However, such a model is required in the present study, as the devices can be brought outside of their nominal operating conditions.

As describing a complete model for the MPS diodes would be beyond the scope of this paper, we will just focus on the on-state. Taking into account the switching losses would indeed require a lot more parameters, most of them being dependent not on the diode itself, but on the external circuit. The conduction losses in a forward-biased diode only depend on its forward current and voltage, and on its junction temperature. Furthermore, it has been shown that the conduction mode is the main source of losses for the SBDs [14].

Therefore, in the remaining of the paper, we will use the model described in figure 5: the MPS diode is considered

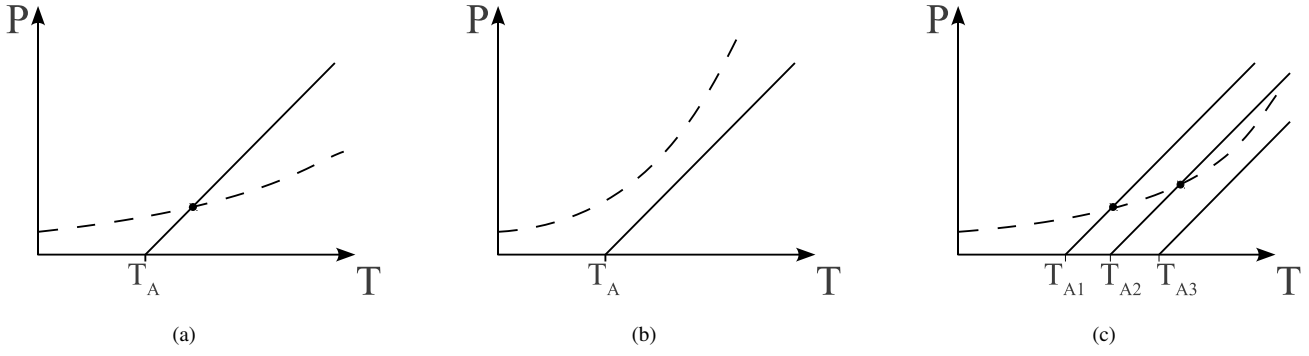


Fig. 4. Three particular cases: (a) only one intersect (unconditionally stable), (b) no intersect (no equilibrium), and (c) a change in stability (from stable to unstable) due to an increase in ambient temperature ( $T_{A1}$  to  $T_{A3}$ ).

as a parallel assembly of a SBD and a PiN diode. For both elements, only the forward behaviour will be modelled.

#### A. SBD Model

The model used for the SBD is described in [18], with some modifications added here to take into account the series resistance of the diode.

$$I_{SBD} = I_{sat} \left[ \exp\left(\frac{qV_d}{nkT}\right) - 1 \right] \quad (9)$$

With  $V_d$  the voltage bias applied to the metal-semiconductor junction,  $n$  the ideality factor, and  $I_{sat}$  given by:

$$I_{sat} = SA^*T^2 \exp\left(-\frac{q\Phi_e}{kT}\right) \quad (10)$$

$S$  being the surface of the diode,  $A^*$  the Richardson constant (see [18] for more details) and  $\Phi_e$  the effective barrier height.

The voltage across the diode,  $V$ , is equal to

$$V = V_d + R_S(T)I_{SBD} \quad (11)$$

Where  $R_S$  is the series resistance of the SBD, and it represents the resistance of the epitaxial layer, as well as that of the SiC substrate. It is considered to have the following dependence on temperature:

$$R_S(T) = R_{S300} \left(\frac{T}{300}\right)^K \quad (12)$$

Where  $R_{S300}$  is the series resistance at 300 K, and  $K$  is a temperature coefficient.

Merging (10) into (9) and (12) into (11) yields:

$$\begin{cases} I_{SBD} = SA^*T^2 \exp\left(-\frac{q\Phi_e}{kT}\right) \left[ \exp\left(\frac{qV_d}{nkT}\right) - 1 \right] \\ V = V_d + R_{S300} \left(\frac{T}{300}\right)^K I_{SBD} \end{cases} \quad (13)$$

#### B. PiN Diode Model

Equation (9) has been found not to be a good model for a PiN diode operating in high-injection [19]. This was confirmed in the present case, as trying to identify the parameters of (9) to the experimental data resulted in aberrant values. Better models exist but have more parameters [20], making them more difficult to identify. Therefore, it was decided to use a



Fig. 6. Picture of the vacuum probe station (with top cover removed) showing the diode under test, directly bonded to the temperature-controlled chuck and the three probes (the fourth is directly connected to the chuck)

very simple, empirical model based on a parabolic equation to represent the relationship between the forward voltage drop and the current in a PiN diode:

$$I_{PiN} = \beta(V - \alpha(T))^2 \quad (14)$$

with  $\beta$  a constant and  $\alpha(T)$  a linear function of temperature:

$$\alpha(T) = \alpha_0 + \alpha_1 T \quad (15)$$

Note that this model is only valid for  $V > \alpha(T)$  (that is, above the threshold voltage of the diode).

## IV. EXPERIMENTAL IDENTIFICATION

#### A. Experimental Setup

The devices under test are SiCED 1200 V un-packaged diodes, with a die area of  $2.7 \times 2.7 \text{ mm}^2$  (batch ref #1024). They are designed as 15 A-nominal-current diodes. The tested diodes are mounted directly on the heating chuck of a vacuum probe station (see figure 6) using a thin layer of silver adhesive. The temperature is monitored using a K-type thermocouple. Our tests showed a temperature accuracy of  $\pm 2 \text{ K}$  or  $\pm 1\%$  across the surface of the chuck. All the tests are performed under vacuum, to prevent the devices from oxidizing.

The electrical measurements are performed using a Keithley Source and Measure Unit (SMU) 2602A, which can source as much as 10 A in pulse mode. A 4-probe setup is used (two

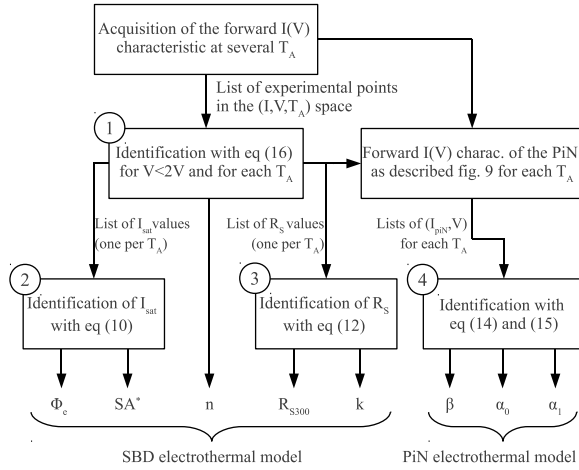


Fig. 7. Diagram of the model identification process. The identification steps are labeled 1 to 4.

probes on the top of the device, one on the chuck, the fourth being the chuck itself), resulting in a measurement accuracy better than 1%. Thanks to this 4-probe setup, the probe-to-die contact resistance has no influence on the measurements. The absence of current focusing effect was confirmed by a series of acquisitions, where the probes were placed in different locations of the die metal pad, with different contact pressures. All the results were identical. The silver adhesive thickness was also found to have a negligible effect on the measurements.

The pulse width is set to 900  $\mu\text{s}$  with a very low duty-cycle (<1%) to reduce self-heating while ensuring good measurement accuracy. With such a configuration, the average power dissipated by the device under test remains very low. Some tests showed that with this pulsed measurement, the results were not dependant on the adhesive thickness, nor on the pulse duration, providing it was shorter than 1 ms.

### B. Model identification

The identification process is summarized in figure 7. As it can be seen, the 8 parameters of the MPS model are identified in 4 different steps (always using a least-square method). The details of this process are described below.

The experimental data are visible in figure 8 (plain lines). To identify the model of figure 5(b), we consider two regions:

- below a forward voltage of 2 V, all the curves show a knee, followed by a straight line. This correspond to a unipolar diode (the straight line corresponds to the unmodulated series resistance  $R_S$ ), so we use this region to identify the SBD model.
- above this voltage, a “bend” is visible. This corresponds to the PiN diode conducting some of the forward current. In this region both diodes of figure 5(b) are carrying current.

For each temperature (corresponding to each single curve in figure 8), the parameters of the models are identified (step 1). Then the parameters which are temperature-dependent (such as  $I_{sat}$  or  $R_S$ ) are plotted versus the temperature, and their

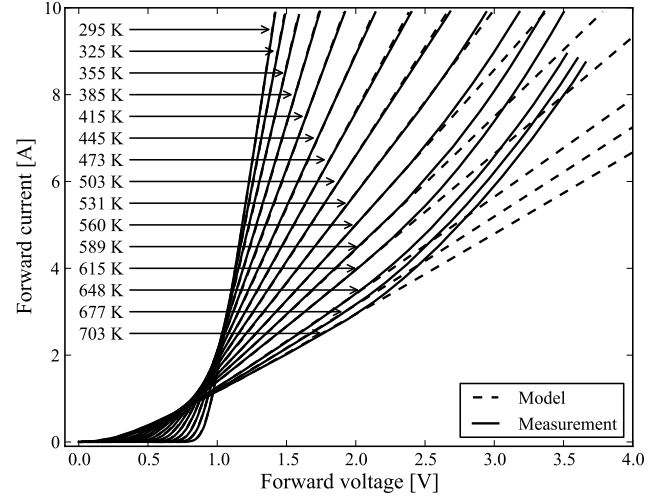


Fig. 8. Forward characteristic measured (plain line) and the SBD model identified from the measurements (dashed line)

TABLE II  
MODEL PARAMETERS IDENTIFIED

Model	Parameter	value
SBD	$n$	1.16
	$\Phi_e$	1.18 eV
	$SA^*$	5.66 $m^2$
	$R_{S300}$	0.043 $\Omega$
	$K$	2.95
PiN	$\alpha_0$	4.23 V
	$\alpha_1$	$-3.44 \cdot 10^{-3} V \cdot K^{-1}$
	$\beta$	$0.89 \Omega^{-1} V^{-1}$

temperature-dependence is itself identified (steps 2 and 3 for the SBD model, step 4 for the PiN). This results in a diode model of the form  $V = f(I, T)$  (or  $I = g(V, T)$ ). More details on the process are given below:

1) *SBD model*: From equations (9) and (11), it can be written:

$$I = I_{sat} \left[ \exp \left( \frac{q(V - R_S I)}{nkT} \right) - 1 \right] \quad (16)$$

This model has two variables ( $V$  and  $I$ ) and 3 parameters ( $n$ ,  $I_{sat}$  and  $R_S$ ). The parameter values are identified for each curve of figure 8 (step 1 in Fig. 7), and the corresponding models are plotted with a dashed line. It can be seen that a very good agreement was found, as experimental and calculated curves match very well at voltage below 2 V (where only the SBD is active).

2) *PiN model*: As written above, over a certain voltage, the current starts flowing through both the SBD and the PiN diode junctions. Therefore,  $I_{PiN} = I - I_{SBD}$ , with  $I_{SBD}$  being calculated (not measured) using the model of the SBD (identified in section IV-B1).

Once  $I_{PiN}$  is calculated, the identification of the parameters of (14) (step 4 in Fig. 7) is pretty straightforward, and gives satisfying results (see figure 9).

3) *Electro-thermal model of the forward-biased MPS diode*: Once a complete (SBD and PiN) model has been identified for

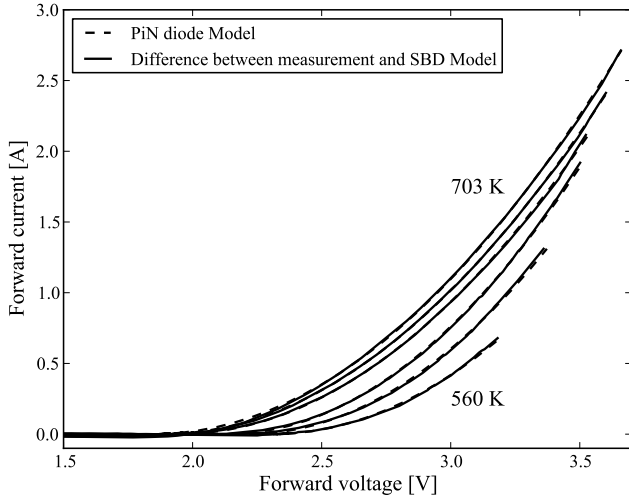


Fig. 9. PiN diode forward characteristics (plain line) and the model fitted (dashed line). The plain line is calculated as the difference between the MPS diode measured characteristic and the SBD model (i.e. the difference between the plain and the dashed lines in figure 8).

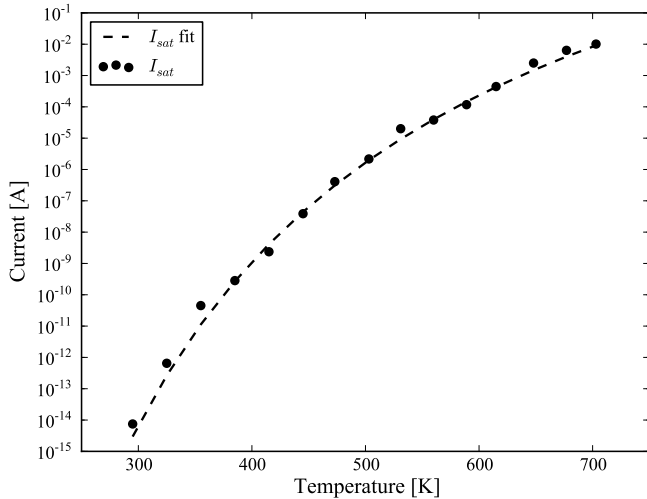


Fig. 10. Values of the  $I_{sat}$  parameter versus temperature for the SBD model, fitted with equation (10) (dashed line).

each temperature in the experimental data, the temperature-dependent parameters can be identified. This is the case for  $I_{sat}$  and  $R_S$  (equations (10) and (12), steps 2 and 3 in Fig. 7), and  $\alpha$  (15) (step 4).

Figures 10 and 11 represent the results of the fitting process for  $I_{sat}$  and  $R_S$  respectively. The table II summarizes all the parameters of the complete, temperature-dependent, MPS model. The experimental and simulated characteristics present a satisfying matching, as can be seen in figure 12.

## V. DISCUSSION

The models described above are of the form  $V = f(I, T)$ . As  $P = I \times V$ , it becomes possible to calculate  $P$  as  $P = I \times f(I, T)$ . This equation is plotted, for various values of  $I$  in figures 13(a) and (b). In the former, only the SBD part of the diode is considered (the PiN model is removed), while in the latter, the whole MPS model is used.

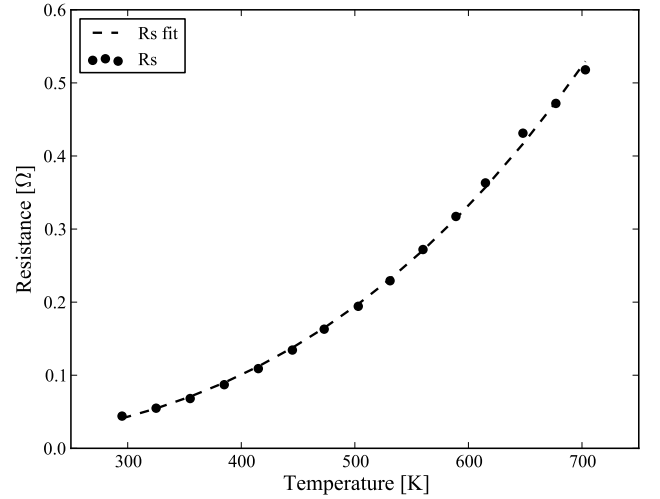


Fig. 11. Values of the  $R_S$  parameter versus temperature for the SBD model, fitted with equation (12) (dashed line).

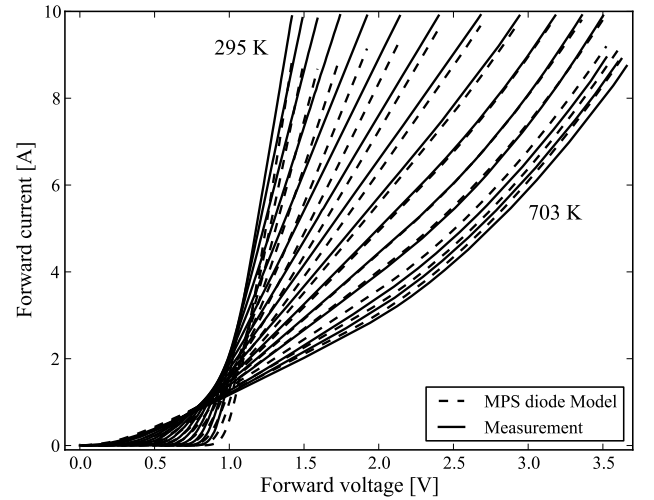
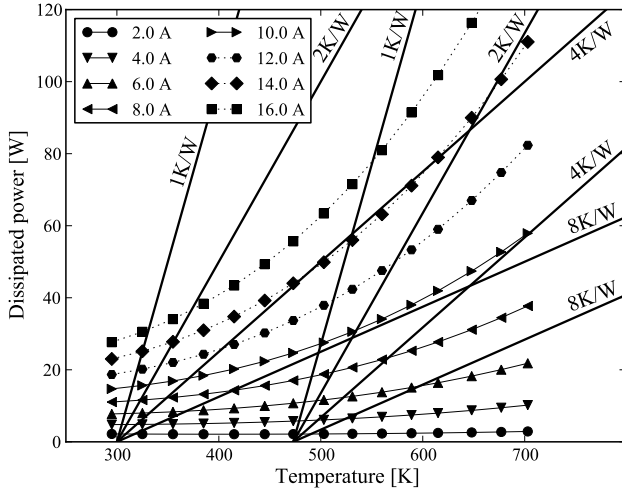


Fig. 12. Comparison between the forward characteristic (measured) and the electro-thermal model (identified). Temperatures are identical to those in fig 8.

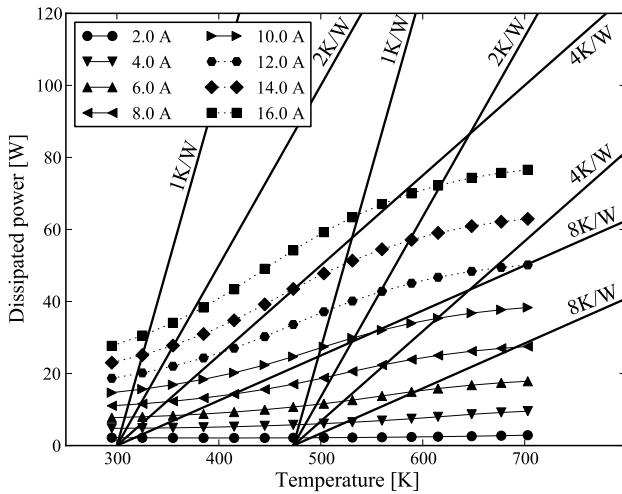
Also in figure 13 the characteristics of 5 cooling systems are plotted. Their  $R_{Th}$  values span between  $1 K \cdot W^{-1}$  (efficient cooling system) and  $8 K \cdot W^{-1}$  (reasonably efficient). These characteristics are given for two ambient temperatures ( $T_A$ ): 300 K (27°C) and 473 K (200 °C).

From these figures, the effect of the PiN diode is obvious: a pure SBD has a characteristic similar to the example in figure 3. For example, the 14 A curve and the 4 K/W characteristic (the one obtained for  $T_A = 300K$ ) have two points of equilibrium, one of them unstable. Also, it can be seen that a cooling system with a thermal resistance of 4 K/W is simply not sufficient to cool the diode operating at 16 A, even with an ambient temperature of 300 K. At an ambient of 473 K, 4 K/W is no longer enough to prevent device thermal runaway as soon as the forward current exceeds 10 A.

The characteristic of the MPS (figure 13(b)), in the opposite, does not show a similar quadratic shape. All the cooling system curves only have one intersect, offering a single, stable,



(a)



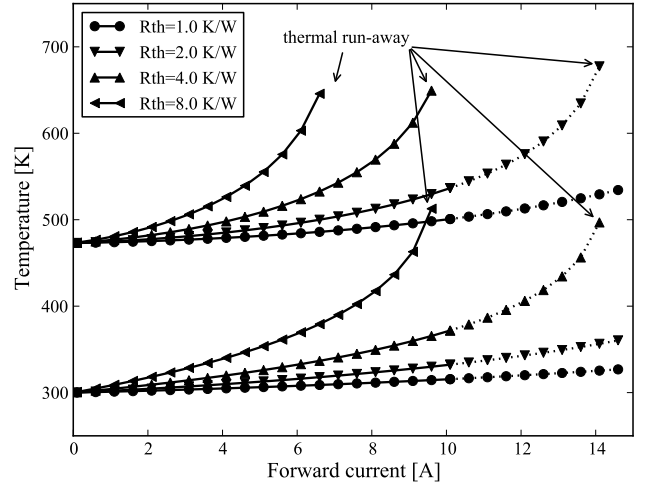
(b)

Fig. 13. Power that would be dissipated by the pure-Schottky Barrier Diode (a), depending on the temperature and the forward current; same plot for the MPS diode (b). Four thermal resistances (1, 2, 4, and 8 K/W) are superimposed on both graphs, for two ambient temperatures: 300 and 473 K (200°C). As the models were only identified with measurements up to 10 A, results higher than this value are displayed with a dotted line.

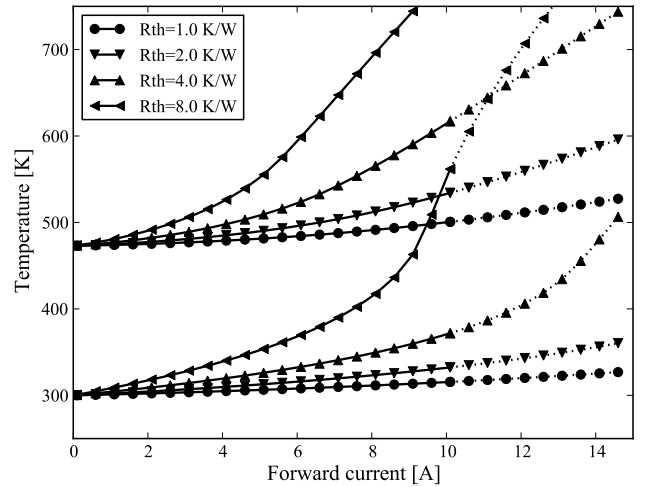
equilibrium. Moreover, as the device characteristics are much flatter, it can be estimated that even at  $T_A = 473$  K, a cooling system with a  $R_{Th}$  of around 3 K/W should be sufficient to allow operation of the diode up to 16 A (providing the diode can operate in the long term at 700 K, which is not the case with our sample).

Using the same diode model, another way of presenting the data is visible in figure 14: each point of a curve represents the stable equilibrium point reached for a given forward current. The curves are plotted for various  $R_{Th}$  (same values as figure 13), and for two ambient temperature values (300 and 473 K, the y-intersects). Once again, two dataset are shown: one for a pure SBD (figure 14(a)) and one for the complete MPS (figure 14(b))

As can be seen, with the SBD, in many cases a thermal equilibrium could not be found. For a thermal resistance of 1 K/W (and 2 K/W for an ambient of 300 K), the diode



(a)



(b)

Fig. 14. Steady-state junction temperature versus forward current, and for two ambient temperatures: 300 K and 473 K for the SBD (a) and for the MPS diode (b). The ambient temperature can be read as the temperature at  $I=0$ . As the models were only identified with measurements up to 10 A, results higher than this value are displayed with a dotted line.

would remain thermally stable over its entire current range. For higher thermal resistances, however, a thermal runaway could be triggered at current levels lower than the nominal current of the diode.

With the MPS (figure 14(b)), no such thermal runaway was found. However, it is interesting to note that both datasets are pretty similar, especially at the lowest temperatures. This is consistent with the static characteristic in figure 8 which shows a very good agreement between the SBD and the MPS characteristics at low temperature and/or lower current.

The bipolar (PiN) diode characteristic has a negative temperature coefficient (NTC), which means that its losses tend to decrease as the temperature increases. This tends to stabilize the unipolar (SBD) diode, which exhibits the opposite behaviour (positive temperature coefficient, PTC). The transition between PTC and NTC is therefore an important parameter for the thermal stability of the diode, which can be adjusted at the design stage [21].



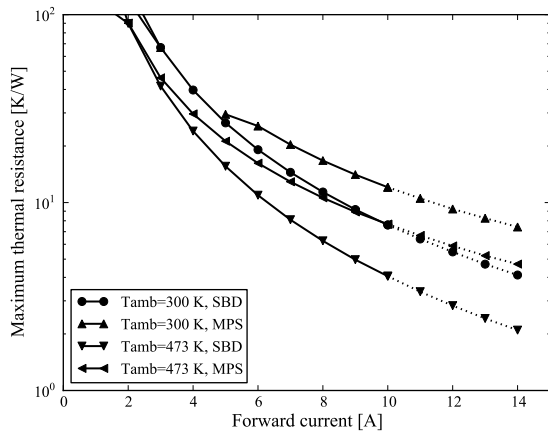


Fig. 15. Maximum value of  $R_{thja}$  versus direct continuous current. Above these curves, the device is either in runaway condition, or at a junction temperature exceeding 783K (the lowest temperature listed in table I). As the models were only identified with measurements up to 10 A, results higher than this value are displayed with a dotted line.

Another approach is to plot the maximum thermal resistance value that will yield to DTR for each forward current value (figure 15). A designer who wants to use this diode can use this graph to choose the appropriate cooling system.

Finally, it must be noted that in this study, the thermal conductivity of SiC was considered constant. This is a coarse approximation, as this conductivity (hence the cooling performance) tends to decrease dramatically as the temperature rises [22]. As a result, thermal runaway can be expected to occur even sooner than calculated. SiC, however, is only a small fraction of the power module thermal stack (figure 2), so a more detailed study would be needed to assess the influence of this non-linearity.

## VI. CONCLUSION

After the first generation of SiC SBDs was commercially introduced in 2001, it was found that they were prone to failure during current or voltage surges. The following generations were designed to be more robust by using a MPS structure.

In this paper we have shown that this MPS structure also makes the diodes more thermally stable, overcoming the limitations of pure SBD devices.

Some of the findings in [5] were confirmed, such as the existence of a risk of thermal runaway with some SiC power devices. It was also found that for a SBD operating in a mild ambient (300 K), this thermal runaway could occur at junction temperatures as low as 200°C.

However, the junction temperature is not a design variable. It is the consequence of the power dissipated in the device, of the performance of its cooling system, and of the ambient temperature. Therefore, we focused on these parameters to provide the engineer with guidelines for the use of SiC diodes. It was shown that a MPS diode does not exhibit a thermal runaway behaviour. It was also demonstrated that, providing that the thermal resistance is kept low enough (depending on the ambient temperature and the maximum current level in the diode), no runaway will occur even with a SBD, as shown in Fig. 15.

In some applications SiC devices are preferred in order to lower the size of the thermal management system (resulting in a higher  $R_{Th}$  and therefore a higher  $T_j$ ). For these applications, it must be stressed that pure SBD should be avoided, as they are at risk of thermal runaway. MPSs offer a much robust behaviour, although sufficient cooling must be provided to keep the nominal junction temperature at a level compatible with long-term operation.

A similar study is ongoing to evaluate the risks of thermal-runaway on other SiC devices such as the JFET or the BJT.

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## REFERENCES

- [1] D. Bergogne, H. Morel, D. Planson, D. Tournier, P. Bevilacqua, B. Allard, R. Meuret, S. Vieillard, S. Raël, and F. Meibody Tabar, "Towards an airborne high temperature SiC inverter," in *Proceedings of the Power Electronics Specialists Conference (PESC)*. IEEE, 2008.
- [2] T. Funaki, J. C. Balda, J. Junghans, A. S. Kashyap, H. A. Mantooth, F. Barlow, T. Kimoto, and H. Takashi, "Power Conversion With SiC Devices at Extremely High Ambient Temperatures," *IEEE Transactions on Power Electronics*, vol. 22, no. 4, pp. 1321–1329, jul 2007.
- [3] C. Buttay, D. Planson, B. Allard, D. Bergogne, P. Bevilacqua, C. Joubert, M. Lazar, C. Martin, H. Morel, D. Tournier, and C. Raynaud, "State of the art of High Temperature Power Electronics," in *Proceedings of the VIII Conference Thermal Problems in Electronics, microtherm 09*, Lodz, poland, jun 2009.
- [4] J. M. Hornberger, E. Cilio, R. M. Schupbach, A. B. Lostetter, and H. A. Mantooth, "A High-Temperature Multichip Power Module (MCPM) Inverter utilizing Silicon Carbide (SiC) and Silicon on Insulator (SOI) Electronics," in *Proceedings of the 37<sup>th</sup> Power Electronics Specialists Conference (PESC)*. Jeju, Korea: IEEE, Jun. 2006, pp. 9–15.
- [5] K. Sheng, "Maximum Junction Temperatures of SiC Power Devices," *IEEE Transactions on Electron Devices*, vol. 56, no. 2, pp. 337–342, feb 2009. [Online]. Available: [http://ieeexplore.ieee.org/xpl/freeabs\\_all.jsp?isnumber=4757346&arnumber=4752775&count=33&index=26](http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?isnumber=4757346&arnumber=4752775&count=33&index=26)
- [6] S. Pyo and K. Sheng, "Junction temperature dynamics of power MOSFET and SiC diode," in *Power Electronics and Motion Control Conference, 2009. IPEMC '09*. Wuhan: IEEE, may 2009, pp. 269–273.
- [7] C. Raynaud, D. Tournier, H. Morel, and D. Planson, "Comparison of high voltage and high temperature performances of wide bandgap semiconductors for vertical power devices," *Diamond and Related Materials*, vol. 19, no. 1, pp. 1 – 6, 2010. [Online]. Available: <http://www.sciencedirect.com/science/article/B6TWW-4XCJ4M2-1/2/76c76271c9345bf77d4fc29077179d2a>
- [8] R. Pérez, N. Mestres, D. Tournier, X. Jordà, P. Godignon, and M. Vellvehi, "Temperature Dependence of 4H-SiC JBS and Schottky Diodes after High Temperature Treatment of Contact Metal," *Materials Science Forum*, vol. 483–485, pp. 945–948, may 2005. [Online]. Available: <http://www.scientific.net/MSF.483-485.945>
- [9] R. W. Johnson, C. Wang, Y. Liu, and J. D. Scofield, "Power Device Packaging Technologies for Extreme Environments," *IEEE Transactions on Electronics Packaging Manufacturing*, vol. 30, no. 3, pp. 182–193, jul 2007.
- [10] N. Lundberg, M. Östling, C.-M. Zetterling, P. Tägtström, and U. Jansson, "CVD-based tungsten carbide schottky contacts to 6H-SiC for very high-temperature operation," *Journal of Electronic Materials*, vol. 29, pp. 372–375, 2000, 10.1007/s11664-000-0080-x. [Online]. Available: <http://dx.doi.org/10.1007/s11664-000-0080-x>
- [11] R. Stout, "Beyond the Data Sheet: Demystifying Thermal Runaway," *power electronics technology*, pp. 14–19, nov 2007. [Online]. Available: [www.powerelectronics.com](http://www.powerelectronics.com)
- [12] P. Friedrichs, "Compact Power Electronics due to SiC Devices," in *Proceedings of the Conference on Integrated Power Systems (CIPS 08)*, nuremberg, march 2008.
- [13] B. J. Baliga, *Power Semiconductor Devices*. Boston: PWS Publishing Company, 1997, ch. 4, pp. 128–197.

- [14] D. T. Morissette and J. A. Cooper, "Theoretical Comparison of SiC PiN and Schottky Diodes Based on Power Dissipation Considerations," *IEEE Transactions on Electron Devices*, vol. 49, no. 9, pp. 1657–1664, sep 2002.
- [15] J. Hilsenbeck, M. Treu, R. Rupp, K. Rüschemschmidt, R. Kern, and M. Holz, "Investigations on surge current capability of SiC Schottky diodes by implementation of new pad metallizations," *Materials Science Forum*, vol. 645–648, pp. 673–676, 2010.
- [16] M. Treu, R. Rupp, C. Tai, P. Blaschitz, H. J., H. Brunner, D. Peters, R. Elpelt, and T. Reimann, "A Surge Current Stable and Avalanche Rugged SiC Merged pn Schottky Diode Blocking 600V Especially Suited for PFC Applications," *Material Science Forum*, vol. 527–529, pp. 1155–1158, oct 2006.
- [17] L. Zhu and P. Chow, "Analytical Modeling of High-Voltage 4H-SiC Junction Barrier Schottky (JBS) Rectifiers," *IEEE Transactions on Electron Devices*, vol. 55, no. 8, pp. 1857–1863, aug 2008.
- [18] C. Raynaud, K. Isoird, M. Lazar, C. M. Johnson, and N. Wright, "Barrier height determination of SiC Schottky diodes by capacitance and current-voltage measurements," *Journal of Applied Physics*, vol. 91, no. 12, pp. 9841–9847, jun 2002.
- [19] F. Masszi, P.-A. Tove, K. Bohlin, and H. Norde, "Computer modeling and comparison of different rectifier (M-S, M-S-M, p-n-n+) diodes," *Electron Devices, IEEE Transactions on*, vol. 33, no. 4, pp. 469 – 476, apr 1986.
- [20] A. Strollo, "A new SPICE model of power P-I-N diode based on asymptotic waveform evaluation," *Power Electronics, IEEE Transactions on*, vol. 12, no. 1, pp. 12 –20, Jan. 1997.
- [21] P. Friedrichs and D. Stephani, "Unipolar SiC power devices and elevated temperature," *Microelectronic Engineering*, vol. 83, pp. 181–184, 2006. [Online]. Available: [www.elsevier.com/locate/mee](http://www.elsevier.com/locate/mee)
- [22] W. Janke and A. Hapka, "Nonlinear thermal characteristics of silicon carbide devices," *Materials Science and Engineering: B*, vol. In Press, Corrected Proof, 2010. [Online]. Available: <http://www.sciencedirect.com/science/article/B6TXF-50H149J-1/2/198d26aae8457ae2de937ef9fe6adfaf>



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