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Design of a Mixed-Signal Cartesian Feedback Loop for a Low Power Zero-IF WCDMA Transmitter

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Abstract— in this paper, an improved digital-stage design of a mixed-signal Cartesian Feedback loop for a zero-IF WCDMA transmitter is presented. The new transmitter architecture consists of an analog stage including filters, I/Q modulator, feedback I/Q demodulator and a digital stage which adjusts the phase misalignment around the loop. We propose an optimized CORDIC design for the digital part in order to improve the system operating frequency without increasing the silicon surface area. ASIC synthesis proves that using a not fully pipelined CORDIC architecture allows us to reach 230 MHz with system power consumption under 4.3 mw which is two times less than a fully analog system.

Keywords—Mixed-Cartesian feedback loop; WCDMA transmitter; CORDIC;

I. INTRODUCTION

Third generation wireless communication standard WCDMA uses non-constant envelope modulation techniques to increase spectral efficiency for high data rates [1]. These modulations require a high linear radio-frequency (RF) power amplifier (PA). Nevertheless, power efficiency is maximized when the PA operates at its non-linear region. The best solution consists in designing a moderately linear PA then employing an adequate linearization technique. Consequently, the amplifier operates as close as possible to saturation, maximizing the power efficiency while the linearization system maximizes the spectral efficiency. Many methods (analog or digital) are proposed to reduce the effects of nonlinearities like Pre-distortion, Post-distortion, Feedback and Feed-forward techniques [2]. Among these, Cartesian feedback loop (CFB) [3], which forms an alternative feedback technique, is an attractive solution for two reasons: first, it automatically compensates all process variations and secondly, its linearization process is applied to all components in the loop. Nevertheless, this technique has suffered from practical shortcoming; it needs a phase corrector to compensate delay around the loop. Furthermore, analog implementation of phase corrector is difficult to realize and highly area expensive [4].

In this paper, authors present a detailed study to improve the based solution discussed on [5] and propose a new optimized CORDIC solution in order to provide an accuracy of 1° for the phase estimation process, to reach the desired frequency and to reduce energy consumption. Due to the increasing demand of cost reduction, a Zero-Intermediate Frequency (Zero-IF) architecture avoiding the use of external filter has been chosen. Delegating the phase rotation

adjustment processing to a digital stage provides flexibility, higher integration and less area size than in full-analog architecture [3].

The paper is organized as follow. Section II presents Zero-IF transmitter with the CFB linearization loop and design consideration. Section III deals with implementation study of the digital stage. Section IV describes the proposed architecture and Section V shows implementation results such as system operating frequency, occupied area and power consumption for (CORE65LPSVT) ASIC targets.

II. MIXED CARTESIAN FEEDBACK TRANSMITTER

A. Cartesian Linearization Technique

The proposed linearization technique architecture based on a digital CFB implementation is made up of both analog and digital building blocks as shown in “Fig. 1”.

Quadrature baseband signals (I_{return} , Q_{return}) are directly up-converted to RF frequency (1.95 GHz) by mixers associated with a local oscillator [6]. The resulting RF signal is then strengthened by the power amplifier. In the feedback path, the PA output is attenuated, down-converted and filtered out. After converting analog signals to the digital domain using analog to digital converters (ADC), a phase adjustment is applied to I_{FB} and Q_{FB} in order to cancel phase rotation around the loop. Feedback signals are subtracted from the input quadrature components to provide return signals I_{return} and Q_{return} . These signals include the forward path non linearity. By loop effect, forward path non linearity is subtracted from input signals. Thus, input I/Q signals are pre-distorted to provide a linearized PA output.

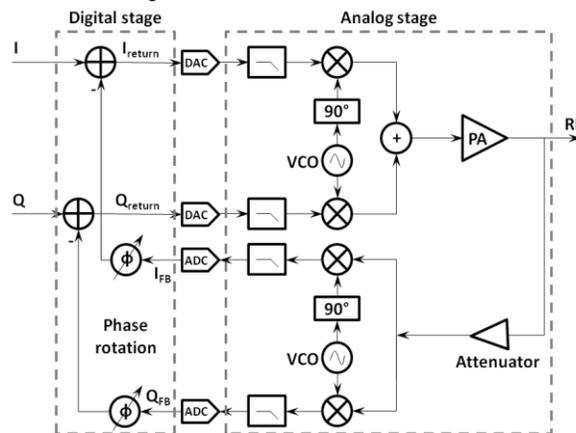


Figure 1. ZERO-IF WCDMA transmitter with mixed CFB Loop

Implementing the phase estimation and the vector rotation in digital domain relaxes linearity and in-band noise constraints compared to a fully analog circuit. By having an optimized and high integrated digital stage, we can reach lower power consumption than an analog design.

B. CFB Digital Stage and Design Consideration

The baseband loop filters in the feedback path results in a delay and symbol rotation after subtracting input and feedback signals [7]. Phase variations are cancelled by using the circular transformation given in (1), where θ represents the phase correction value.

$$\begin{bmatrix} I_c \\ Q_c \end{bmatrix} = \begin{pmatrix} \cos(\theta) & -\sin(\theta) \\ \sin(\theta) & \cos(\theta) \end{pmatrix} \begin{bmatrix} I_{fb} \\ Q_{fb} \end{bmatrix} \quad (1)$$

θ is calculated by comparing the forward path phase and the feedback path phase. Two architectures are evaluated for the circular transform implementation. The first architecture uses lookup tables (LUT) and a costly multiplier operator [5]. Even this solution does not introduce a large delay into the loop, it is highly expensive in terms of area occupation. In this paper, we'll focus on the second architecture which is based on a coordinate rotation digital computer (CORDIC) algorithm [8]. This iterative algorithm requires less area than a high complexity multiplier when the data path exceeds 10 bits. The pipelined CORDIC introduces latency in the CFB loop, a tradeoff between area occupation, latency and throughput is revealed. A fine tuning of input variables when implementing this architecture will lead to an optimal solution with 1° accuracy. For stability consideration, the delay in the loop is limited by the period of WCDMA data (T_{chip}) [9]. The digital-stage's operating frequency threshold is set to 220 MHz with respect to DAC and ADC characteristics Fig.1.

III. DIGITAL CFB IMPLEMENTATION

As already mentioned, the main task of the digital stage is to perform the vector rotation. Previously, the angular deviation has to be estimated. This angle is the difference between the phase of the feedforward channel I/Q and the feedback channel I_{FB}/Q_{FB} . Therefore, the digital CFB architecture is organized using three distinct blocks as shown in Fig. 2.

1. *Phase estimation*: to estimate the angular distortions in the two paths.
2. *Vector rotation*: to compensate phase error.
3. *Subtraction*: to predistort the input signals.

A. Phase estimation

Considering the phase estimation process, it is very important to notice that phase subtraction must be done "modulo 2π " to keep a same range of variation of the angle applied to the next block (vector rotation). It implies that the phase estimation block is divided into two sub-functional units;

- *Phase estimation* for both paths: computing atan function.
- *Modulo function*: to keep phase subtraction in $[-\pi, \pi]$.

1) "atan" function implementation

The implementation of the atan function can be done in several ways. The most trivial method was discussed in [5] and consists of using Lookup table. This solution seems to be over-sized and very costly in silicon consumption in comparison with other alternatives such as the CORDIC algorithm. This well-known iterative algorithm was designed for the first time by Jack E. VOLDER in 1959 [8]. It consists of two operating modes and it allows the calculation of trigonometric, hyperbolic and some linear functions by only using basic operations with respect to (2). It was subsequently improved in order to reduce computing cost and to facilitate implementations on an embedded target. For our application, we have used the rotation mode (RM) to perform vector rotation and the vectoring mode (VM) to compute atan function Fig. 2.

$$\begin{aligned} x_{i+1} &= x_i - y_i \cdot d_i \cdot 2^{-i} & d_i &= \begin{cases} -1, & z_i < 0 \\ +1, & \text{else} \end{cases} \text{ for : (RM)} \\ y_{i+1} &= y_i + x_i \cdot d_i \cdot 2^{-i} \\ z_{i+1} &= z_i - d_i \cdot \tan^{-1}(2^{-i}) & d_i &= \begin{cases} +1, & y_i < 0 \\ -1, & \text{else} \end{cases} \text{ for : (VM)} \end{aligned} \quad (2)$$

Atan function process consists of taking as input variables the two coordinates of the vector, initializing z_0 with zero and retrieving the corresponding phase value after performing nine iterations.

A scrupulous study depending on different hardware implementations of the CORDIC algorithm described in [10] has shown that adopting a fully pipelined design meets performance criterion. In fact, this architecture, as shown in Fig.3, has a small computation complexity and allows reaching high frequency. We note that calculation accuracy depends only on the number of the CORDIC iterations, thus nine iterations were needed to perform the same accuracy, 1° , as that achieved by the LUT based solution described in [5].

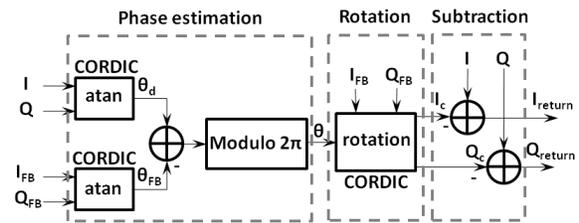


Figure 2. The Digital stage architecture

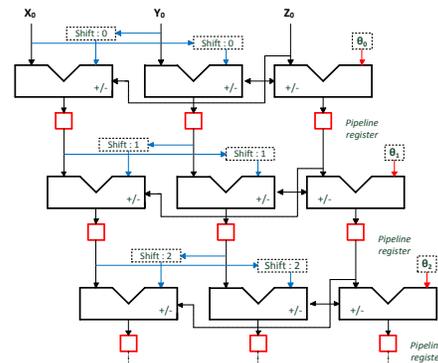


Figure 3. Fully pipelined CORDIC architecture

2) “Modulo” function implementation

Subtraction result must be standardized to avoid a possible overflow due to phase computing and to be suitable for the input of the next stage. Consequently, the “Modulo” function consists on calculating the remainder of the Euclidean division of the wanted angle by $K \cdot 2\pi$. A smart implementation of this function can be described by an algorithm organized as follows. First, a sign test is effectuated to benefit from the symmetry property of this function. Then the angle value is tested if it has exceeded a full circle turn. If so, 2π is subtracted from it and the test continues, else this value is retained as the output result.

B. Vector Rotation

The CORDIC algorithm performs the vector rotation without multiplier resources allocation. The rotation is computed using a serial of specific incremental rotation angles whose sum is equal to the desired angle of rotation. Each elementary rotation is performed only by using a shift- and - add operations. The same pipelined architecture is used. A simple initialization on its entries with the vector to rotate: namely IFB/QFB and the angle to perform, with respect to (2), is enough. Nine iterations were required to perform 0,1 % accuracy.

C. Subtraction

The subtraction function is simple enough to be implemented digitally. Indeed, it is necessary to calculate the two’s complement of the second operand and then use an adder.

IV. NOT FULLY-PIPELINED CORDIC DESIGN DESCRIPTION

ASIC synthesis results using the CORE65LPSVT technology have shown that with using a pipelined architecture we reach an operating frequency around 400 MHz. However, this result does not suit the system’s low power criterion. A smart alternative which decreases cost and meets system specifications consists on altering the fully pipelined architecture by reducing the number of registers used at each output stage. We notice that this adjustment should not decrease operating frequency under 220 MHz in order to meet DAC and ADC constraints. Starting from a non-pipelined architecture, a register is added after each arithmetic unit. An FPGA target was used to assess the performance of the implemented modules.

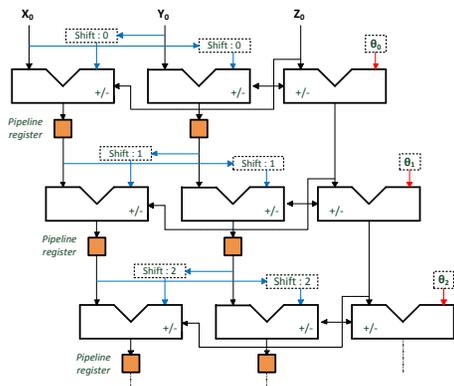


Figure 4. Not fully-pipelined CORDIC architecture for the vectoring mode

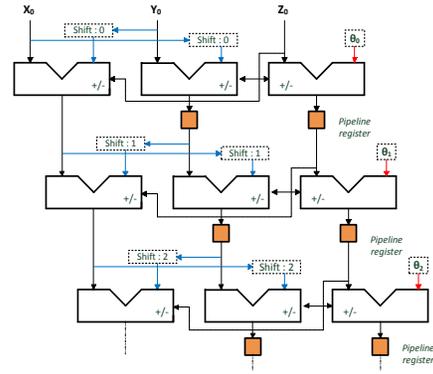


Figure 5. Not fully-pipelined CORDIC architecture for the rotation mode

By trying all possible configurations, it was concluded that the best is to reduce the registers number of each stage down to two. The choice of these registers depends on the CORDIC’s operating mode. When performing the vectoring mode, the best configuration is to store the values y_n and x_n in different registers at each output stage as mentioned in Fig. 4. However it is more appropriate to store y_n and z_n when performing the CORDIC’s rotation mode Fig.5.

In the next section, ADS simulation of the analog part and ASIC synthesis results of the whole digital stage will be discussed.

V. SYSTEM VALIDATION AND ASIC SYNTHESIS RESULTS

All given results in this section were obtained by performing ASIC synthesis.

A. Linearization Technique Validation

All building blocks making the digital stage have been designed and simulated in hardware descriptive language (HDL) with ModelSim® and have been characterized stand-alone. Now, we are able to realize system level simulations in order to validate the overall architecture, why for ADS Software have been used. Fig. 14 and Fig. 15 depict the output spectrum of the PA with and without CFB technique for a same output power. This last exhibits clearly a decrease of the distortions on the adjacent channel due to CFB loop (Adjacent channel power ratio (ACPR) receives an improvement of 22dB at 5MHz from the carrier). In fact comparing with the mask defined by the standards UMTS, the output spectrum for a Zero-IF architecture is out of specifications, in opposite with the output spectrum of the CFB loop.

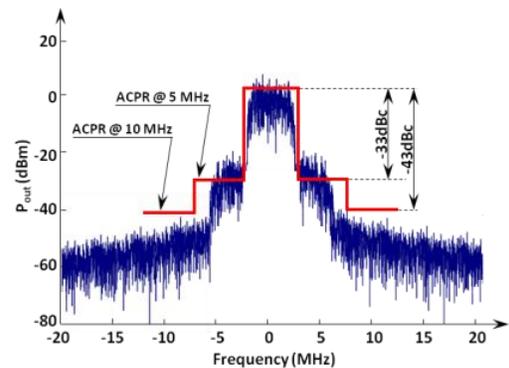


Figure 6. Output spectrum without CFB (Left) and with CFB (Right)

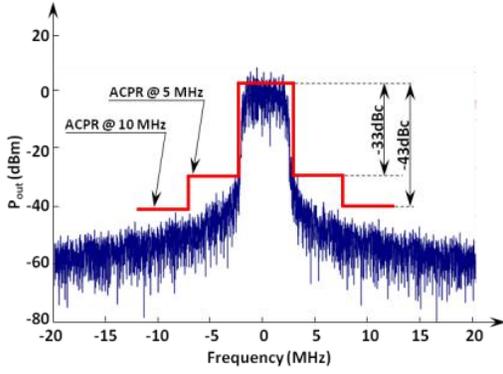


Figure 7. Output spectrum without CFB (Left) and with CFB (Right)

B. Hardware implementation results

Simulation result of the optimized CORDIC solution is shown in Fig 8. The predistorted signal generated using floating simulation is illustrated by using a dotted line whereas that obtained using a HDL implementation is represented by continuous line, as shown in Fig 8.

Table I summarizes ASIC synthesis results on 65nm low power technology (CORE65LPSVT) in terms of area occupation and energy consumption for our two considered solutions. Two power types are presented: the dynamic power which depends on working frequency and the leakage power whose consumption depends only on the occupied surface area. ASIC synthesis of the proposed architecture shows that a frequency of 232 MHz is reached with lower power consumption than the fully pipelined solution.

We note that power consumption of the improved design is reduced by **35 %** with respect to system constraints. We note also that the obtained surface area occupation is **22 %** less than the fully-pipelined solution Fig.9.

TABLE I. SYNTHESIS RESULTS OF THE IMPROVED ARCHITECTURE

	Fully- pipelined solution	Our solution	Saving
Occupation (μm^2)	51452	40165	22 %
Leakage power (μW)	49,0	38,9	20.61 %
Dynamic power (μW)	11415,0	4170,0	63.47 %
Power consumption ($\mu\text{W}/\text{MHz}$)	28,586	18,512	35,3 %
frequency (MHz)	400	232,6	---

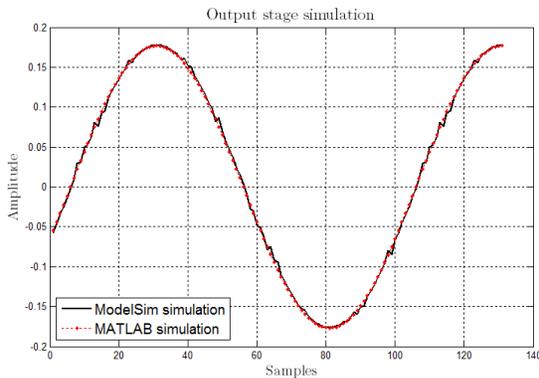


Figure 8. Output stage simulation

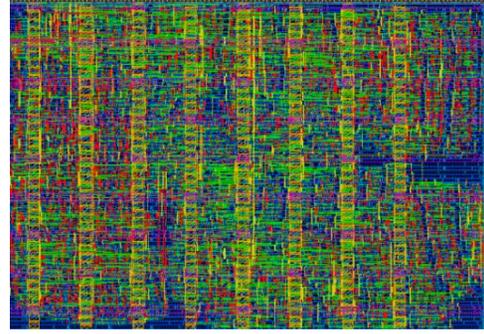


Figure 9. Die area of our digital stage ($228,085 \times 215,030 \mu\text{m}^2$)

It is important to notice that the proposed solution is two time less energy than the full-analog one; **4.3 mW** for our solution compared to **8.8 mW** in the case of full-analog architecture [3].

VI. CONCLUSION

In this paper a Cartesian feedback direct conversion transmitter with digital processing stage has been presented and evaluated for the WCDMA standard. This mixed-signal architecture is two time less energy than the full analog architecture. Moreover the proposed design allows the linearity constraints on the subtractor, on the phase corrector and also on the DACs to be relaxed.

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