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# Study of the impact of hot carrier injection to immunity of MOSFET to electromagnetic interferences

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## Abstract

This paper presents an original study about the effect of hot carrier injection stress on the DC offsets induced by electromagnetic interferences (EMI) on a nanometric NMOS transistor, which is one of the major sources of failures in analog circuits. Measurements and simulations based on a simple model (Sakurai-Newton model) of fresh and stressed transistors are presented showing significant variations of EMI-induced DC shifts of drain current.

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## 1. Introduction

Recent publications have shown that integrated circuit lifetime tends to decrease with CMOS nanometric technologies because transistor failures, such as Negative Bias Temperature Instability (NBTI), Hot Carrier Injection (HCI) or Time Dependent Dielectric Breakdown (TDDB) arise prematurely [1]. Even if the degradation mechanisms do not lead systematically to hard failures, they can degrade circuit performances and reduce the margins to external disturbances, e.g. such as electromagnetic interferences (EMI). Several recent studies have shown that device aging could lead to significant change in circuit immunity to EMI [2,3] making necessary to understand the link between time-dependent transistor degradations and circuit immunity.

A typical source of failures of analog circuits exposed to electromagnetic interferences (EMI) is

linked to EMI-induced offsets [4,5]. Due to their nonlinear characteristics, transistors rectify the voltage fluctuations produced by EMI coupling on their terminals, resulting in DC shifts that affect circuit operation points and performance degradations.

The following paper proposes a study of the impact of a typical degradation mechanism of MOSFET (HCI) on EMI-induced offset at transistor level. Comparisons between measurements and simulations of drain current shifts induced by EMI coupling are presented before and after HCI stress of NMOS transistor in CMOS 90nm technology. Transistor models are based on the Sakurai-Newton model [6]. This simple model is able to take into account short channel effects of deep submicron transistors with a reduced set of parameters and has been successfully used to predict delay and current consumption in digital circuits. In this paper, we propose to extend the use of this model to take into

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account HCI degradations and simulate the EMI-induced offset of drain current. In the first section of the paper, the test set-up is presented. The Sakurai-Newton model and the model extraction procedure are described in the third section. Comparisons between measurement and simulation of EMI-induced offsets are given in the last section.

## 2. Device under test and test set-up description

### 2.1. Device under test description

The device under test in this paper focuses on a set of NMOS transistors designed in 90nm Freescale CMOS technology with thick oxide option. The gate length and width of NMOS are 1.52 $\mu$ m and 10  $\mu$ m. The nominal bias voltage is equal to 3.3 V.

#### 2.1. Hot carrier injection test

With technology moving into deep submicron level, hot carrier injection becomes one of the major failure mechanisms. Among different type of failure in HCI, we chose the mechanism: Drain Avalanche hot-carrier injection, since it causes the worst degradation in the normal operating temperature range. High drain voltage results in very high electric fields near the drain, which accelerate channel carriers into the drain depletion region. This is known as impact ionization, which reduces the transconductance and saturation current, and shifts the threshold voltage.

To analyze the impact of HCI and generate maximum hot carriers, the appropriate gate and drain voltages need to be determined in advance as part of the stress conditions. The stress condition should be defined as follows. The  $V_{DS}$  stress voltage should be equal to the drain-to-source voltage breakdown minus 0.5 V. The  $V_{GS}$  stress voltage is obtained by measuring the substrate current ( $I_{SUB}$ ) while the  $V_{GS}$  is swept with the  $V_{DS}$  set to  $V_{STRESS}$ . The  $V_{GS}$  stress voltage is defined as the optimal gate voltage for which  $I_{SUB}$  is maximum.

To prevent from transistor breakdown risks, the gate and drain voltages are limited to 1.5 times of nominal voltage, i.e. 5V. The  $I_{SUB}$  characterization is shown in Fig. 1, the  $V_{GS}$  stress voltage is equal to 1.9V.

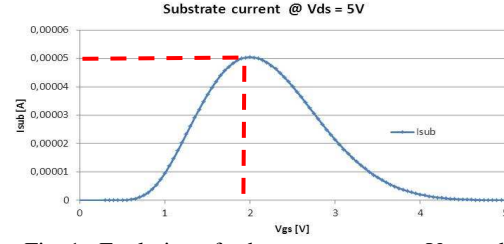


Fig. 1. Evolution of substrate current vs.  $V_{GS}$  and extraction  $V_{GS}$  stress voltage

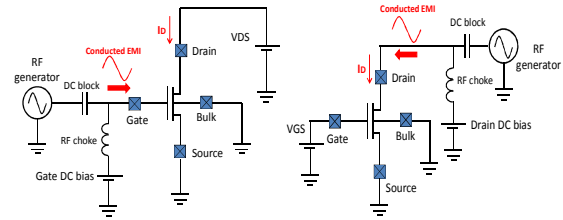


Fig. 2. Test set-up to measure EMI-induced DC shift on drain current for conducted injection on gate (Right) and on drain (left)

### 2.2. Set-up for Conducted injection of EMI

The experimental setup is described in Fig. 2. Interference is superposed on DC bias signal by a decoupling network (to prevent RF disturbances flowing into DC supply) and couple to the NMOS transistor terminal: gate or drain. The interference is a sinusoidal signal generate by RF generator. The mean drain current  $I_{DS}$ , has been measured by a DC current meter with 100nA accuracy. The bulk and source of the NMOS are connected to the ground.

## 3. Modelling with Sakurai-Newton model

### 3.1. Sakurai-Newton Model description

Nowadays, the BSIM4 model [7] has been widely used by semiconductor and design companies for IC design and device modelling. However for the confidential reason and too complicate to extract the parameters (more than 300 parameters), it always difficult for user to research with this model. We choose a comprise model: Sakurai-Newton model [6]: which has only six main parameters and has a good accuracy for short channel device (see Eq. 1).

$$V_{DSAT} = K^*(V_{GS} - V_{th})^m$$

$$I_{DSAT} = B^*(V_{GS} - V_{th})^n$$

when  $V_{GS} < V_{th}$   $I_D = 0A$

when  $V_{GS} \geq V_{th}$  : for  $V_{DS} < V_{DSAT}$

$$I_D = I_{DSAT}^*(1 + \lambda V_{DS})^*(2 - V_{DS}/V_{DSAT})^*(V_{DS}/V_{DSAT})$$

$$\text{for } V_{DS} \geq V_{DSAT} \quad I_D = I_{DSAT} * (1 + \lambda V_{DS}) \quad (1)$$

$V_{GS}$  and  $V_{DS}$  are the gate-to-source and the drain-to-source voltages.  $V_{th}$  denotes the threshold voltage,  $V_{DSAT}$  the drain saturation voltage and  $I_{DSAT}$  the drain saturation current.  $K$  and  $m$  control the linear region characteristics while  $n$  determine the saturated region characteristics.  $B$  is related to the transconductance,  $\lambda$  is the finite drain conductance in the saturated region.

### 3.2. Modelling NMOS transistor before and after HCI stress

The extraction of the six parameters uses a global optimization strategy: firstly a Matlab program executes the extraction algorithm defined in [6] to find the optimal set of parameters to fit the model on measured IV curves. Then, these parameters feed a SPICE model under ADS to improve manually their tuning. Our objective is simulating the behaviours of transistor before and after ageing to evaluate the degradation of its immunity to EMI. So if the model can well reproduce the DC behaviour of transistor during ageing and under EMI, even if these “fitting” parameters might yield values that are not consistent with their physical intent, we can use them just to predict the variation.

The model parameters extract from measurement for fresh and aged component are listed in Table 1.

Table 1  
*Sakurai-Newton Model parameters before and after HCI stress*

| NMOS  | $\lambda$ | $V_{TH}$ | $n$   | $B$      | $m$    | $K$   |
|-------|-----------|----------|-------|----------|--------|-------|
| Fresh | 0.014     | 0.915    | 1.400 | 0.000621 | 0.7928 | 1.137 |
| Aged  | 0.017     | 1.032    | 1.494 | 0.000467 | 0.7753 | 1.063 |
| Var.  | +21%      | +13%     | +7%   | -20%     | -2%    | -6%   |

The model parameters are compared in the list that after 2000s HCI stress, the transconductance ( $B$ ) reduce about 20%, meanwhile the threshold voltage ( $V_{th}$ ) and channel length modulation ( $\lambda$ ) increase about 13% and 21% respectively.

The comparison of measurement and simulation for fresh component is shown in Fig.3. After 2000 seconds HCI stress NMOS's IV curve has obvious degradation (see Fig.4). The maximum saturation current decrease 19.6% (see Fig.5). The models fit well the measurement for both fresh and aged component.

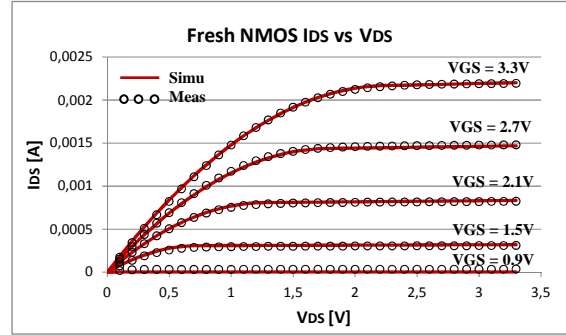


Fig. 3. Comparison of simulation and measurement for fresh NMOS,  $I_{DS}$  vs.  $V_{DS}$

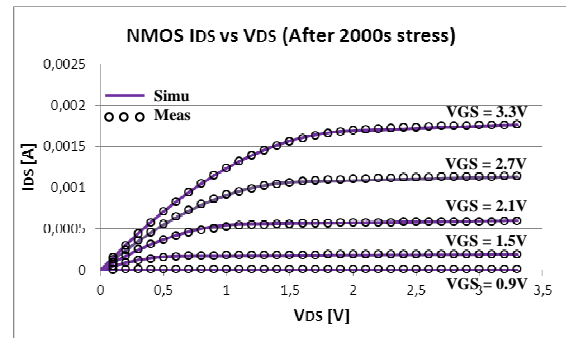


Fig. 4. Comparison of simulation and measurement for NMOS after 2000s HCI stress,  $I_{DS}$  vs.  $V_{DS}$

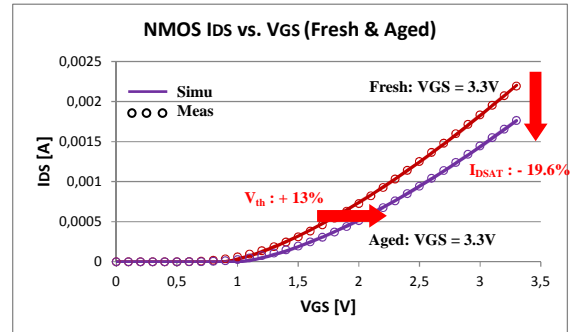


Fig. 5. Comparison of fresh and aged NMOS IV curve ( $I_{DS}$  vs.  $V_{GS}$ ) for measurement and simulation

## 4. Measurement and simulation of EMI-induced DC offsets

### 4.1. EMI coupling on NMOSFET Gate

We apply a set of EMI at 1MHz with different amplitudes ( $V_{emi}$ ) ranging from 0.5 to 0.7V on the gate of NMOS.

$V_{GS}$  is biased at 2.1V. The average value of  $I_{DS}$  is measured at drain of NMOS before and after the HCI stress. The EMI-induced DC shift is extracted by

computing the difference between average drain current with and without EMI. Fig. 6 presents the variation of the EMI-induced DC shift vs.  $V_{DS}$  and the EMI amplitude. The DC offset on drain current depends on transistor regime and increases with EMI amplitude. The EMI coupling on gate with amplitude of 0.7V can induce DC offsets on drain current which reach 6% of the current value for fresh component.

The same measurement was done after HCI stress. The comparisons between simulation and measurement for fresh and aged component were shown in Fig.6. The simulation can show a right tendency of variation, and have a good approximation to measurement.

After HCI stress, with the same EMI, stressed component has a larger DC drift than fresh one in the saturation regime. In linear regime, the DC offset is reduced, which can be explained by reducing of  $\lambda$  and increasing of the  $V_{th}$ . The maximum DC offset varies from  $-29.7 \mu A$  to  $-16 \mu A$ , so decrease 47% after HCI stress. In saturation regime, the maximum DC offset varies from  $45 \mu A$  to  $49 \mu A$ , i.e. an increase of 9 % of EMI induced DC offset on transistor drain current, since the enhanced 21% of  $\lambda$  plays the leading role. By comparison IV curves in Fig.5 and Fig.6, the drain saturation voltage shift from 1.3V to 1.12V, due to the augmentation of threshold voltage and slight reduction of  $m$  and  $K$ .

#### 4.2. EMI coupling on NMOSFET Drain

We apply a set of EMI at 1MHz and different amplitudes on the drain of NMOS,  $V_{DS}$  is biased at 2.1V. The same procedure is used to measure the EMI-induced DC offset. Fig. 7 presents the EMI-induced DC shift before and after the HCI stress.

The same measurement was done after ageing, the comparison between simulation and measurement for a fresh and an aged component were shown in Fig.7. EMI induced DC offsets appear for both linear and saturation regime, and became obvious when  $V_{GS} > V_{DS}$ . It can be explained by the reduction of mobility and increase of  $V_{th}$ . When  $V_{GD} > 0$ , with the effect of channel modulation reduced, the role of augmentation of  $\lambda$  will be weakened. The absolute value of DC offset increases with EMI amplitude. Conversely to EMI injection on gate, the DC offset induced by EMI coupling on the drain varies from  $-89.8 \mu A$  to  $-54.5 \mu A$ , i.e. a decrease of 39.3 % of EMI induced DC offset on transistor drain current after HCI stress.

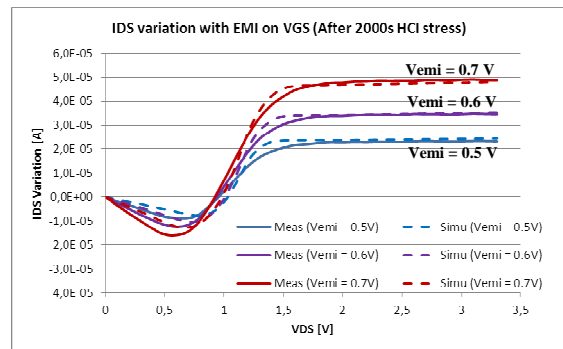
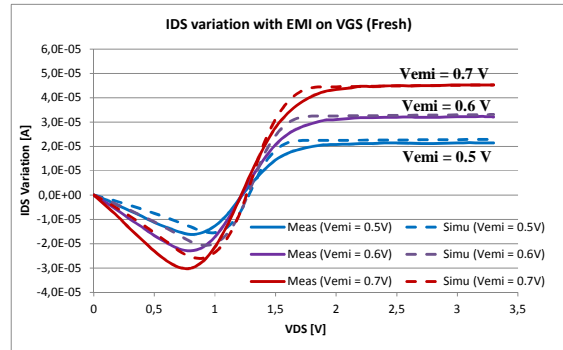


Fig. 6. Comparison of simulation and measurement of  $I_{DS}$  variation when apply EMI on Gate for a fresh component (up); and an aged component (down);

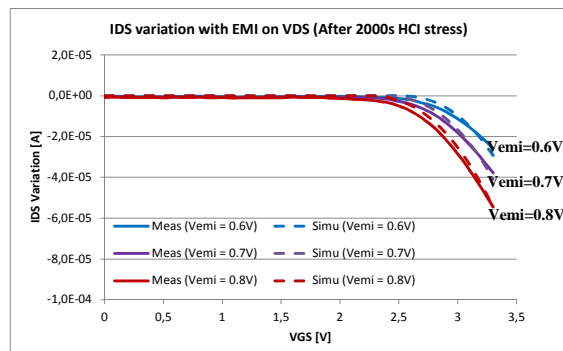
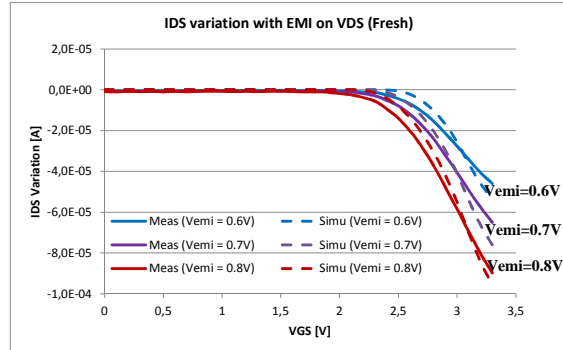


Fig. 7. Comparison of simulation and measurement of  $I_{DS}$  variation when apply EMI on Drain for a fresh component

(up); and an aged component (down);

## 5. Conclusion and discussion

In this paper, the first results of a study about the impact of HCI on circuit immunity have been presented. The study is focused on the DC offset induced by EMI coupling on transistor terminals, which is a common source of failures of analog circuits exposed to EMI. The measurements have shown that EMI-induced DC shifts can change after device degradations: the drain current shift is reduced in both linear regime and saturation regime when EMI coupling on the drain. When the gate is exposed to EMI, the drain current decrease in linear regime, while it is enhanced in saturation regime. Further studies are on-going to measure the variation of EMI-induced DC shifts on different geometric transistors and on thin oxide MOSFET for both NMOS and PMOS node, and validate the HCI impact on simple structures such as current mirror and common source/drain amplifiers.

Moreover, the Sakurai-Newton model has been successfully used in this preliminary work to predict the variation of EMI-induced DC shift after HCI stress. The good correlation with measurement encourages us to use this simple model to take into account device degradations and to simulate the effects on the immunity to EMI of larger circuits.

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