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Construction and Evaluation of the Susceptibility Model of an Integrated Phase-Locked Loop

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Abstract— Developing integrated circuit immunity models has become one of the major concerns of integrated circuits suppliers to predict whether a chip will pass susceptibility tests before fabrication and avoid redesign process. This paper presents the development process of the susceptibility model an integrated phase-locked loop to harmonic disturbances up to 1 GHz.. The model construction is based on basic circuit information and S parameter measurements. An evaluation of the model accuracy is ensured by the characterization of internal voltage fluctuations with an on-chip sensor.

Keywords- susceptibility; integrated circuit; phase-locked loop; on-chip measurement; modeling

I. INTRODUCTION

These last years, the concerns about electromagnetic compatibility (EMC) of integrated circuits (emission and susceptibility issues) have grown considerably. Susceptibility to electromagnetic interferences (EMI) has become one of the major issues for all circuit classes (digital, analog, RF, power). In order to reduce IC redesign costs and time-to-market, the evaluation of non-compliance risks during design stage is critical. A significant research effort was dedicated to the prediction of power integrity and parasitic emission in large scale circuits at early design phases [1]. A first standard immunity model called Integrated Circuit Immunity Modeling (ICIM) has been proposed since 2008 [2] and some publications have presented examples of immunity model development [3] [4] [5]. However, simulation and modeling of IC susceptibility is more challenging and the definition of a generic immunity model needs a large collection of case studies in order to cover all circuit classes.

This paper is a contribution to the development of an IC susceptibility model, applied on a common analog block used in mixed-signal circuit and particularly sensitive to EMI: a phase-locked loop (PLL). The proposed model followed the formalism suggested in ICIM. The model is made of two blocks: the passive distribution network (PDN) which describes the coupling of external interferences on sensitive nodes of the circuit, and the immunity behavior (IB), which indicates the failure presence, nature and/or probability for a given amount of coupled noise. In the paper, the construction of both parts is based on circuit information and external measurements such as S parameters. However, the characterization of internal voltage fluctuation induced by

external EMI coupling can have a significant importance to validate both model parts. In this paper, on-chip noise measurements by wideband voltage sensors placed on various locations of PLL power distribution network are presented to validate or evaluate the limit of the IC susceptibility model.

The paper is organized as follows: section II describes the structure of the studied PLL and the on-chip sensor, and then the conducted susceptibility test set-up. Section III describes the construction of PDN block based on S parameter characterization of the circuit. On-chip noise measurements are performed to validate the ability of the model to predict the coupling of external conducted EMI accurately. Section IV presents the development of IB block. On-chip noise measurements are also performed to correlate the amount of internal voltage fluctuations and failures, and verify if the same sensitivity level can be predicted by the model.

II. PRESENTATION OF THE CASE STUDY

A. Phase locked loop description

The proposed study is focused on a PLL designed in the 0.25 μm SMARTMOS from Freescale Semiconductor (Toulouse - France). Fig. 1-a presents the PLL schematic. The PLL is based on a first order filter, and made of three sub-blocks (phase detector, voltage-controlled oscillator (VCO) and frequency divider) which have separated power supply pairs. The VCO is a delay-controlled ring oscillator (Fig. 1-b), designed to operate nominally at 112 MHz, the frequency divider divides by 4 the VCO frequency. In the following tests, the reference signal applied on PLL input has a frequency of 24 MHz.

The PLL power distribution network is unconventional but the separation of power supplies of each sub-block has been chosen to characterize and model internal coupling between different power supply domains. The different power supply pairs are written $V_{\text{DD}}\text{VCO}/V_{\text{SS}}\text{VCO}$ for the VCO, $V_{\text{DD}}\text{Ph}/V_{\text{SS}}\text{Ph}$ for the phase detector and $V_{\text{DD}}\text{Div}/V_{\text{SS}}\text{Div}$ for the frequency divider.

B. Conducted susceptibility measurement set-up

The test chip is packaged in a 64 pin Quad Flat Package and attached to an EMC test board dedicated to conducted susceptibility characterization based on IEC 62132-4 Direct

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Power Injection (DPI) [6]. VCO are extremely sensitive to power supply fluctuations which increase the phase noise level. Although all the sub blocks of the PLL would be affected by conducted interferences in a real case, we focus the modelling work on the coupling on VCO power supply. Thus, harmonic disturbances are applied on the power supply pin of the VCO called V_{DDVCO} as shown on Fig. 2. The noise coupled on VCO power supply induces jitter on the PLL output period or period jitter, which is monitored by a digital storage oscilloscope (DSO). The maximum allowed deviation of PLL period is set to 2 ns.

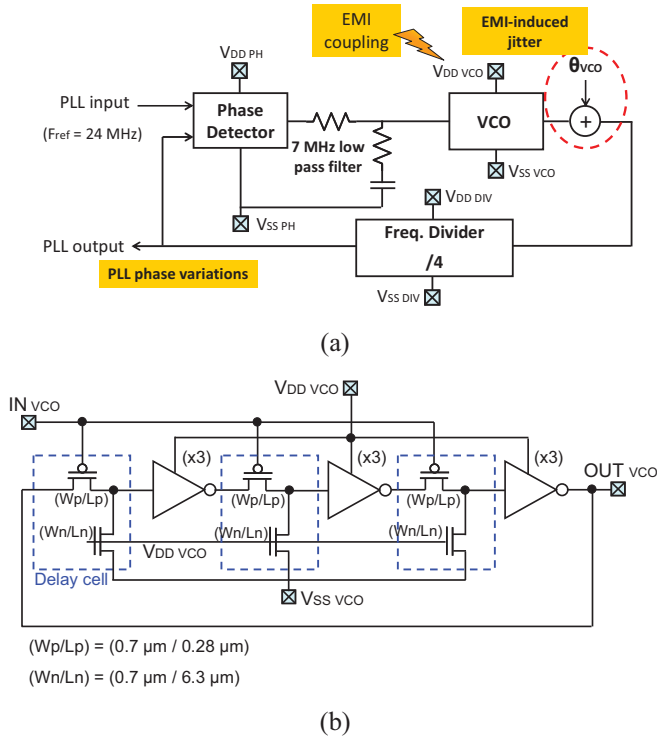


Figure 1. (a) PLL and (b) VCO schematics

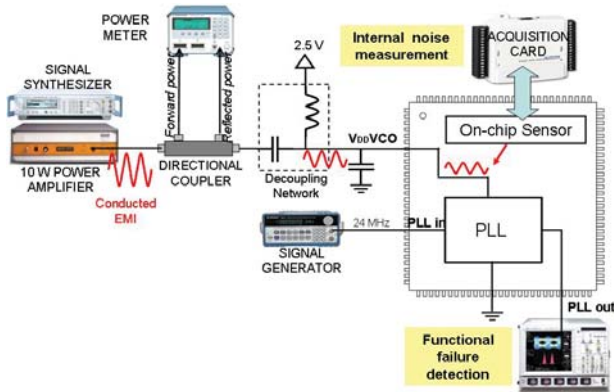


Figure 2. Conducted susceptibility test set-up

C. On-chip voltage sensor

Three on-chip voltage sensors are placed on the VCO, the phase detector and the divider power supplies in order to characterize EMI coupling within the circuit PDN and extract

the actual sensitivity level of each sub-block. The sensor is based on a wideband sample and hold (S/H) cell that directly probes the voltage on a given internal node (Fig. 3). As shown on [7], the bandwidth of the sensor reaches 1.5 GHz.

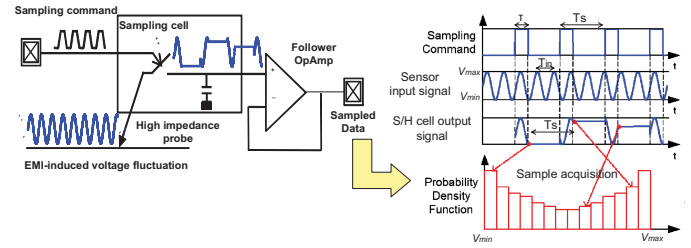


Figure 3. On-chip voltage sensor and random acquisition of EMI-induced voltage fluctuation

Although the sensor operates in sub-sampling conditions, the sensor is able to reconstruct the time waveform of the measured signal with a very small time step by post-processing if the sensor acquisition is synchronized with the measured signal and if the output amplifier does not filter the S/H output signal [8]. However, as we are only focused on voltage fluctuation amplitude, the set-up can be simplified. The S/H cell is not synchronized on the external EMI so the acquisition of the internal voltage fluctuation is randomly performed. The statistical distribution of the voltage fluctuation, its amplitude and standard deviation can be extracted.

The on-chip sensor has been carefully designed to isolate them from external disturbances coupled on other blocks of the test chip:

- the sensor power supply is separated, carefully decoupled and internally regulated by a built-in regulator
- all the devices of the sensor are isolated from the P substrate by a buried N layer and dielectric-filled trenches on the sides, in order to prevent from interference coupling on the sensor by the substrate

III. POWER DISTRIBUTION NETWORK MODELING

The first essential part of the susceptibility model is the power distribution network (PDN). The PDN describes how the incoming EMI couple on the internal nodes of the circuit. First, the PDN model is built from S parameter measurements made between the different power supply pins of the PLL. Then, on-chip sensor measurements are done to test the validity of the PDN model.

A. S parameter characterization of the PDN and equivalent model extraction

The PDN model of the PLL is an impedance network which links the power and ground pins of the PLL sub-blocks. Each sub-block counts one power supply and two ground pins. Moreover, the PLL input-outputs are biased by a dedicated power supply which can interact with the PLL PDN. Thus, the PLL PDN counts a total of 11 pins.

A specific test board has been designed to extract the impedance network of the PLL PDN by 2-port S parameter measurements. The circuit is connected to a vector network analyzer (VNA) by high frequency GS probes (Fig. 4). Probes are connected to PCB pads placed as close as possible to the circuit under test. All the measurement configurations between each pin of the PLL PDN are possible, so package inductances, block equivalent capacitances, substrate coupling ... can be extracted from measurements.

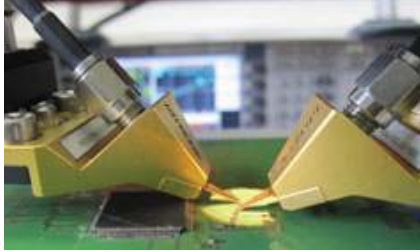


Figure 4. PLL PDN model extraction by S parameter measurements

Fig. 5 presents the PDN model extracted from S parameter measurements. For readability purpose, only some element values are reported on the schematic. The protection elements between the different power supply and ground rails are omitted because they were not triggered during susceptibility tests, except their equivalent capacitances. Otherwise, they should have been added in the model. Fig. 6 presents comparisons between S parameter measurements and simulations obtained from the extracted model. The comparisons between measurement and simulation show a good agreement up to 1 GHz.

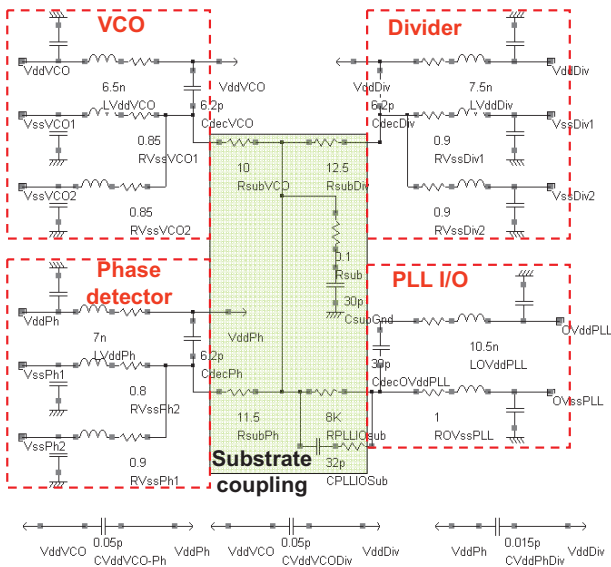


Figure 5. PLL PDN impedance model extracted from S parameter measurements

B. Characterization of noise coupling on VCO power supply

An on-chip sensor has been placed on the $V_{DD}VCO$ in order to characterize the amount of noise coupled on this node and validate the PDN model. The PLL PDN filters the voltage

fluctuation induced by the conducted EMI. The filtering effect can be expressed by a transfer function that relates the induced voltage fluctuation ΔV to the amount of incoming disturbance. In DPI test, the conducted disturbance amount is given in term of forward power P_{forw} .

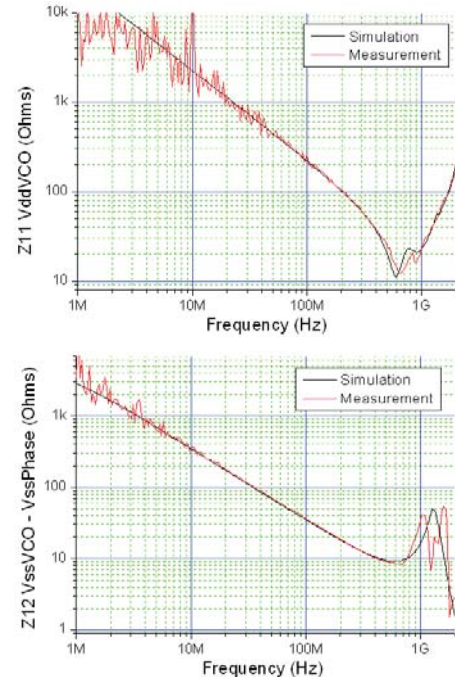


Figure 6. Examples of comparisons between S parameter measurements and simulation from the extracted model (Top: Z11 seen from $V_{DD}VCO$ pin. Bottom : Z12 between $V_{ss}VCO$ and $V_{ss}Ph$ pins)

The coupling of the conducted disturbances is characterized by an “EMI transfer function” of a given IC pin (1). It is an indicator of the coupling efficiency of the conducted disturbance on this pin.

$$EMI \text{ Transfer Function } (V/W) = \frac{\Delta V}{P_{forw}} \quad (1)$$

The EMI transfer function provides information about the frequency dependent behavior of the circuit PDN. If the PDN is modeled by an impedance matrix with the first port placed on the node where the voltage fluctuation is measured and the second port placed at the injection node, the EMI transfer function is related to impedance parameters by equation (2) (Z_c is the characteristic impedance of the EMI injection system, i.e. 50 Ω).

$$EMI \text{ Transfer Function } (V/W) = \frac{4 \cdot Z_{12}^2 \cdot Z_c}{(Z_c + Z_{22})^2} \quad (2)$$

First, in order to demonstrate the relevance of internal noise measurement, the EMI transfer function measured internally by the on-chip sensor is compared with the same measurement

obtained externally with a DSO and an active probe. Their cut-off frequencies are equal to 1.5 GHz. The comparison is shown in Fig. 7. Both measurement methods give similar results up to 250 MHz. At higher frequencies, the voltage fluctuation amplitudes measured by both systems diverge due to the filtering effect of the PLL PDN. The internal measurement provides the actual amount of voltage fluctuation on the $V_{DD}VCO$.

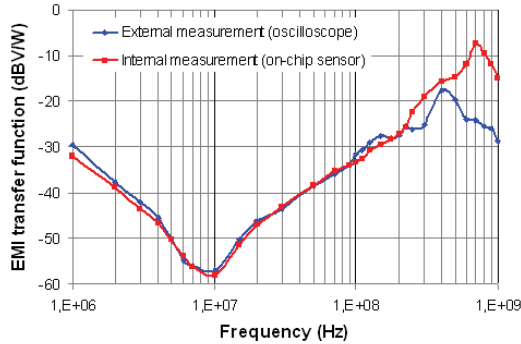


Figure 7. Comparison of EMI transfer function of VCO power supply pin measured internally and externally

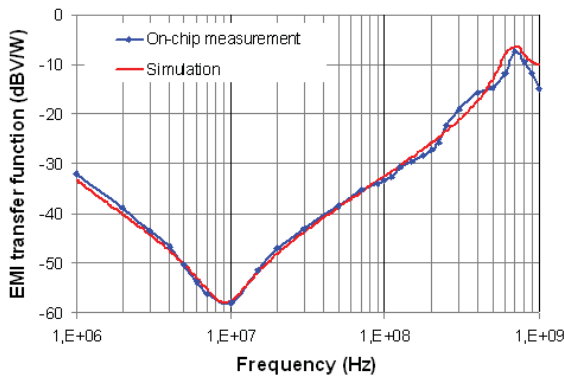


Figure 8. Comparison of measured and simulated EMI transfer function of VCO power supply pin

Then, the PDN model is used to simulate the EMI transfer function of the VCO power supply pin. S parameter measurements are also performed to extract an equivalent model of the DPI test bench and the EMC test board, which is finally merged with the PLL PDN model. Fig. 8 presents the comparison of the measured and simulated EMI transfer functions of $V_{DD}VCO$ pin. The excellent agreement demonstrates that the PLL PDN model is able to predict the amount of voltage fluctuations coupled on the VCO power supply up to 1 GHz.

Measurement and simulation results show the frequency dependent behavior of the noise coupling, linked to the characteristics of the PDN. The noise coupling is minimum about 10 MHz (board decoupling resonance) and is maximum about 600 – 700 MHz when the external disturbance excites an anti resonance between on-chip capacitance and parasitic inductances of package and external decoupling. Surprisingly, the on-chip voltage fluctuation is larger than the off-chip voltage fluctuation between 200 MHz and 1 GHz. The VCO PDN is formed by an on-chip capacitance and a complex

network of package inductances coupled by the substrate. Basically, this complex RLC network can be compared to a second-order RLC filter. At the resonant frequency, the voltage fluctuation can be amplified. Depending on the measurement location (on-chip or off-chip), the parasitic inductances of the equivalent RLC filter are not the same so the transfer function for the noise coupling are different.

C. Coupling between the different power supplies

Some crosstalk exists between the power supplies of the PLL sub-blocks. They share the same substrate and capacitive couplings exist between the power supply rails through inactive ESD protections. The values of the equivalent elements of these couplings have been extracted from S parameter measurements. Fig. 9 presents the comparison between measured and simulated S12 transfer coefficient between $V_{DD}VCO$ and $V_{DD}Ph$ pins. The measurement shows that a significant coupling can exist above 500 MHz. Even if the model extracted from S parameter measurement reproduces the same coupling increase, the coupling model is not enough accurate to ensure a sufficient correlation between measurement and the simulation above 300 MHz.

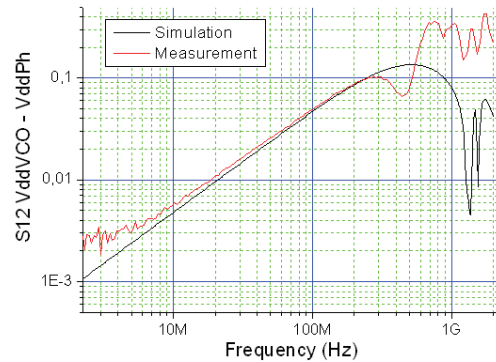


Figure 9. Comparison between measured and simulated transfer coefficient between $V_{DD}VCO$ and $V_{DD}Ph$ pin

The on-chip sensors on $V_{DD}VCO$, $V_{DD}Ph$ and $V_{DD}Div$ are now used to measure simultaneously the amplitude of the voltage fluctuation on these three nodes. Fig. 10 presents the measured ratio between voltage fluctuation amplitude of $V_{DD}Ph$ and $V_{DD}Div$ on $V_{DD}VCO$.

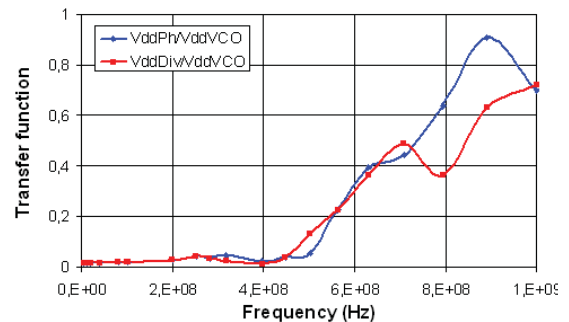


Figure 10. Measurement of the coupling between VCO, phase detector and frequency divider power supplies

Fig. 11 presents the same ratio obtained by simulation. As suggested by the S parameter measurement, a significant

coupling between the different power supplies exists above 500 MHz. It has to be taken into account because noise is not only injected on the VCO power supply and the PLL total phase noise can be affected. The model indicates also that a strong coupling exists between these different supplies above 500 MHz but it underestimates the actual amount of noise. A more accurate model of internal coupling between the different power supplies have to be found to improve the PDN model.

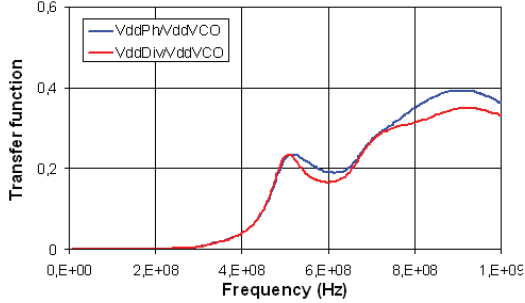


Figure 11. Simulation of the coupling between VCO, phase detector and frequency divider power supplies

IV. IMMUNITY BEHAVIOR MODELING

The second part of the susceptibility model is the immunity behavior block (IB), which describes how the circuit reacts to an incoming disturbance. First, two IB models are proposed and compared. Then, on-chip measurement gives the actual susceptibility level of the PLL, i.e. the internal voltage fluctuation on $V_{DD}VCO$ when a failure arises. This measurement is compared to the simulation to evaluate the accuracy of the IB model.

A. IB model construction

Two approaches are tested to model the behavior of the PLL to the coupling of disturbance on the $V_{DD}VCO$. First, a transistor-based SPICE model is built from the circuit schematic. Transistor models of SMARTMOS technology were not available, so a typical CMOS 0.25 μm transistor model given in [9] has been used. Its parameters have been modified to fit simulations on measurements of VCO and PLL characteristics (e.g. acquisition range, free oscillation frequency, VCO pushing coefficient).

The second approach is based on an analytical model of the PLL period jitter, which allows a fast and simple evaluation of jitter induced by VCO power supply fluctuations. The injection of voltage fluctuations on $V_{DD}VCO$ leads to instantaneous variations of VCO oscillation frequency. A quasi-linear relation exists between the VCO frequency and the power supply voltage, for small voltage variations, which can be characterized by the pushing coefficient of the VCO K_{VCO} . The VCO can be considered as a frequency modulator commanded by its power supply fluctuations. Assuming that the noise coupled on the $V_{DD}VCO$ is a harmonic noise with a frequency F_{EMI} and an amplitude V_{EMI} , the jitter variance σ_ϕ can be computed according to (3) [10]. Considering our case study, the disturbance is related to period jitter at the PLL output. The period jitter σ_T is the first difference of the jitter and can be computed according to (4) [10]. The overall PLL phase noise is

equal to the phase noise induced by the VCO filtered by the PLL sub-blocks. From the characteristics of the PLL, the PLL closed loop is considered as a first order low pass filter.

$$\sigma_\phi^2(F_{EMI}) = \frac{1}{(2\pi F_0)^2} \frac{K_{VCO} \cdot V_{EMI}}{2 \cdot (2\pi F_{EMI})^2} \quad (3)$$

$$\sigma_T^2(F_{EMI}) = \sigma_\phi^2(F_{EMI}) \cdot |1 - \exp(-j2\pi F_{EMI} T_0)|^2 \quad (4)$$

The simulations of PLL period jitter vs. EMI frequency for constant voltage fluctuation amplitude given by the SPICE and analytical models are compared in Fig. 12. Both methods provide similar results up to 200 MHz, demonstrating that the assumptions of the analytical model are valid. The period jitter tends to decrease with frequency and cancels at each multiple of the PLL output frequency. However, the analytical model underestimates the period jitter above 200 MHz and fails to predict the special VCO behavior around 288, 576 and 864 MHz. Due to the VCO structure, a synchronization between each delay cells of the VCO and the EMI happens at these frequencies and leads to a large increase of VCO jitter. The analytical model has to be improved to take into account this effect. In spite of its complexity, the SPICE model is chosen as IB model for the PLL.

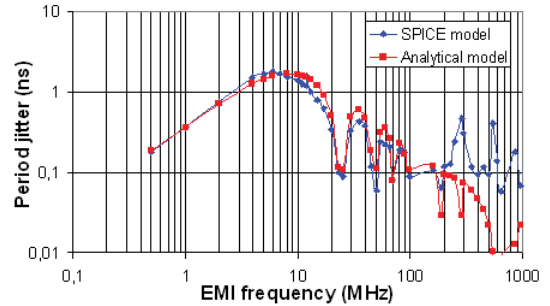


Figure 12. Simulations of PLL period jitter vs. EMI frequency with SPICE and analytical models

B. Characterization of PLL sensitivity to VCO power supply fluctuations

The on-chip sensor placed on $V_{DD}VCO$ is now used to measure the amount of voltage fluctuations when a failure arises according to the susceptibility criterion defined in II.B. At each EMI frequency, when a failure arises, the sensor is activated and the peak-to-peak amplitude and standard deviation of the measured voltage fluctuations are acquired. Fig. 13 presents the measurement of the PLL sensitivity to VCO power supply fluctuations. Two failure types are detected and reported in Fig. 13: either the period jitter exceeds 2 ns or the PLL unlocks directly. As suggested by simulation results, the PLL is very sensitive in low frequency, except around each multiple of the PLL output frequency where no failures are detected. Moreover, the PLL becomes very sensitive around particular frequencies: 288, 576 and 864 MHz. This behavior has also been detected by SPICE simulation.

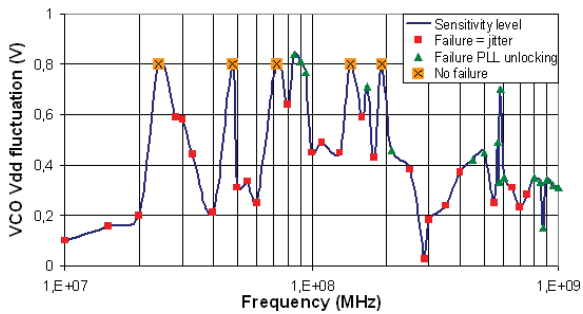


Figure 13. Measurement of PLL sensitivity to VCO power supply voltage fluctuations

C. Simulation of PLL sensitivity to VCO power supply fluctuations

The PLL IB block is inserted in the circuit PDN in order to simulate the required amount of noise on VddVCO to induce a failure. Transient simulations are performed for various EMI frequencies between 10 and 1000 MHz. Fig. 14 shows the simulation results which can be compared with on-chip measurement results presented in Fig. 13.

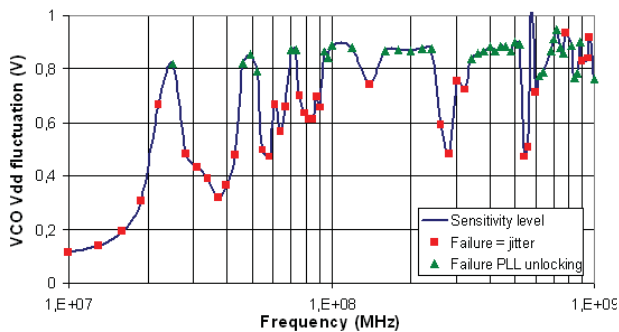


Figure 14. Simulation of PLL sensitivity to VCO power supply voltage fluctuations

The simulation provides the right trend of the PLL susceptibility level. The same failures observed in measurement arise in simulation, at the same frequencies. The simulated and measured susceptibility levels of the PLL are very similar in low frequency, up to 100 MHz. The SPICE model predicts very accurately the amount of period jitter versus the VCO power supply fluctuations. However, the simulation tends to overestimate the amount of noise required to unlock the PLL. Simulation shows that PLL unlocking is linked to a failure of the frequency divider which happens when the noise at the VCO output is enough large to induce false switchings. Two ideas to improve the susceptibility model are: first, modifying the coupling model between the different power supply pairs of the PLL. As shown in Fig. 10, a significant noise is injected on V_{DDPh} and V_{DDDiv} which contributes to increase the jitter at the PLL output. Secondly, a better SPICE model of divider susceptibility to voltage fluctuations has to be developed.

V. CONCLUSION

The paper has presented the construction of the susceptibility model of a PLL based on ICIM formalism. The passive distribution network (PDN) and immunity behavior (IB) blocks are modeled from S parameter measurements and basic circuit information. To test the validity of the susceptibility model, several on-chip voltage sensors have been implemented on PLL power supply rails. The measurement of internal voltage fluctuations characterizes the coupling efficiency of an external conducted disturbance in the circuit, the sensitivity of a function to voltage fluctuations and thus helps to validate or not the PDN and IB models. The on-chip measurements have shown that the proposed model predicts accurately the amount of noise coupled on the VCO power supply up to 1 GHz and the behavior of the PLL to conducted disturbances. However, the model underestimates both the internal couplings between separated power supplies and the sensitivity of the PLL to voltage fluctuations. The on-chip measurements have revealed some limits of the circuit model which would be hard to detect otherwise, such as the sensitivity of the VCO to power supply voltage fluctuations and parasitic coupling through separated power supplies.

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