



**HAL**  
open science

## An On-Chip Sensor for Time Domain Characterization of Electromagnetic Interferences

Alexandre Boyer, Sonia Ben Dhia, Christophe Lemoine, Bertrand Vrignon

► **To cite this version:**

Alexandre Boyer, Sonia Ben Dhia, Christophe Lemoine, Bertrand Vrignon. An On-Chip Sensor for Time Domain Characterization of Electromagnetic Interferences. 8th Workshop on Electromagnetic Compatibility of Integrated Circuits (EMC Compo), Nov 2011, Dubrovnik, Croatia. pp.251. hal-00669533

**HAL Id: hal-00669533**

**<https://hal.science/hal-00669533v1>**

Submitted on 13 Feb 2012

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

# An On-Chip Sensor for Time Domain Characterization of Electromagnetic Interferences

A. Boyer, S. Ben Dhia, C. Lemoine  
LAAS-CNRS, INSA de Toulouse  
Toulouse, France  
[alexandre.boyer@insa-toulouse.fr](mailto:alexandre.boyer@insa-toulouse.fr)

B. Vrignon  
Freescale Semiconductor  
Toulouse, France  
[Bertrand.vrignon@freescale.com](mailto:Bertrand.vrignon@freescale.com)

**Abstract**— With the growing concerns about susceptibility of integrated circuits to electromagnetic interferences, the need for accurate prediction tools and models to reduce risks of non-compliance becomes critical for circuit designers. However, on-chip characterization of noise is still necessary for model validation. This paper presents an on-chip noise sensor dedicated to the time-domain measurement of voltage fluctuations induced by interference coupling.

**Keywords** – *integrated circuits; conducted susceptibility; on-chip measurement*

## I. INTRODUCTION

These last years, susceptibility of integrated circuits has become one of the major issues for all circuit classes (digital, analog, RF, power). Concerns about failure mechanisms, electromagnetic interferences (EMI) coupling and susceptibility modeling at circuit level have arisen [1]. The need for prediction of non-compliance risks during the design stage has become critical for IC manufacturers in order to reduce redesign costs and time-to-market. Although many research works about IC susceptibility modeling are on-going [2] [3] [4], accurate measurements of EMI-induced noise at IC level are still a critical information for designers for model validation and design optimization.

Few papers have been published about the on-chip characterization of EMI-induced voltage fluctuations. In [5], an on-chip sensor designed in CMOS 0.25  $\mu\text{m}$  technology has been implemented. Its bandwidth is equal to 2.5 GHz and it is able to extract statistical information about the amplitude of voltage fluctuations. The following paper presents an improved version of this sensor designed in CMOS 90 nm technology, which can acquire the time domain waveform of EMI-induced voltage fluctuations. It gives us valuable information about the distortion induced by the circuit.

After presenting the relevance of characterization of internal voltage fluctuation for the analysis and the modeling of IC susceptibility, a description of the principle and the structure of the sensor is proposed. In the third part, a characterization of sensor performances is presented. In the last part, different examples of time profile of EMI-induced internal voltage fluctuation measured by the on-chip sensor are presented. The acquisition mode proposed by this new version allows an

accurate characterization of incoming disturbance distortion induced by the circuit.

## II. MOTIVATION FOR ON-CHIP MEASUREMENTS OF EMI-INDUCED VOLTAGE FLUCTUATIONS

The susceptibility of a circuit depends not only on the intrinsic sensitivity of disturbed functions, but also on the filtering effect of the circuit and its package. Measuring the amount of EMI-induced noise on a sensitive node of a circuit is critical for IC designers for two reasons. First, an accurate measurement of induced voltage fluctuations on circuit terminals helps to determine the actual sensitivity of the disturbed function. Secondly, the efficiency of EMI coupling on a given node at various frequencies can be measured.

The external characterization of EMI-induced voltage fluctuations is limited by the bandwidth of CMOS analog buffer and electrical parasitic elements of chip and package interconnects. Moreover, the accuracy of results can be affected by repeatability errors due to probe positioning, especially at high frequency. In the following example published in [6], off-chip and on-chip measurements of EMI-induced voltage fluctuations are compared to demonstrate the relevance of on-chip measurements. Conducted harmonic disturbances are applied on the power supply pin of a digital core designed in 0.25  $\mu\text{m}$ . Off-chip measurements are ensured by a 2.5 GHz active probe placed on the power supply pin of the digital core and connected to a 2 GHz digital storage oscilloscope. On-chip measurements rely on an on-chip sensor, based on the previous design version, connected to the core power distribution network. Preliminary characterizations have shown that the sensor bandwidth is equal to 2.5 GHz [5].

Both measurements are compared in Fig. 1. The forward power required to induce a voltage fluctuation equal to 0.25 V is acquired versus the EMI frequency. Both measurement methods provide different results above 50 MHz. Between 50 and 140 MHz, the voltage fluctuation amplitude is larger inside the chip than outside the chip, while the off-chip voltage fluctuations exceeds the on-chip voltage fluctuations above 140 MHz. As the cut-off frequencies of both measurement systems exceed 1 GHz, the observed differences cannot be explained by their frequency limitations but by the differences in measurement locations. CAD simulation helps us to understand the difference between both measurement results. The circuit package, IC interconnects and equivalent on-chip capacitance

act as a second order low pass filter. The on-chip EMI-coupling optimum measured at 140 MHz is due to the resonance between package inductances and core equivalent capacitance. Above the resonance frequency, the on-chip decoupling filters EMI-induced voltage fluctuations efficiently.

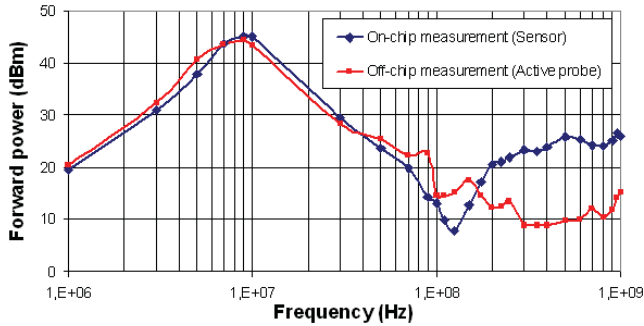


Figure 1. Comparison of off-chip and on-chip measurements of EMI coupling efficiency on a CMOS 0.25 μm digital core

The significant measurement discrepancies between on-chip and off-chip noise can lead to different evaluation of circuit susceptibility. These measurements show that the on-chip noise sensor provides a more realistic measurement of noise that is actually coupled across the digital circuit above 50 MHz. Around 100 MHz, the amount of EMI-induced noise tends to be underestimated by off-chip measurements, while it is overestimated above 200 MHz. Moreover, the complex on-chip propagation of conducted EMI can be understood more clearly by on-chip noise sensor measurements.

### III. ON-CHIP SENSOR PRESENTATION

#### A. On-chip sensor principle

A first version of the on-chip noise sensor was designed in the early 2000s to address signal and power integrity issues at IC level [7]. The sensor is based on a sequential equivalent-time sampling. Its principle is described in Fig. 2. An on-chip sample and hold (S/H) cell directly probes the voltage along IC interconnects and operates in sub-sampling conditions [8].

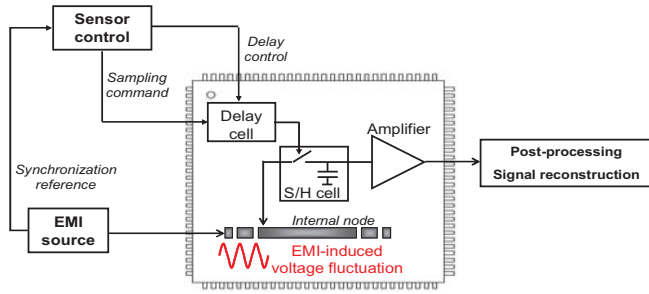


Figure 2. Principle of the sensor

In the previous sensor version [5], the acquisition is not synchronized on the incoming disturbance (asynchronous acquisition) and the delay cell is removed. The acquisition is made randomly and only the statistical distribution of the signal amplitude is available. Although the actual signal waveform cannot be measured, the set-up is very simple. The asynchronous acquisition mode is adapted to harmonic

disturbances. As the waveform is known, the disturbance amplitude can be easily computed, as shown in Fig. 3 and (1). For other type of disturbances (such as pulse) or if non linearity arises in the circuit, the voltage fluctuation is not sinusoidal and the statistical distribution is not sufficient to have a complete characterization of the voltage fluctuation.

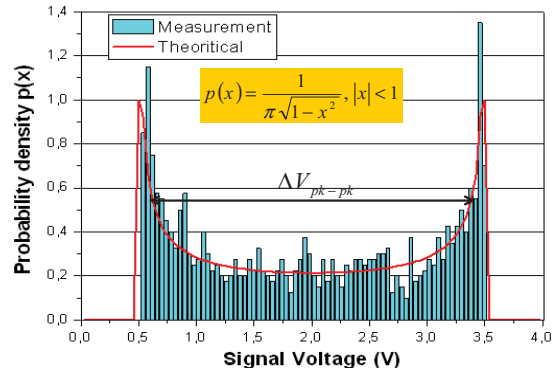


Figure 3. Theoretical and measured statistical distribution of a sinus waveform

$$\Delta V_{pk-pk} = 2\sqrt{2} \cdot \sigma \quad (1)$$

$$\sigma = \frac{1}{N-1} \sqrt{\sum_{i=1}^N (X_i - \bar{X})^2}$$

The new version is based on a synchronous acquisition mode, where the sensor acquisition is synchronized on the incoming disturbance, as shown in Fig. 2. The principle of signal reconstruction in time domain is explained in Fig. 4. The signal acquisition is made over several occurrences of a reproducible phenomenon, and only one sample is taken at each repetition. An external synchronization signal is used to both trigger off the event to characterize and activate the S/H cell. The sampling command is shifted from the synchronization signal by a delay cell. When the first synchronization signal is detected, the first sample is acquired. At the next period, a new sample is acquired after a short delay from the time position of the first sample. The output low frequency signal is externally sensed for waveform reconstruction. The time step of the reconstructed waveform is set by the minimum delay step, while its duration is set by the maximum delay produced by the delay cell.

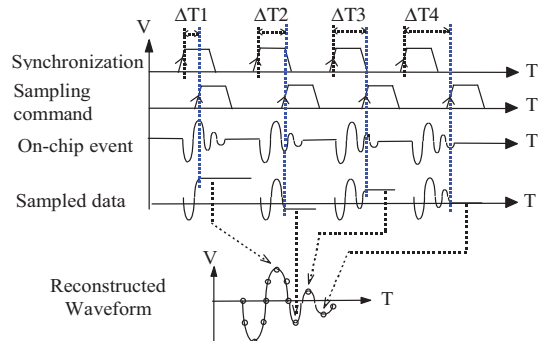


Figure 4. Principle of signal reconstruction

### B. On-chip sensor architecture

A version of the on-chip sensor in synchronous version has been designed in a test chip developed in CMOS 90 nm technology. This sensor can be still used in asynchronous mode, by removing the synchronization between the incoming disturbance and the sampling command. The test chip contains also various analog and digital test structures. Fig. 5 describes the architecture of the new version of the sensor. The sensor is made of two parts: the sensor probe placed on the characterized node, and the sensor core which multiplexes the 32 sensor probes placed in the circuit, controls the variable delay on the sampling command and contains the output amplifier.

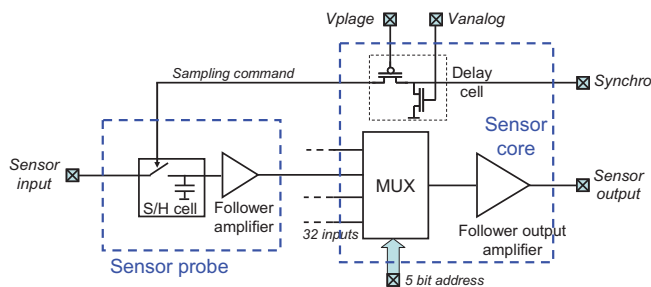


Figure 5. On-chip sensor architecture

The sensor probe is made of the S/H cell and a first follower amplifier. Its size is equal to  $19.47 \times 18.86 \mu\text{m}$ . The input probe capacitance is equal to 4 fF. The input impedance is enough large to ensure a non-invasive measurement up to 10 GHz (unfortunately, the experimental characterization of sensor bandwidth is not possible due to the limitation of our equipments. In the following part, several measurements will show that the bandwidth exceeds 2 GHz). The 32 sensor probes have been spread on various nodes of the test chip.

The delay added on the sampling command is controlled by two analog signals called Vanalog and Vplage. Vplage configures the time range for delay, while Vanalog ensures a fine control on the delay. The last stage is a follower amplifier which offers a constant gain up to 2.5 MHz. The signal reconstruction is possible only if the output amplifier does not filter the sampled signal. That's why the sampling frequency must remain smaller than the cut-off frequency of the amplifier.

The isolation of the sensor from all noise sources is critical to ensure accurate measurements. Thus, the sensor is powered by a dedicated 3.3 V power supply, separated and isolated from the other power supplies of the circuit. Moreover, the sensor is isolated from the bulk substrate by a deep N-well layer, so the input sensor voltage can be shifted to negative value (up to -0.6 V).

## IV. SENSOR CALIBRATION

The sensor has not an ideal behavior. First, charge injection occurs when the S/H cell turns off and leads to parasitic offset. Although it has been reduced in design, it cannot be totally canceled. Secondly, as the output amplifier is not perfectly linear and as the storage capacitance is slightly voltage dependent, the overall gain of the sensor is not constant.

Finally, the relation between the delay and the voltage of delay cell command is not linear. In order to compensate the non ideal behavior of the sensor and set the command for the delay, a calibration procedure is required.

### A. Input-output characteristic – Compensation of parasitic offset and non linearity

The sensor operation is affected by imperfections and mismatch in the implementation of its elements, which degrades the output response. The input-output characteristic is measured to check the sensor linearity, evaluate the offset and calibrate the sensor. It consists in applying a constant and known voltage on the sensor input and measuring the voltage amplitude of the output samples. If the sensor response is quasi linear, a linear relation can be established between sensor output and input. From this relation, both static gain and offset can be extracted to compensate sensor imperfections. Fig. 6 presents the measured input/output characteristic of the sensor.

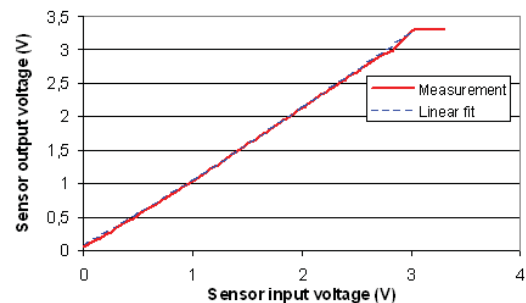


Figure 6. Sensor input-output characteristic

The sensor is highly linear with a gain equal to 0.99 and affected by an offset of 60 mV. The sensor imperfection can be easily corrected without inducing a large error. The largest difference between the actual and the fitted input-output characteristics reaches 22 mV. The input voltage range of the sensor is quasi rail-to-rail (from 0 V to 3 V).

### B. Delay cell calibration

The reconstruction of the signal in time domain needs a perfect knowledge of the delay added on the sampling command. A delay cell has been isolated and placed within a ring oscillator. The delay is extracted by the measurement of the ring oscillator frequency versus Vanalog for different values of Vplage. Fig. 7 shows the characterization of the delay produced by the delay cell for different control voltage values.

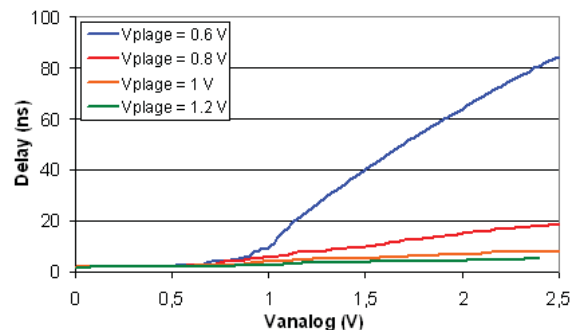


Figure 7. Delay cell characteristic

The time range of the sensor is equal to the maximum allowed delay i.e. 80 ns. If we consider the characterization of a harmonic disturbance, the sensor can measure disturbance with frequency larger than 12.5 MHz. The time resolution of the sensor can be reached for the largest  $V_{plage}$  value (3 V) and depends on the noise coupled on delay cell control signals. For a voltage step equal to 50 mV on  $V_{analog}$  and  $V_{plage}$  equal to 3 V, the time resolution is equal to 3 ps, but the time range is equal to 110 ps.

## V. TIME DOMAIN CHARACTERIZATION OF ELECTROMAGNETIC INTERFERENCES

The on-chip noise sensor is now used to measure the waveform of conducted disturbance within the circuit. Sensor measurements aim at determining the amount of voltage fluctuations induced by disturbance and distortion level. On-chip measurements in synchronous mode are first compared with external measurements done with an oscilloscope and then compared with on-chip measurements made in asynchronous mode.

### A. Test set-up presentation

The following part is focused on a sensor placed on the 1.2 V power supply of a digital core called VddCore. Conducted harmonic disturbance is applied on the VddCore pin according to IEC 62132-4 Direct Power Injection (DPI) standard [9], as described in Fig. 8.

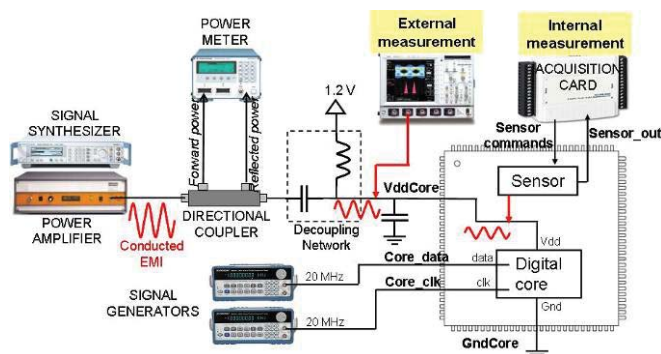


Figure 8. Experimental set-up for the external (oscilloscope) and on-chip (sensor) characterization of EMI-induced voltage fluctuation

During injection, three measurement methods are compared:

- External measurement: the EMI-induced voltage fluctuation is measured directly on the Vddcore package pin with 2 GHz digital oscilloscope equipped with a 2.5 GHz active probe.
- On-chip measurement in asynchronous mode: the EMI-induced voltage fluctuation is measured within the circuit by the on-chip sensor. The sampling command is not synchronized on the disturbance produced by the signal synthesizer, so only the statistical distribution of the disturbance is acquired.
- On-chip measurement in synchronous mode: the EMI-induced voltage fluctuation is measured within the

circuit by the on-chip sensor. The sampling command is synchronized on the disturbance produced by the signal synthesizer, so the waveform of the disturbance is acquired.

### B. Characterization of conducted disturbance coupling

First, the on-chip measurements in synchronous mode of VddCore are compared with external measurements at different disturbance frequencies. Fig. 9 compares the results of both measurement methods at 100, 500 and 1000 MHz. The time resolution is equal to 0.5 ns for the measurement at 100 MHz, 0.2 ns for the measurement at 500 MHz and 0.15 ns for the measurement at 1000 MHz.

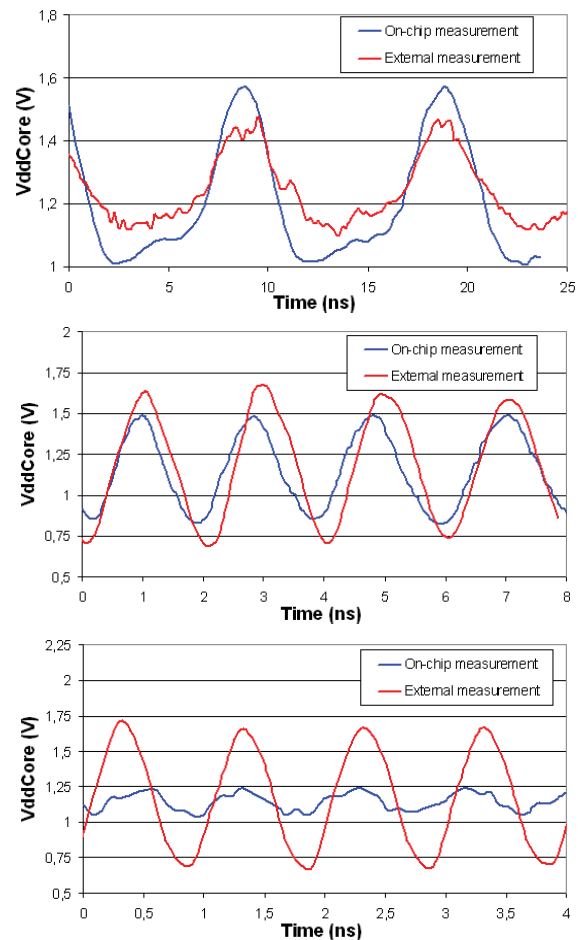


Figure 9. Comparison between external and on-chip measurement of VddCore fluctuations at  $F_{emi} = 100$  MHz (top), 500 MHz (middle) and 1000 MHz (bottom)

The sensor provides an accurate waveform of the internal voltage fluctuation induced by the conducted disturbance coupling. The fluctuation amplitude measured on-chip is different of the one measured externally. At 100 MHz, the on-chip voltage fluctuation is larger than the fluctuation measured off-chip. The package and the circuit resonate and amplify the amount of internal noise. At higher frequency, the situation is inverted. The coupled disturbance is filtered by the circuit and the package. As explained in II, the on-chip measurement provides more exact information about EMI coupling in an IC.

If the on-chip measurement is analyzed in detail, some noise disturbs the measured waveform. This noise is due to the switching noise of the digital core which superimposes on the coupled external disturbance. To isolate both source of noise, the digital core activity, the sensor sampling and the disturbance source are synchronized. The harmonic disturbance frequency is equal to 100 MHz and the core operates at 20 MHz. Fig. 10 compares on-chip and external measurements. The time resolution of the sensor is set to 0.5 ns and is small enough to measure accurately the time profile of the core switching noise. The switching noise has a very high frequency content which does not seem filtered by the on-chip sensor. As the time resolution of the on-chip measurement is equal to 0.5 ns, we can conclude that the sensor bandwidth is larger than 2 GHz.

On-chip and external measurements are quite different: the 100 MHz EMI-induced voltage fluctuation and the switching noise are larger in the circuit due to filtering effect of the circuit and the package. Once again, this comparison shows the relevance of on-chip measurements for the evaluation of EMI coupling.

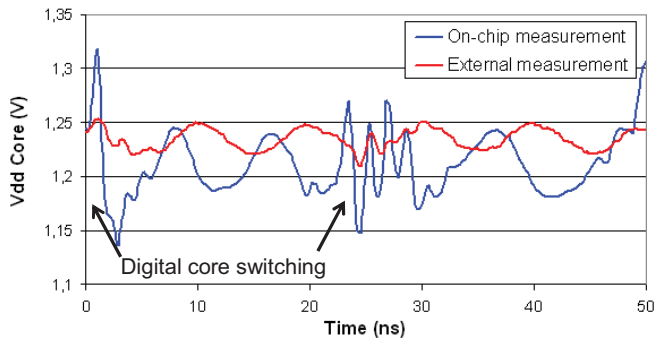


Figure 10. On-chip and external measurement of VddCore fluctuations at Femi = 100 MHz, digital core activity, the sensor sampling and the disturbance source are synchronized

### C. Characterization of EMI distortion induced by the circuit

The synchronous acquisition has a significant importance when the waveform of the disturbance cannot be forecasted, e.g. when the circuit distorts harmonic disturbance. The following measurements show on-chip measurement results of voltage fluctuations for EMI frequency equal to 100 MHz and various amplitudes. The sensor is used both in asynchronous and synchronous modes. In Fig. 11, the voltage fluctuation waveforms measured for three different disturbance amplitudes are compared. When the disturbance amplitude increases, more distortion occurs.

Fig. 12 presents the statistical distribution of VddCore voltage fluctuations extracted by the on-chip sensor in asynchronous mode. The histogram provides the probability density function (PDF) of the VddCore voltage fluctuation. As the circuit distorts the incoming disturbance, the PDF is quite different of the distribution of an ideal sinus waveform (Fig. 3). Although the asynchronous acquisition can detect distortion appearance, the exact waveform of the signal cannot be found out and the exact fluctuation amplitude cannot be extracted.

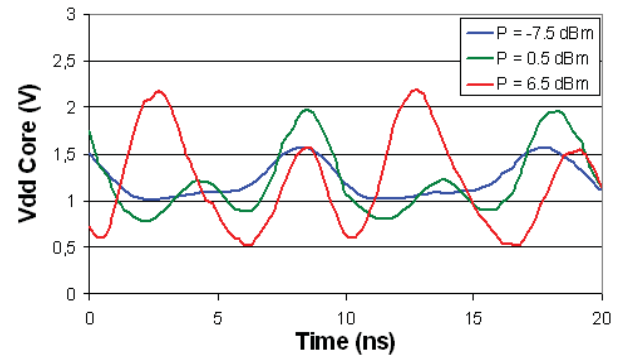


Figure 11. On-chip measurement of VddCore fluctuations at Femi = 100 MHz for different disturbance amplitude

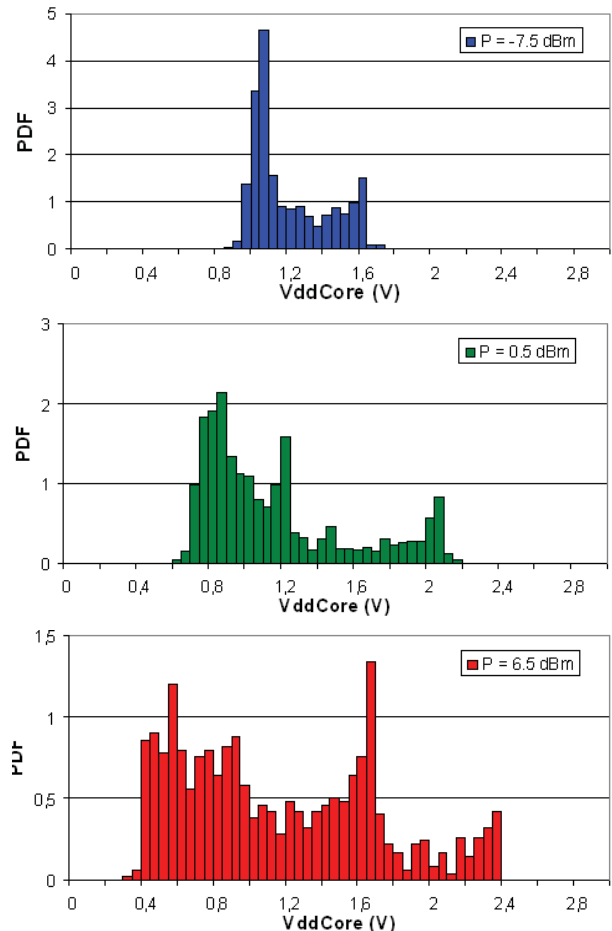


Figure 12. Statistical distribution (in term of Probability Density Function) of VddCore fluctuation at Femi = 100 MHz for different disturbance amplitude, measured by the on-chip sensor in asynchronous mode

## VI. CONCLUSION

The paper has presented a sensor designed in CMOS 90 nm which aims at characterizing the waveform of conducted disturbance coupled in an integrated circuit. The on-chip characterization of EMI-induced voltage fluctuation is essential for circuit designer to understand more clearly the origin of circuit susceptibility and validate their susceptibility model. The measurement examples presented in the paper show that

the sensor is able to acquire the time profile of circuit switching noise and harmonic disturbance up to 1 GHz. Compared to external characterization, the on-chip measurement provides more exact information about interferences coupling in a circuit. Besides, the characterization in time domain provides an accurate characterization about distortion induced by the disturbed circuit. The minimum time resolution of the sensor shown in proposed measurement examples reaches 0.15 ns. Although simulations show that the sensor bandwidth exceeds 10 GHz, the exact bandwidth of the sensor has not been characterized experimentally because of equipment limitations. Examples presented in the paper have suggested that the sensor bandwidth exceeds 2 GHz.

#### REFERENCES

- [1] M. Ramdani, E. Sicard, A. Boyer, S. Ben Dhia, J. J. Whalen, T. Hubing, M. Coenen, O. Wada, "The electromagnetic compatibility of integrated circuits - past, present and future", *IEEE Transactions on Electromagnetic Compatibility*, vol. 51, no. 1, February 2009.
- [2] A. Boyer, S. Ben Dhia, E. Sicard, "Modelling of a mixed signal processor susceptibility to near-field aggression", *IEEE Symposium on Electromagnetic Compatibility*, July 2007.
- [3] J. B. Gros, G. Duchamp, A. Meresse, J. L. Levant, C. Marot, « An analog to digital converter ICIM-CI model based on design », *EMC Compo 09, 7th International Workshop on Electromagnetic Compatibility of Integrated Circuits*, Toulouse, France, November 2009.
- [4] S. O. Land, F. Lafon, F. de Daran, F. Leferink, M. Drissi, M. Ramdani, "Immunity modeling of the LM2902 Operational Amplifier", *EMC Europe 2010*, September 2010, Wroclaw, Poland
- [5] Deobarro, M., Vrignon, B., Ben Dhia, S., Shepherd, J., "On-chip sampling and EMC modeling of I/Os switching to evaluate conducted RF disturbances propagation", *Asia Pacific EMC conference, APEMC 2010*, 2010 April, Beijing, China..
- [6] Ben Dhia, S., Boyer, A., Vrignon, B., Deobarro, M., IC immunity modeling process validation using on-chip measurements, *12th IEEE Latin-American Test Workshop (LATW2011)*, Porto de Galinhas, Brazil, March 27th-30th, 2011.
- [7] S. Delmas - Ben Dhia, E. Sicard, F. Caignet, "A new method for measuring signal integrity in CMOS ICs", *Microelectronic International Journal*, Vol. 17, No. 1, MCB University Press, pp. 17-21, January 2000.
- [8] Y. Zheng, K. L. Shepard, "On-Chip Oscilloscopes for non invasive time-Domain Measurement of Waveforms in Digital Integrated Circuits", *IEEE Transactions on Very Large Scale Integration Systems*, Vol. 11, No 3, June 2003.
- [9] IEC 62132-4, 2003, "Direct RF Power Injection to measure the immunity against conducted RF-disturbances of integrated circuits up to 1 GHz", IEC standard.