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A new approach to modelling the impact of EMI on MOSFET DC behaviour

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Abstract

In this letter a simple analytical model to predict the DC MOSFET behaviour under electromagnetic interference (EMI) is presented. The model is able to describe the MOSFET performance in linear and saturation regime under EMI disturbance applied on the gate. The model consists of a unique simple equivalent circuit based on a voltage dependant current source and a reduced number of parameters which can accurately predict the drift on the drain current due to the EMI source. The analytical approach has been validated by means of electric simulation and measurements and can be easily introduced in circuit simulators. The proposed modelling technique combined with the nth-power law model of the MOSFET without EMI, significantly improves its accuracy in comparison with the nth-power law directly applied to a MOSFET under EMI impact.

KEYWORDS: MOSFET, Electromagnetic Interference (EMI), Electromagnetic Compatibility (EMC), Electrical modelling

Introduction: Electronic systems are disturbed by electromagnetic interference (EMI) which can potentially disrupt their operation. In fact, the increasing EMI pollution environment is a major concern in the design of electronic devices based on MOSFET transistors [1-2]. Therefore, the modelling and prediction of interference effects play an outstanding role in the electromagnetic compatibility (EMC) field. Likewise, accurate models of MOSFET are required in order to design and implement modern electronic circuits. From the previous reported works, the nth-power law model has been revealed as one of the most successful DC MOSFET modelling techniques in the linear and saturation regions [3]. Unfortunately, this modelling technique directly applied to MOSFET subjected to EMI impact, decreases its degree of accuracy in comparison with the free EMI case. In this letter, a new MOSFET model based on a combination of the nth-power law MOSFET together with a voltage gate and voltage EMI dependant current source is proposed in order to accurately describe the transistor behaviour under EMI impact.

Experimental: In order to measure the impact of the EMI on the DC behaviour of the MOSFET, the direct power injection (DPI) method has been applied [4]. Specifically, nMOSFET samples with aspect ratio of $10\ \mu\text{m}/0.38\ \mu\text{m}$ fabricated in 3.3 V CMOS 90-nm *Freescale Semiconductor* process have been evaluated. The developed test is based on the experimental setup described in Fig. 1. An interference signal with an amplitude and frequency sweep ranges of $V_{\text{EMI}}=0\ \text{V}$ (free EMI disturbance)-1.2 V and $f=1\text{-}100\ \text{MHz}$ is coupled to the transistors' gate through a bias-T block. The drain current, I_D , has been measured with a single measurement unit connected to the transistor's drain. Fig. 2 illustrates the experimental I_D - V_{DS} behaviour with and without interference disturbance. Curves for $V_{GS}=3.3\ \text{V}$, 2.7 V and 2.1 V are depicted at $V_{\text{EMI}}=0\ \text{V}$, 0.6 V and 1.2 V ($f=10\ \text{MHz}$). Free EMI disturbance corresponds to the continuous line, 0.6 V to the dotted line and 1.2 V dashed line. In all the interference cases, a drain current degradation is observed. This degradation is shown by decreasing the I_D with regard to the free EMI case. The degree of degradation increases with the amplitude interference level and it is mainly observed in the transition between linear and saturation region.

Proposed model and results: In order to estimate the absolute value of the impact of the interference disturbance, the drain current shift between free-EMI and disturbed samples corresponding to $V_G=3.3V$ on Fig. 2 has been calculated and plotted in Fig. 3 (for cases: $V_{EMI}=0.6 V, 0.9 V$ and $1.2 V$). As expected the difference is higher at the transition between linear and saturation region and the effect is enhanced with V_{EMI} . With the aim to evaluate this current drain shift with a circuit simulator, the nth-power law parameters have been extracted in the devices under test without EMI (Table I). It is important to remark that the model fits the experimental data with an error lower than 0.5%. The model has been included in a circuit simulation reproducing the experimental setup (*i.e.*, by taking into account a sinusoidal EMI source). The comparison between measurements (dot symbols, Fig. 3) and nth-power law model simulation (continuous line, Fig. 3) under EMI conditions reveals a significant variation. Although the nth-power law model can accurately reproduce the DC MOSFET behaviour, it overestimates the drain current shift roughly in a factor 2 with regard to the experimental data. In fact, this variation roughly corresponds to a 3%, respect to the actual current, which is clearly higher than the intrinsic error of the nth MOSFET model (0.5%). Therefore, some additional corrections describing this shift effect are required. A parametric analysis of the experimental data in Fig. 3 has been performed in terms of several MOSFET variables. The study reveals that the drain current shift produced by interference signals, ΔI_D , depends on V_{EMI} , V_{DS} and V_{GS} according to the equation (1),

$$(1)$$

where C_1 , C_2 and C_3 are fitting constants, which are summarized in Table II. According to this analytical method, the proposed circuit describing the DC behaviour of MOSFET samples under EMI impact is based on the nth-power law model together with an extra voltage dependant current source, $\Delta I_D=f(V_{EMI}, V_{DS}, V_{GS})$, in parallel between drain and source nodes, as shown in Fig. 4. The simulation results of the proposed model are depicted in Fig. 3 (dashed line). As can be observed, the model accurately reproduces the current drain shift by combining the nth-power law parameter extraction without interference conditions with the proposed ΔI_D source.

Conclusions: In summary, a simple analytical circuit model to predict the DC MOSFET behaviour under EMI has been proposed. The model consists of a V_{EMI} , V_{DS} and V_{GS} dependant current source and a reduced number of constants. Simulated and experimental results reveal a good accuracy in the prediction of the drift on the drain current due to the EMI source located on the transistor's gate. The proposed modelling technique combined with the nth-power law model of the MOSFET without EMI disturbance, significantly improves its accuracy in comparison with the nth-power law directly applied to a MOSFET under EMI impact. Therefore, it can be easily included on circuit simulators.

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References.

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FIGURE CAPTIONS

Fig. 1. Experimental setup.

Fig. 2. Experimental I_D - V_{DS} characteristics under EMI conditions. Continuous lines correspond to MOSFET without EMI and dot and dashed lines correspond to I_D - V_{DS} under EMI of 0.6V and 1.2V, respectively. Curves for $V_G= 3.3V, 2.7V$ and $2.1V$ are shown.

Fig. 3. Drain current shift due to EMI. Dot points correspond to measured data, continuous lines correspond to simulated data using the nth power law model and dash line correspond to the proposed model. Curves for $V_G= 3.3V$, and EMI amplitude of 1.2V, 0.9V and 0.6V are shown.

Fig. 4. Proposed MOSFET model under EMI conditions.

Table I. nth-power law parameters without EMI

Table II. Model parameters of expression 1 for the data in Fig.3

Figure 1.

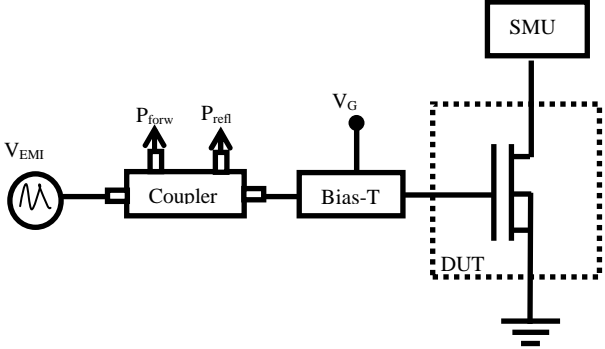


Figure 2

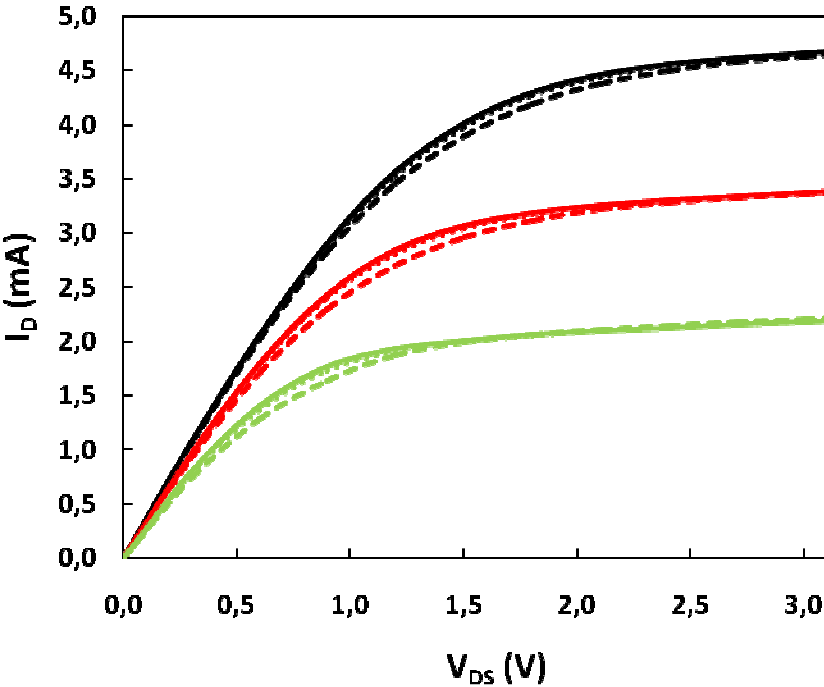


Figure 3

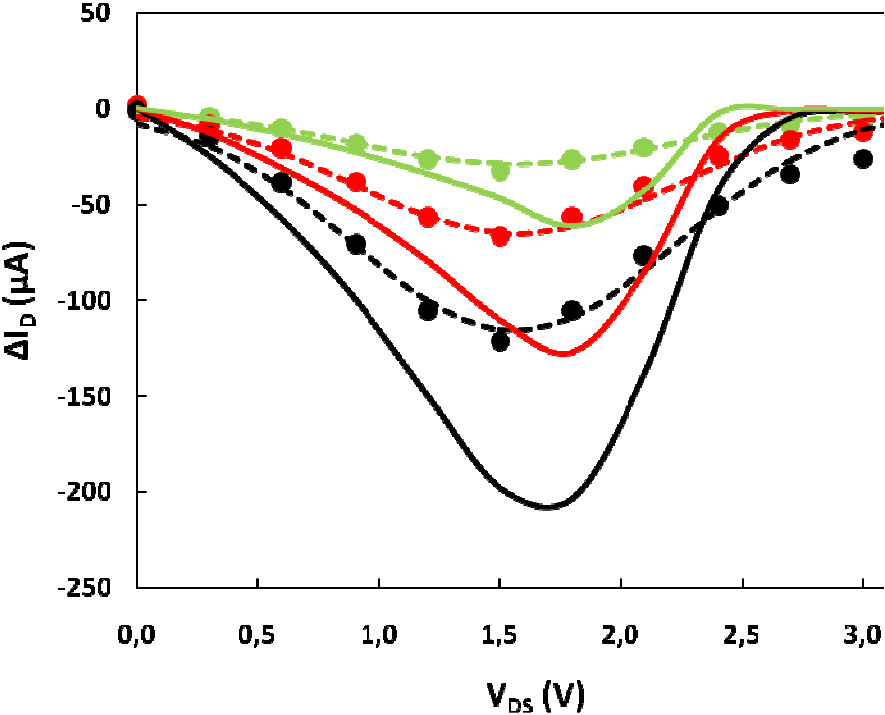


Figure 4

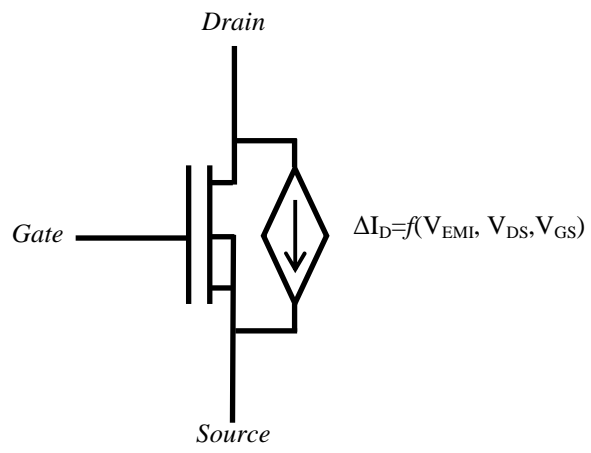


Table I.

V_{l0}	m	n	K	B	λ_0
1.134	0.678	0.995	1.267	$73.48 \cdot 10^{-6}$	0.038

Table II.

C_1	C_2	C_3
80.41	1.12	0.47