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# Understanding the failure mechanisms of protection diodes during system level ESD: towards repetitive stresses robustness

M. Diatta, D. Trémouilles, E. Bouyssou, R. Perdreau, C. Anceau and M. Bafleur

**Abstract**— In electronic systems the ever-increasing level of integration is paced by component scaling. Consequently, system level protection improvements in electrostatic discharge (ESD) reliability during a device’s lifetime is mandatory. To this end we have investigated bidirectional system level ESD protection diodes that have been subjected to repetitive HMM stresses. Our goal was to develop robust ESD components by understanding the physical and electrical behaviors of components after multiple ESD surges. In this paper, three ESD-induced failure modes of protection devices are demonstrated and analyzed in terms of severity: charge trapping in the silicon-oxide interface, metallic diffusion towards the contacts and melted filaments in the silicon bulk at the junction periphery.

**Index Terms**— Electrostatic Discharge (ESD), Failure Mechanisms, Protection diode, System level.

## I. INTRODUCTION

ELECTRONIC devices become more and more portable as components dimensions scale down. Hence, for the robustness of electronic systems such as in automotive or hand help applications, efficient ElectroStatic Discharge (ESD) protection devices are greatly desirable. The challenge of adopting new and more stringent reliability test conditions is essential to provide improved robustness regarding the various type of aggressions the device will encounter in the real world. For a single ESD pulse, typical failure mechanisms are well understood especially for Human Body Model (HBM) or Transmission Line Pulsing (TLP) type of stress [1] [2], but almost no study is available for system level and repeated ESD stresses [3] [4] [5].

This work is aimed at further understanding failure mechanisms of ESD protection diodes subjected to system level ESD stresses. We identified the degradation mechanisms so as to design a reliable protection diode with improved robustness and able to sustain at least 1000 ESD stresses over the product lifetime.

The studied devices and the applied ESD stress are presented in section II. In section III, single and cumulative stresses robustness are compared for different device geometries. Finally, failure mechanisms are identified and their severity analyzed and compared.

## II. STRUCTURES UNDER STUDY AND APPLIED ESD STRESS

### A. Studied Devices

The investigations have been carried out on two protection structures: “Lateral” and “Surrounded” back-to-back diodes dedicated to system level ESD protection (Fig. 1).

The same P type substrate is used to build both diodes. In/Out and Ground junctions have the same  $N^+$  doping profile (Fig. 2). The diodes have a breakdown voltage of about 16V.

For both positive and negative ESD current stresses, one diode is forward biased whereas the other one operate in reverse mode. Neither snapback nor any bipolar effect is observed due to the large distance separating the diode’s junctions ( $>30\mu\text{m}$ ). However, conductivity modulation induced by the forward biased diode helps reducing the on-resistance of the whole device.

To investigate the impact of device shrinking on its ESD robustness, the distance  $D$  separating In/Out and Ground junctions is varied from  $35\mu\text{m}$  to  $65\mu\text{m}$  for “surrounded” diodes and from  $65\mu\text{m}$  to  $130\mu\text{m}$  for “lateral” diodes.

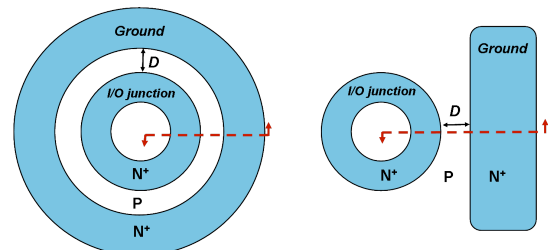


Fig. 1. Top view of “surrounded” (left) and “lateral” (right) back-to-back diodes. These naming, “lateral” and “surrounded” is related to the rectangular and circular geometry of the ground junction.

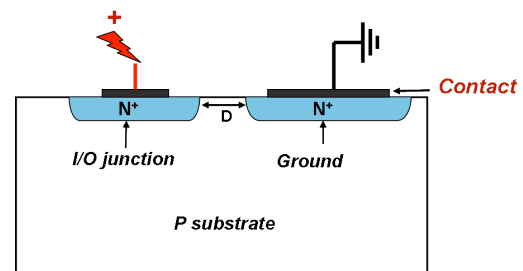


Fig. 2: 2D cross section of “lateral” and “surrounded” back-to-back diodes. The visualization is done through the dashed line in Fig. 1.

Positive stresses are the most stressful for the device because the smallest junction is reversed biased in this configuration. Indeed the reversed biased junctions locally develop hot spots in the device during ESD stress due to avalanche generation. Furthermore, the surface of the ground

junction being much larger than the one of the I/O junction (Fig. 1), the current density in the I/O junction is much higher than in the ground junction. It results that these devices are weaker for positive stress configuration. This was experimentally evidenced and for this reason we will only consider positive stresses in this paper.

### B. Test Setup

The ESD robustness of the studied devices is tested by applying a current pulse with a generator compliant to IEC61000-4-2 standard. This standard is intended to simulate a person discharging into a device while holding a metallic tool. Basically the discharge is modelled by a 150 pF capacitance discharging through a 330  $\Omega$  resistor [6]-[7]. IEC 61000-4-2 is designed to guarantee the immunity of electronic systems to ESD. However, although its application is not adapted to integrated circuits, this is an increasing request from system designers. To extend the application of IEC 61000-4-2 to integrated circuits and ensure a reliable measurement method, a standard practice was proposed by ESDA: the Human Metal Model (HMM) that reproduces the IEC 61000-4-2 waveform that simulates the discharge of a person through a metallic tool.

To overcome the issue of non reproducible results with ESD guns, an alternative method was proposed to generate IEC pulse waveforms with a 50  $\Omega$  transmission line tester [1]. In this work, the Barth 4702IEC-50 test system is used to deliver HMM pulses up to 30 kV according to the IEC 61000-4-2 standard and following ESDA HMM recommendations.

To define the ESD stress level for repetitive testing, structures under study are electrically characterized between I/O junction and Ground. In this paper, measurement are carried out with an IEC gun tester on packaged devices mounted on a Printed Circuit Board (PCB) with 50  $\Omega$  traces which was provided by the customer.

### III. SINGLE AND REPETITIVE ESD ROBUSTNESS COMPARISON

In this section, we demonstrate that protection devices can be weaker when stressed with multiple surges [8]. Furthermore, “lateral” and “surrounded” structures present different behaviors, which allows suspecting two distinct failure mechanisms.

In the following, HMM single ESD robustness is actually defined as the pass/fail results of three positive pulses followed by three negative ones applied to the device under test.

The single ESD robustness level is defined as a guaranteed maximum ESD voltage the device can survive without any change of its low-current static DC I-V characteristic.

After each series of pulses, the low-current static DC I-V characteristic of the component is monitored and compared to the initial one. If the component passes the test, ESD pulse voltage is incremented until an electrical failure is detected.

The number of three pulses is chosen to minimize the repetition of stresses to the device during a single ESD robustness characterization. This choice was made to clearly

differentiate single from repetitive robustness test method. Nevertheless, our investigation showed that despite the rather short series of pulses (e.g. below 5 pulses), the device degradation is always observed during the first pulse. The remaining pulses are actually applied to guarantee that the device under test effectively sees the selected ESD current level. This is to overcome any tester malfunction issues, even if such problem was not identified with the testers used in this study.

On Fig. 3, the results of ESD robustness obtained using HMM and IEC testers are compared in order to illustrate the measurement correlation. It has to be noticed that there is a good correlation of the ESD robustness between packaged devices tested with an IEC gun and with a Barth 4702IEC-50 testers. We also observed an excellent agreement between devices tested at wafer level and packaged ones using the Barth tester. Nevertheless it is worth underlining that any general and universal correlation law could be defined from these results.

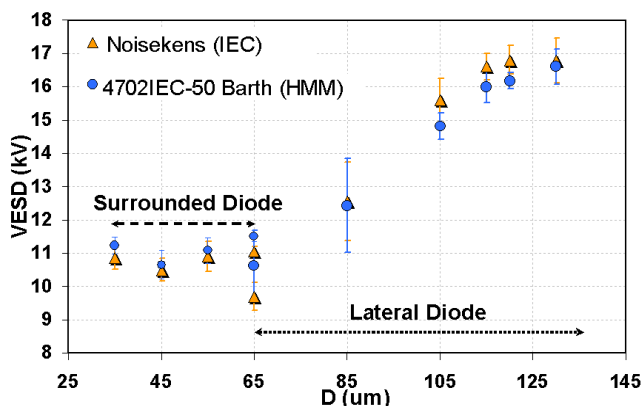


Fig. 3: Single ESD robustness for “surrounded” and “lateral” bidirectional ESD protection diodes as a function of distance D. Robustness obtained from IEC and HMM testers on packaged devices are compared here.

In Fig. 4, single stress ESD robustness is reported in a Box Plot graph [9]. Medians, represented by dashes inside the boxes, correspond to the middle-value of the dataset. 17 devices were tested for each distance. In summary, reducing the structure dimensions (smaller D distance) results in lower ESD performances. This impact is much more significant for “lateral” structures that have larger D distances than the “surrounded” ones. Indeed, their ESD robustness varies from about 18kV for the largest D down to 11kV for the shortest one.

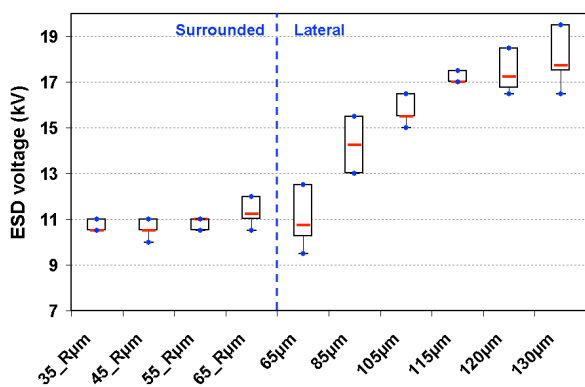


Fig. 4: Single ESD robustness for "surrounded" (left part of the graph) and "lateral" (right part of the graph) bidirectional ESD protection diodes as a function of distance D in a BoxPlot graph. Medians represented by dashes inside boxes, correspond to the middle value of the dataset for 17 components and are actually close to the average value.

It has to be noticed that the studied devices failed for an HMM voltage higher than 9kV. As a result, the failure level of these devices cannot be assessed with typical and broadly available HBM, CDM or TLP test equipments that would not deliver enough current nor discharge energy compared to system-HBM (HMM) stress. This is the main reason that motivated the use of HMM stress type, which is compliant with the stress levels required for our application.

Repetitive robustness testing consists in applying at 1 Hz frequency an ESD pulse whose voltage  $V_{ESD}$  is lower than the single ESD robustness level. To characterize components in a repetitive mode, three different stress levels, respectively at 70%, 80% and 90% of the single ESD robustness median values, were used in this study and are summarized in the tables below.

Table I: Summary of ESD robustness measured for: a) "lateral" diodes and b) "surrounded" diodes. Minimum, median and maximum are given in order to show the scattering of single-ESD-measurement-results. This is important to choose an appropriate repetitive stress level in order to investigate on failure mechanisms that are independent of the single ESD stress ones and thus specific to the repetitive stress mode.

a) "Lateral diodes"

Distance ( $\mu\text{m}$ )	65	85	105	115	120	130
Min Robustness (kV)	9.5	13	15	16	16.5	16
<b>Median (kV)</b>	<b>10.5</b>	<b>13.7</b>	<b>15.5</b>	<b>17</b>	<b>17.2</b>	<b>17.5</b>
Max Robustness (kV)	12.5	15.5	16.5	17.5	18.5	19.5
70% Median (kV)	7.3	9.6	10.8	11.9	12.1	12.2
80% Median (kV)	8.4	11	12.4	13.6	13.8	14
90% Median (kV)	9.4	12.3	13.9	15.3	15.5	15.7

b) "Surrounded" diodes

Distance ( $\mu\text{m}$ )	35	45	55	65
Min Robustness (kV)	10.5	10	10.5	10.5
<b>Median (kV)</b>	<b>10.5</b>	<b>10.5</b>	<b>11</b>	<b>11.5</b>
Max Robustness (kV)	11	11	11.5	12.5
70% Median (kV)	7.4	7.4	7.7	8

80% Median (kV)	8.4	8.4	8.8	9.2
90% Median (kV)	9.5	9.5	9.9	10.3

The number of pulses required to degrade the protection diodes is reported in Fig. 5 as a function of the geometry and ESD stress levels. The robustness in a repetitive stress mode is improved with distance D for "surrounded" diode, whereas for "lateral" one, increasing D leads to an overall decrease in the repetitive robustness.

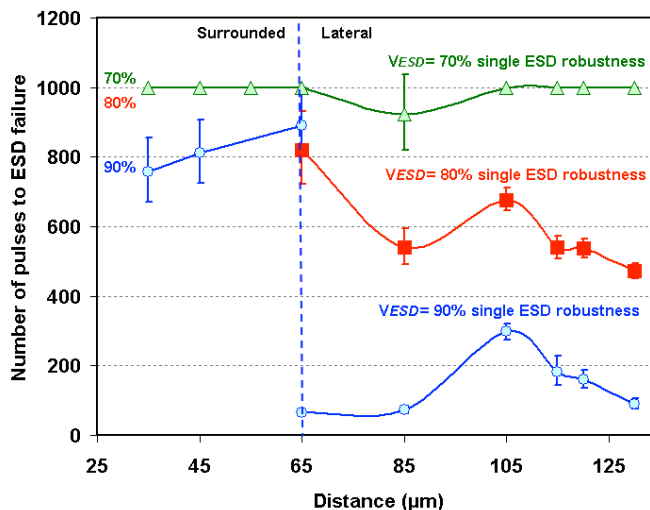


Fig. 5. Repetitive ESD robustness as a function of distance D for "surrounded" (left part of the graph) and "lateral" (right part of the graph) ESD protection diodes.  $V_{ESD}$  stress levels are applied at 70%, 80% and 90% of the median single-ESD robustness (Fig. 4).

The "lateral" components with 65 $\mu\text{m}$ , 85 $\mu\text{m}$  and 130 $\mu\text{m}$  distances stressed at 90% of their single robustness failed with a low number of pulses compared to the other devices (Fig.4). This has to be related to the spreading of the single-stress robustness results (Table.1). The spreading is indeed relatively important for these devices which mean that several devices repetitively stressed at 90% of the median are actually degraded in a single-stress way. Given this dispersion, the "lateral" devices characterized in repetitive mode at 90% of their median single-stress robustness are actually failing in both failure modes (single and repetitive) thus making the results difficult to interpret in a straightforward way.

To summarize, on the one hand, at 90% of the median, all "surrounded" and "lateral" diodes have been degraded by less than 1000 stresses. On the other hand, almost all kinds of diodes are robust to more than 1000 stresses when the repetitive stress level is chosen at 70% of the median.

In order to discriminate and understand the repetitive failure mechanism based on failure analysis, it is important to select an ESD stress level where results would be meaningful. Consequently, a failure analysis was carried out on "surrounded" devices stressed at 90% of single ESD robustness level since at 70% and 80% no electrical degradation was observed after 1000 stresses. For "lateral" diodes, the devices stressed at 80% of the median were selected. Indeed, for this devices, almost no electrical degradation was observed at 70% of the median and at stress

level at 90% of the median, the failure level is within the scattering of single stress robustness levels, which would not allow discriminating whether the devices failed in a repetitive or single stress mode.

#### IV. DISCUSSION

As shown previously, failure mechanisms of protection devices against system level ESD stress including repetitive stress appear to depend on device geometry. We have actually identified three distinct failure modes of different severity detailed in the following sections. First, repetitive ESD surges generate charge traps at the silicon oxide interface, which increases the leakage current in a reversible way. The second failure mode is particularly related to devices presenting an inhomogeneous current distribution, such as “lateral” diode, that can suffer of metallic spiking into the contact. The last common observed fatal failure is independent of the diode structures and corresponds to a melted filament at the junction periphery in the silicon bulk. Details of the failure mechanisms of each structure are described hereafter.

##### A. Physical Mechanisms

In “lateral” diodes, repetitive ESD stress induces multiple melted points due to metal spiking located at the shorter distance between I/O and ground and close to the I/O junction contact opening (Fig. 6). In contrast, in “surrounded” diodes, a unique melted filament is observed at the junction periphery (Fig. 7). We should notice that both failures are generated deep into the bulk of the substrate.

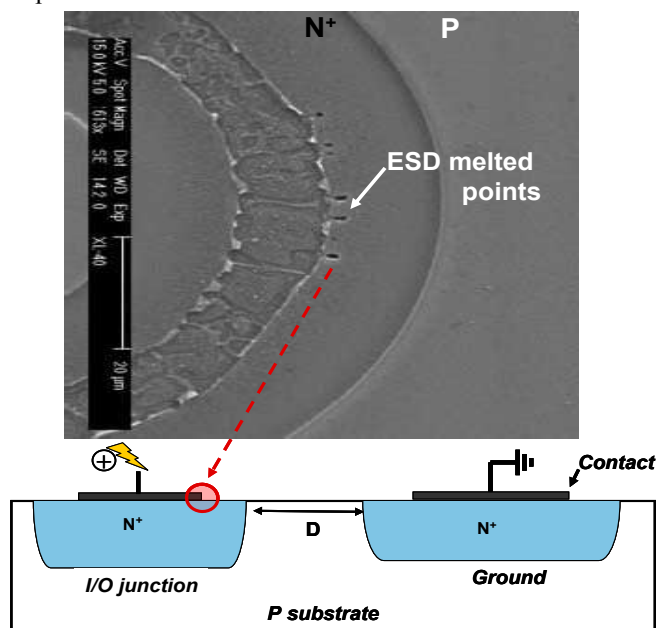


Fig. 6. Failure decoration using “Wright etch” [10] technique, followed by SEM inspection for “lateral” bidirectional ESD protection diodes with a  $D=105\ \mu\text{m}$ . Note that all other distance presents the same failure characteristic for “lateral”-geometry diodes.

An inhomogeneous current distribution resulting from the ground position for the “lateral” diode is suspected to induce metal diffusions at the contact opening during cumulative ESD stresses. However, the fatal degradation occurs thermally

when the I/O junction reaches locally the silicon-melting temperature.

“Surrounded” diodes present a uniform current distribution due to the uniform distance between I/O and ground diffusions [11]. This physical behavior results in a better reliability toward repetitive ESD surges compared to “lateral” components.

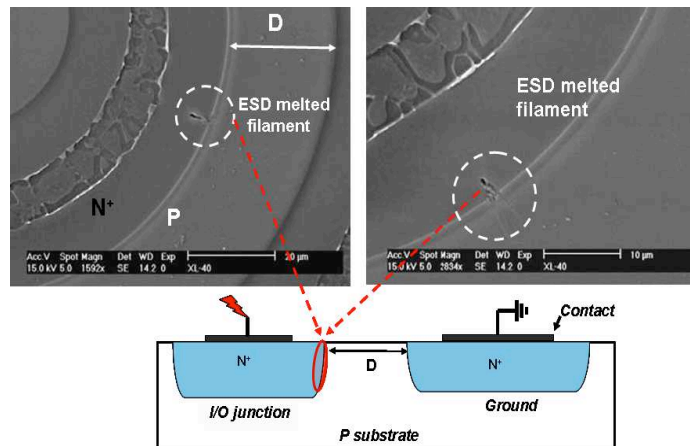


Fig. 7. Failure localization and visualization by chemical decoration followed by SEM inspection for “surrounded” bidirectional ESD protection diodes.

##### B. Electrical Mechanisms

Fatal failure induces more than two decades increase in leakage current and a drastic reduction of the breakdown voltage. However, during pulses repetition, we also observed an increase of the leakage current that is activated by charge trapping at the silicon-oxide interface [12]. In the following, it is demonstrated that melted points, melted filament and the small rise of leakage current are three phenomena independent from each other. By analyzing the localization of melted-points with regard to the junction, we investigated the influence of physical failures on the initial DC I-V characteristic.

On Fig. 8 DC I-V characteristics show a relatively slight increase of the leakage current compared to a fresh device [13].

After ESD surges, a thermal treatment of the device at  $125\ ^\circ\text{C}$  during 24 h reveals that the leakage current increase induced by ESD can be cured, thus demonstrating that this type of degradation is reversible.

It might be surprising to observe a lower leakage current after annealing than before any stress. This is however expectable as the fabrication process itself creates charge traps at the silicon-oxide interface leading to some level of leakage current. These traps states related to fabrication are also cured by the thermal treatment, thus resulting in a leakage current which is lower than the fresh devices one.

The small electrical degradation during repetitive stress corresponds to a raise of the leakage current lower than two decades. Moreover, no dependence of this current increase with the distance  $D$  has been identified. In fact, if not related to a fatal degradation, the leakage current increase varies in a random way for each device. In Fig. 8, a “surrounded”  $55\ \mu\text{m}$  and “lateral”  $115\ \mu\text{m}$  diode subjected to 200 repeated pulses have been selected to illustrate this behavior.

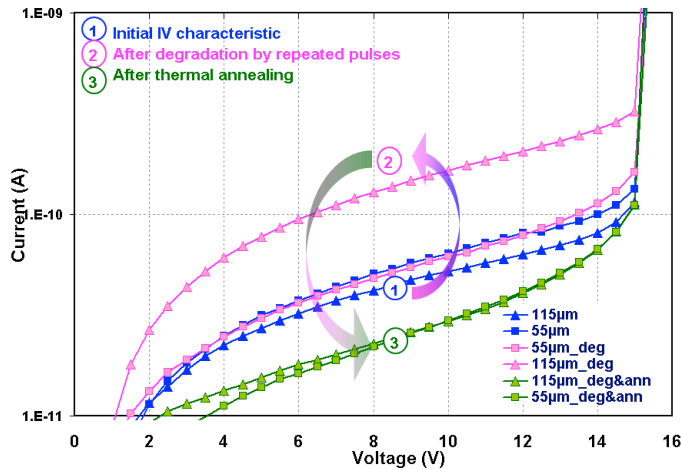


Fig. 8. Evolution of the leakage current of a “lateral” diode with  $D=115\mu\text{m}$  and a “surrounded” component with  $D=55\mu\text{m}$ : DC I-V characteristic measured for a fresh diode before any stress (1), after repetitive ESD surges (200 pulses) (2), and after thermal annealing at  $125^\circ\text{C}$  during 24 h (3).

In addition, chemical decoration of the defects was performed on the “lateral”  $115\mu\text{m}$  diode and the “surrounded”  $55\mu\text{m}$  component both electrically degraded and thermally cured as described in the previous paragraph. Identical electrical signatures are observed before and after annealing (Fig.8 left and Fig.6). Therefore, no correlation exists between static DC I-V characteristic evolution and melted points, thus appearing as two totally uncorrelated phenomena.

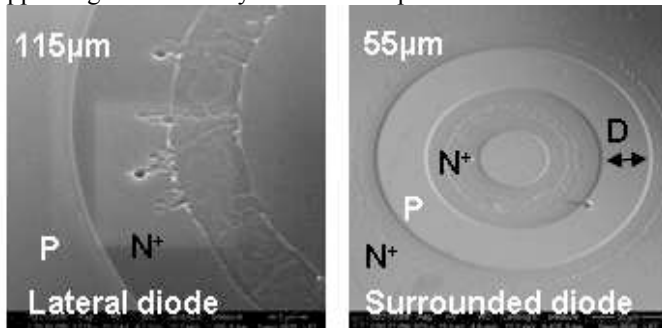


Fig. 9. Physical characterization for “lateral” (left picture) and “surrounded” (right picture) ESD protection diodes after 200 successive HMM pulses followed by thermal annealing. Chemical decoration and SEM inspection has been performed while fatal electrical degradations are not reached in these referenced conditions.

For the “surrounded” diode, a failure analysis was carried out before reaching a fatal electrical degradation: no surface defects are visible (Fig.9 right) despite the leakage current increase. This complementary result strengthened the fact that DC I-V characteristic evolution and melted filaments are not directly related. Therefore, the fluctuation of the leakage current for a fresh device, before and after annealing can be attributed to oxide charge (de)trapping.

### C. Impact of the $D$ distance

The electrical and physical observations made in the previous sections show that repetitive robustness of “lateral” diodes is reduced when increasing  $D$  whereas single stress robustness is improved. This is related to the two different failure modes taking place during single-stress and repetitive-

stress.

For single stress the failure of all devices is related to local silicon melting at the P-N junction. This indicates that current crowding leading to localized overheating and formation of a thermal hot spot in the region of highest electric field is the root cause of the observed degradation. Increasing  $D$  distance improves the current uniformity, which delays the onset of thermal runaway and consequently increases the single-stress robustness.

For repetitive-stress on “lateral” device, the failure mechanism is different and is related to electromigration of the metallic contact induced by high currents densities. Increasing  $D$  distance, while being favorable to delay the onset of thermal runaway at the junction, also results in an increased series resistance of the device and consequently to an increase of the total power dissipated at a given current level. This increased power dissipation generates a higher joule heating, which accelerates the metal spiking at the contact opening and thus induces a decreased repetitive robustness with increased  $D$  distance.

## V. CONCLUSION

The device geometry of the protection has an influence on failure mechanism related to multiple ESD stresses. Depending on the involved degradation process, long-term robustness may or may not be affected. To summarize three different degradation modes are identified which have different severity levels:

- Melted filament at the junction corresponds to the standard and catastrophic failure, which induces a large and irreversible leakage current increase. This is the failure always observed for single pulse stress degradation.
- Oxide charge trapping induces an increased leakage current. This degradation is reversible and the rise of the leakage current may not have any impact depending on application.
- Contact metal spiking, which does not affect leakage current at the beginning of the failure mechanism, induces the formation of metal filament. However, with cumulated stresses, it results in a fatal device failure suspected to be related to a higher focalization of the discharge current into the spiking area leading to higher local heating and accelerated spiking progress through an electromigration phenomenon [14]. This failure mechanism should be avoided in protection structure as they really reduce the long-term device robustness.

## REFERENCES

- [1] T.J. Maloney and N. Khurana, “Transmission Line Pulsing techniques for circuit modeling of ESD phenomena,” in *Proc. EOS/ESD Symp.*, pp.49-54, 1985.
- [2] T. Smedes, R. Velghe, R. S. Ruthand, A. J. Huitsing “The application of transmission line pulse for the ESD analysis of integrated circuits,” in *Journals of electrostatics*, 2002.
- [3] D. Johansson, M. Mayerhofer, J. Willemen, U. Glaser, D. Pogany, E. Gornik, and M. Stecher, “Avalanche breakdown delay in high-voltage p-n junctions caused by pre-pulse voltage from IEC 61000-4-2 ESD generators,” in *IEEE Trans. Devices Mat. Reliability*, Vol. 9, no. 3, pp. 412-418.
- [4] Z. Pan, S. Holland, D. Schroeder, and W.H. Krautschneider, “Understanding the Mechanisms of Degradation and Failure Observed

- in ESD Protection Devices Under System-Level Tests,” in *IEEE Trans. Devices Mat. Reliability*, Vol. 10, No. 2, pp. 187-191, 2010.
- [5] S. Thijs, M. Scholz, D. Linten, A. Griffoni, C. Russ, W. Stadler, D. Lafontese, V. Vashchenko, M. Sawada, A. Concannon, P. Hopper, P. Jansen and G. Groeseneken, “SCCF-System to Component level Correlation,” *EOS/ESD Symp.*, pp. 157-166, 2010.
- [6] R. Chundru, D. Pommerenke, K. Wang, T. V. Doren, F. P. Centola, and J. S. Huang, “Characterization of Human Metal ESD reference Discharge Event and Correlation of generator Parameters to Failure Levels-PartI: reference Event,” in *IEEE Trans. Electron Compatibility*, Vol. 46, No. 4, Nov. 2004.
- [7] *Electromagnetic Compatibility (EMC) Part 4-2*, “Testing and Measurement Techniques -Electrostatic discharge immunity test,” IEC 61000-4-2 ED-1.2, 2001-2004.
- [8] I. Laasch, H. M. Rittner, A. Werner, “Latent damage due to multiple ESD discharges,” in *EOS/ESD Symp.*, 2009
- [9] D. F. Williamson, R.A. Parker, J. S. Kendrick, “The Box Plot: a simple visual method to interpret data,” in *Anneals of internal medicine*, Vol. 110, No. 11, June 1989.
- [10] M. Wright. Jenkins, “A new preferential etch for defects in silicon crystals,” in *J. Electrochems. Soc.*, p757-762, May 1977.
- [11] A. Salman, S.Beebe, M. Pelella, G. Gilfeather, “SOI Lateral diode optimization for ESD protection in 130nm and 90nm technologies,” in *EOS/ESD Symp.*, Sept. 2005.
- [12] G. Barletta, G. Curro, “Junction leakage current degradation under temperature reverse-bias stress induced by band-defect-band tunneling in power VDMOS”, in *Microelectronics and Reliability*, Vol. 45, No. 5-6, pp. 994-999, 2005.
- [13] Donald G. Pierce, “Electro-Thermomigration as an electrical overstress failure mechanism,” in *EOS/ESD Symp. Proc.*, pp. 67, 1985.
- [14] J.R. Black, “Electromigration failure modes in aluminum metallization for semiconductor devices,” in *Proc. of the IEEE*, Vol. 57, No. 9, Sept. 1969