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**Porous SiOCH integration:  
Etch challenges with a trench first metal hard mask approach**

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The use of a metallic hard mask approach for porous dielectric film integration implies for patterning processes, different difficulties like dimensional control, bottom line roughness and residue formation or chamber conditioning. In this paper we propose to present these issues and associated solutions for p-SiOCH integration in dual damascene structure using a trench first metallic hard mask approach.

## I. Introduction

The choice of copper/ultra low-k interconnects architecture is one of the key building blocks for integrated circuit performance, process manufacturability and scalability. Many low-k materials have been proposed as silicon containing (silica-based and silsesquioxane) or non silicon containing materials [1]. Finally, from the 90 nm technological node, the semiconductor manufacturers opted to go with methyl groups (Si-CH<sub>3</sub>) containing organosilicate materials close to the well known silicon dioxide (SiO<sub>2</sub>) [2]. The SiOCH trench patterning can be achieved using different hard mask strategies (metallic or organic hard masks), all presenting different advantages and drawbacks in terms of selectivity, faceting, etc. [3]. But from the 45nm interconnect technology node, with porosity introduction into SiOCH materials, the metallic hard mask strategy appears to be a promising integration scheme compared to a full organic hard mask approach. Indeed with porosity introduction, the dielectric film presents a high sensitivity upon fluorocarbon (FC) etching [4] and ashing plasma exposures [5] which can lead to dielectric constant increase and reliability degradations. In this context, the metallic hard mask integration provides a greater compatibility with porous dielectric materials than the organic hard mask approach since no ashing step is required. However, in all cases, etching processes involved in dual damascene structures fabrication generate serious issues. In this paper we propose to present and discuss the porous SiOCH (p-SiOCH) integration difficulties using a trench first metallic hard mask integration scheme (TFMHM) with the following stack: starting from the silicon substrate: a silicon-carbonitride layer deposited by plasma-enhanced-chemical vapor deposition (PECVD SiCN) / porous carbon-doped silicon-oxide (PECVD p-SiOCH, 25% porosity, k = 2.5) / PECVD silicon dioxide (SiO<sub>2</sub>) / titanium nitride deposited by physical vapor deposition (PVD TiN). We will focus on problems encountered during metal hard mask (MHM), via and line etching steps with associated solutions.

## I. Metal hard mask opening

A thin metallic hard mask layer is deposited on the top of a dense dielectric layer ( $\text{SiO}_2$ ) which encapsulates the underlying ultra low-k material. The trench photolithography is performed using a positive tone photoresist coupled with a bottom antireflective layer (BARC) (Fig. 1(a)). The BARC and titanium nitride layers are etched using a chlorine-based chemistry in a dedicated transformer-coupled plasma (TCP) (Fig. 1(b)).

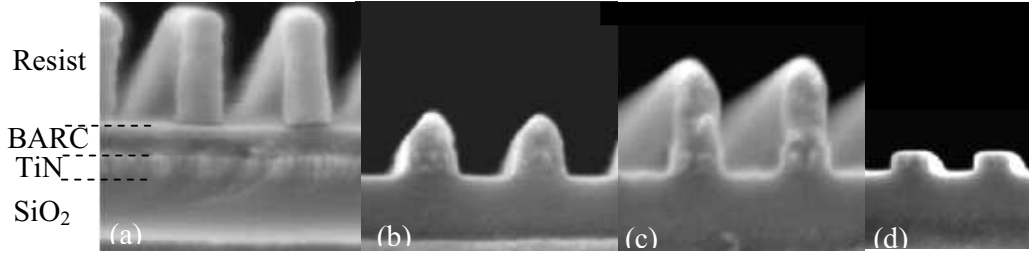


Fig. 1: Sequence of metallic hard mask opening from line lithography (a), BARC and hard mask opening with either chlorine only (b) or with methane addition (c) chemistries followed by the resist removal with an  $\text{O}_2$  based plasma (d).

The control of line dimensions is fine tuned during this step by playing with the different plasma parameters (like RF bias voltage) or TiN over-etch time. But the low etching resistance to resist during the TiN etching combined with the shrink in resist thickness at each new technological node makes this step very critical. The solution to overcome this issue is either to develop new metallic hard mask etch chemistries, like methane-based chemistries allowing a two-times selectivity improvement to the resist (Fig. 1(c)), or to transfer the line into the metallic hard mask using a tri layer approach (not shown here). In this later case, the line dimension is fine tuned by playing on the  $\text{CF}_4/\text{O}_2$  ratio during the SiARC opening. Then the organic planarized layer (OPL) and TiN layers are opened using  $\text{NH}_3$ - and chlorine- based chemistries, respectively. After TiN opening, the remaining resist (for the conventional approach) or OPL (for the tri-layer approach) are removed using an  $\text{O}_2$ -based (Fig. 1(f)) or  $\text{He}/\text{H}_2/\text{O}_2$  downstream plasmas, respectively.

## II. Partial via opening

The shallow hard mask topography, is then planarized with an organic BARC and the via lithography is performed (Fig. 2(a)).

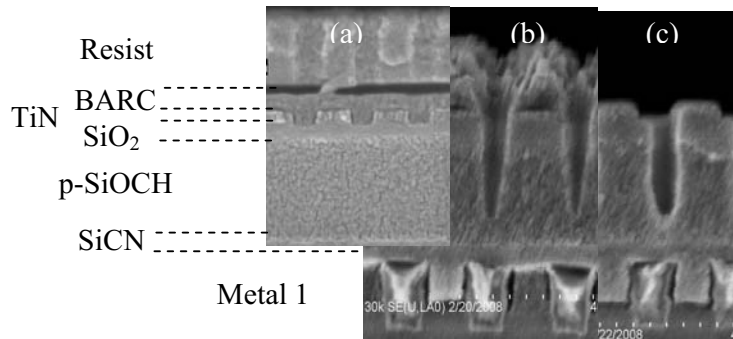


Fig. 2: Sequence of partial via etching from via lithography (a), BARC/ $\text{SiO}_2$ /p-SiOCH etching in FC based plasma (b) followed by resist removal in  $\text{O}_2$  plasma (c)

The via is partially etched into the p-SiOCH material using a fluorocarbon (FC) chemistry in a capacitive coupled plasma (CCP) etcher (Fig. 2(b)). Similarly to MHM etching, the problem during this step is the low selectivity to the resist which becomes a major problem to control the via dimensions. Furthermore, a highly physical etching step used to sputter the TiN in the misaligned vias can lead to arcing in the plasma chamber. The solution is the use of a tri layer approach previously described. In this case the via dimension is fine tuned by the  $\text{CF}_4/\text{O}_2$  ratio during the SiARC opening then the OPL and dielectrics ( $\text{SiO}_2+\text{p-SiOCH}$ ) are open using  $\text{NH}_3$ - and FC-based chemistries, respectively. The remaining resist or OPL are removed by an  $\text{O}_2$  (Fig. 2(c)) or  $\text{NH}_3$  plasma, respectively.

### III. Via-line etching

The last step in the p-SiOCH via-line patterning using a TFMHM approach is the via-line etching processed with the same fluorocarbon (FC) based chemistry followed by the etch-stop layer (SiCN) opening with a  $\text{CH}_3\text{F}/\text{CF}_4/\text{N}_2/\text{Ar}$  chemistry. But this step must be optimized in order to overcome the different issues that we will present.

#### III.1 Bottom line roughness and hard mask faceting

The two first problems encountered during the line-via etching, using low polymerizing FC chemistry at substrate temperatures above  $50^\circ\text{C}$ , are the hard mask faceting in via-line misaligned structures (Fig. 3(a)) and bottom line roughness formation (Fig. 3(b)). In the first case, it is difficult to control the line-via dimensions which can lead to short defects while the second issue degrades the time dependent dielectric breakdown.

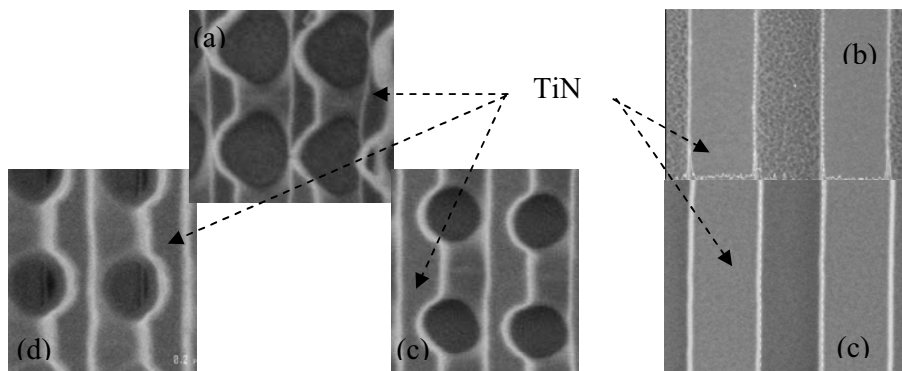


Fig. 3: Top view of problems encountered during via/line etching using a low polymerizing chemistry at substrate temperature above  $50^\circ\text{C}$ : hard mask faceting (a), bottom line roughness (b). High polymerizing chemistry at substrate temperature above  $50^\circ\text{C}$  allows to solve both issues (c) while developing low polymerizing chemistry at substrate temperature lower than  $50^\circ\text{C}$  improves TiN faceting (d).

#### III.1.1 Mechanism of TiN etching and bottom line roughness formation

Previous studies on the p-SiOCH etching in fluorocarbon-based plasmas using TiN as a hard mask reported that the TiN etching is mainly driven by an ion-assisted chemical etching mechanism, and that the etch rate, increasing with temperature, is controlled by the fluorine concentration in the plasma gas phase, and the ion bombardment density and energy [3]. The p-SiOCH roughness formation is explained by different mechanisms like intrinsic roughness or micromasking (coming from reactor wall conditioning or FC species), increased by the low volatility compounds ( $\text{TiF}_x$ ) coming from the sputtered hard mask.

### III.1.2 Solutions

The solution to limit the metallic hard mask faceting during line-via etching is to develop process at temperature lower than 50°C to reduce TiN etching reaction (Fig. 3(e)). However, this can lead to profile distortions [3] and bottom line roughness increase due to (in both cases) the condensation of non-volatile  $TiF_x$  compounds coming from the TiN mask sputtering. Finally, using a metallic hard mask approach, the best way is to develop etching processes at substrate temperature above 50°C (to limit sputtered metal species condensation leading to micromasking) with a highly polymerising chemistry to protect the MHM (Fig. 3(d)) and prevent the p-SiOCH surface roughening (Fig. 3(c)) [6].

### III.2 Residues formation

The metallic hard mask approach suffers also from specific issues such as the growth of metallic residues on top of the mask after dielectric materials etching in fluorocarbon-based plasmas (Fig. 4(b)). These residues grow with air exposure time and are not removed after conventional wet cleaning steps (basic solution + 0.1%HF) (Fig. 4(b)). They prevent a good metal barrier deposition conformity, which generates via or line opens (Figs. 4(d) and 4(e), respectively) after chemical mechanical polishing (CMP) and strongly impacts the electrical yield (Fig. 4(c)).

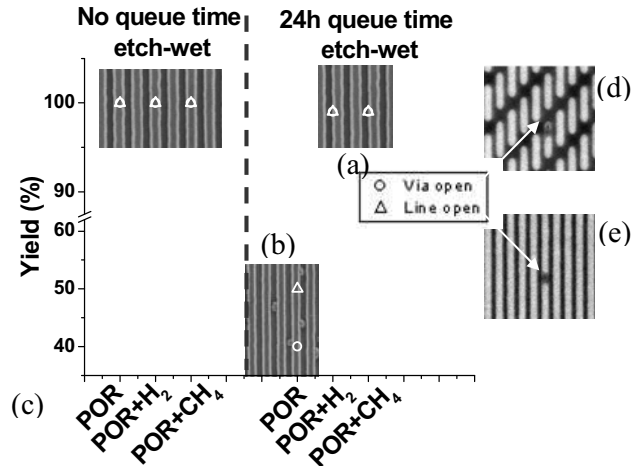
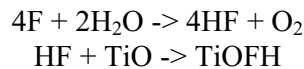


Fig. 4: Study of residue formation with (a) and without (b) in-situ post etch treatment addition after etching and one day air exposure. Effect on yield as a function of the waiting time between etch and wet steps (c) with the formation of defects like via (d) and line (e) opens.

#### III.2.1 Mechanism

The mechanism of formation was attributed to fluorine species reacting with the titanium nitride and catalyzed by air moisture. More precisely, fluorine species present on the TiN surface after plasma exposure react with air moisture from the atmosphere leading to HF formation. HF reacts with the partially oxidized TiN surface and forms metallic salts through the following sequence [7]:



Therefore, the solution to avoid the metallic residue formation is to act on the acid formation by either removing the fluorine or to avoid the reaction with the air moisture.

### III.2.2 Solutions

Different *in situ* post-etch plasma treatments such as hydrogen- and methane-based plasmas are efficient to avoid residue formation after one day air exposure (Fig. 4(a)), strongly improving the yield (Fig. 4(c)). This efficiency was explained by the fact that hydrogen-based plasmas act on the kinetic of residue formation by removing the fluorine concentration on top of the titanium nitride layer. With methane-based chemistries, the formation of a carbon and nitrogen based passivation layer on top of the titanium nitride layer prevents the reaction with air moisture [8].

The compatibility and benefit (on reliability) of methane PET addition with porous SiOCH integration using TFMHM has been demonstrated for 45nm interconnect technology node [9].

### III.3 Dielectric line undulation

With the constant scaling down of dimensions, etching process steps are facing new issues. Indeed, with patterning of sub-50 nm porous SiOCH trenches using a metallic hard mask approach, a line undulation phenomenon, also called line wiggling, is observed (Fig. 5(b)). Mechanical simulations performed using the ANSYS™ code [10] show this line undulation is due the compressive residual stress of the metallic hard mask (Fig. 5(a)) combined with the p-SiOCH film thickness (not shown). The Young moduli of the metallic hard mask and the p-SiOCH also play a role on the wiggling formation but in second order compared to the previous parameters (not shown).

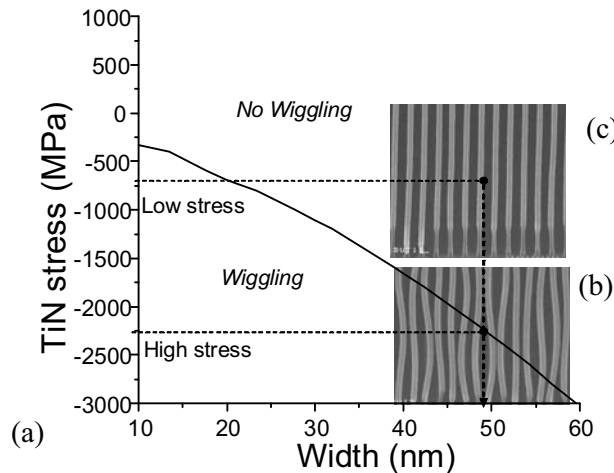


Fig. 5: Comparison of the line wiggling formation between simulation prediction (a) and experimental results as a function of the line dimension for the stack 20nm SiCN/ 290 nm p-SiOCH/ 40nm SiO<sub>2</sub> with high (b) and low (c) TiN residual stress.

Therefore, one solution to continue the porous material integration with a metallic hard mask for advanced interconnect technology nodes is to develop TiN materials with lower residual stresses and thicknesses (Fig. 5(c)). In addition, the effect of the p-SiOCH film thickness on line undulation will be minimized for advanced technology node, since the p-SiOCH thickness continuously decreases (aspect ratio almost constant).

## IV. Chamber conditioning

The use of a TFMHM has also a strong effect on process stability and reproducibility. Indeed, with this metal hard mask approach, a drift of the line etching processes (etch rates, uniformity) and lower mean time between cleans (compared to the use of an

organic hard mask) are observed when using non heated top electrode with a standard clean procedure ( $O_2$  plasma). The main cause is the chamber defectivity increase after several RF hours of etching process (Fig. 6(a)) due to the formation of micromasking on silicon top electrode induced by Ti etched by product redeposition.

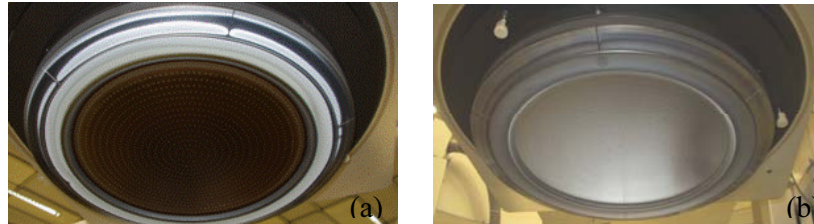


Fig. 6: Observation of (a) non heated and (b) heated ( $>100^\circ\text{C}$ ) top electrodes after more than 500 Rf hours processes.

A solution to delay this chamber defectivity is to heat the top electrode (above  $100^\circ\text{C}$ ) to limit Ti species redeposition and thus silicon micro-masking (Fig. 6(b)). A second possibility is to clean up the reactor walls after each wafer being etched by developing appropriate plasma clean processes. For instance, Chevolleau et al. propose to use a  $SF_6$  plasma to remove the fluorocarbon layer and Ti based species followed by an  $O_2$  flash plasma to clean up the chamber walls from the remaining carbon [11].

## V. Conclusion

Major difficulties of the p-SiOCH material integration using a TFMHM integration have been presented from the etching point of view. The first problem encountered during the hard mask and partial via etching is the low selectivity to resist leading to dimensional control issue. The use of a tri layer approach can solve this problem. While during via-line etching we are dealing with hard mask faceting, bottom line roughness and residue formation or line undulation. In this case the use of TiN hard mask with a low residual stress and thickness but also the development of highly polymerizing chemistries followed by *in situ* post etch treatment addition at high substrate temperature (above  $50^\circ\text{C}$ ) are required. Finally, with the use of a metallic hard mask, reactor cleaning strategies must be revisited to allow better process stability and reproducibility.

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