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DESIGN OF A HIGH VOLTAGE INPUT – OUTPUT RATIO DC-DC CONVERTER DEDICATED TO SMALL POWER FUEL CELL SYSTEMS

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Abstract

Consuming chemical energy, fuel cells produce simultaneously heat, water and useful electrical power [1] [2]. As a matter of fact, the voltage generated by a fuel cell strongly depends on both the load power demand and the operating conditions. Besides, as a result of many design aspects, fuel cells are low voltage and high current electric generators. On the contrary, electric loads are commonly designed for small voltage swing and a high V/I ratio in order to minimize Joule losses. Therefore, electric loads supplied by fuel cells are typically fed by means of an intermediate power voltage regulator. The specifications of such a power converter are to be able to step up the input voltage with a high ratio (a ratio of 10 is a classic situation) and also to work with an excellent efficiency (in order to minimize its size, its weight and its losses) [3].

This paper deals with the design of this essential ancillary device. It intends to bring out the best structure for fulfilling this function. Several DC-DC converters with large voltage step-up ratios are introduced. A topology based on a coupled-inductor or tapped-inductor is closely studied. A detailed modelling is performed with the purpose of providing designing rules. This model is validated with both simulation and implementation.

The experimental prototype is based on the following specifications: the fuel cell output voltage ranges from a 50 V open-voltage to a 25 V rated voltage while the load requires a constant 250 V voltage. The studied coupled-inductor converter is compared with a classic boost converter commonly used in this voltage elevating application. Even though the voltage regulator faces severe FC specifications, the measured efficiency reaches 96 % at the rated power whereas conventional boost efficiency barely achieves 91.5 % in the same operating conditions.

1 Introduction

Since the 19th, industrial expansion has always leaned on intensive use of fossil resources: coal, oil and natural gas [4]. At the beginning of the 21st century, governments gradually become aware of the limit of the hydrocarbon reserves [5]. On top of a secure and sustainable long-term energy supply, the huge use of hydrocarbon resources already proved to have negative impact on the earth environmental equilibrium. As a matter of fact, greenhouse gases such as carbon dioxide and methane have deeply and suddenly increased leading to a previous unknown situation [6]. For these two main reasons, finding out new energy alternatives has become a key issue of this century. In this context, hydrogen has attracted great attention in the recent years as a new and clean energy carrier. Hydrogen avoids the dependency and depletion of fossil fuels because it can be produced by different means and especially thanks to renewable resources (wind, sun ...) [7]. Furthermore, hydrogen has a good energy specific gravity (120 MJ/kg); no toxic gas is generated during its combustion, particularly in the case of the electrochemical oxidation and reduction reactions taking place in fuel cells; residue is only water and heat [8]. Therefore, fuel cells (FCs) are the most important field of the "hydrogen-energy" use. Theirs areas of application are various. It provides electric power to portable electronic devices, communication equipments, spacecraft power systems (electricity and water cogeneration), transport systems (cars, boats, and planes), and also buildings (electricity and warmth cogeneration), in a range of power from a few watts to hundred kilowatts.

However, FC is not an ideal voltage generator and the FC voltage becomes smaller as far as the load power demand increases. Indeed, the FC voltage-current relationship is induced by the three main irreversible losses that occur in the FC processes. Activation polarization (ΔV_{act}) is the irreversible voltage loss associated with overcoming the energy barrier to the electrode reaction and cathode (air) kinetic limitations dominate in this ΔV_{act} term. Ohmic losses are basically due to ionic current in the electrolyte whereas collector resistance and contact resistance (electronic current) are negligible. It induces an ohmic polarization (ΔV_{ohm}). Transport mechanisms within the gas diffusion layer and electrode structure cause a reactant concentration decrease at

the electrode surface and produce an irreversible voltage loss named concentration polarization (ΔV_{con}) [9]. As a conclusion, the actual fuel cell voltage (V_{FC}) at any given current (I_{FC}) can be represented as the reversible voltage (roughly the open-circuit voltage) minus the activation, ohmic and concentration voltage losses.

$$V_{FC} = E_{FC} - \Delta V_{act} - \Delta V_{ohm} - \Delta V_{con} \quad (1)$$

From a practical point of view, the electric load is strongly affected by an important voltage swing. In the worst case (aged FC and /or bad operating conditions), the fuel cell voltage can be divided by a factor of 2 when the required power rise from zero to a critical level. To face this huge voltage constraint, a power converter usually regulates the voltage delivered by the FC to the electric load (figure 1) [10] [11].

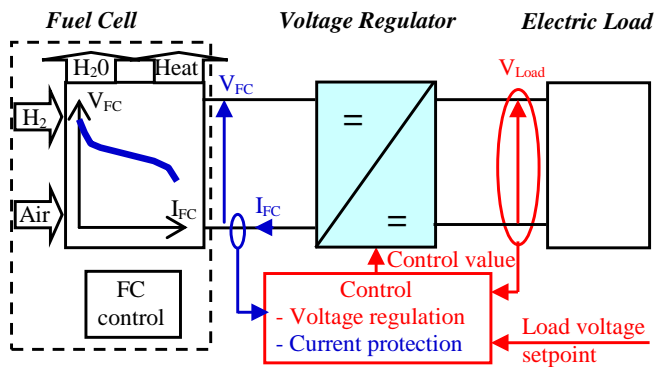


Figure 1. Block diagram of a FC electric generator

In addition, the voltage regulator specifications are quite special. As a matter of fact, the change in Gibbs free energy associated to the reduction/oxidation reactions lead to a 1.18 V standard theoretical cell potential, assuming a vapour water product. Even when no current is drawn from a fuel cell, there is irreversible voltage loss due to parasitic reactions which means that the practical open circuit voltage never exceeds 1 V. Now, in order to obtain homogeneous cells conditions (temperature, partial pressure, water draining, seal pressure ...), FC designer rarely stacks more than a thousand cells together. This practical choice induces that the FC is a low voltage and high current electric generator. As loads commonly behave the opposite way, the voltage regulator connecting FC and load has to raise the voltage value with a high ratio and to withstand high input voltage swing. The step-up voltage conversion ratio is usually about 10, and the voltage swing is typically about 1/2 with respects to open circuit voltage [12].

This paper focuses on the specific voltage regulator integrated in a FC system. The current investigations are limited to small power systems (from a few watts to 1 kW). This article is divided into four parts. First, it analyses various topologies based on a unique controlled power switch in order to bring out the more appropriate structure (section 2). Then, a detailed survey of this latter is carried out; taking components real characteristics into account (section 3). Third, an experimental study is developed to validate the effectiveness of this analysis. Last, comparative experiments allow

confirming and quantifying the importance of the proposed structure as far as classic boost converter is concerned. Finally, the conclusion remarks end the paper in section 6.

2 Power converters topology

2.1 General purpose

In order to obtain both a good efficiency and a safe operation, FC current density is limited. Hence, their electrodes areas define their rated current. With regard to their rated voltage, the FC voltage is limited because of the restricted number of elementary cells that can be connected in series. This optimal number depends on the application case but does not exceed much more than one hundred. On the contrary, the load is usually designed to minimize the Joule losses while taking voltage isolation constraints into account and thus it works with low currents. For small power, DC voltage bus commonly ranges from 300 V to 600 V.

Our experimental setup is based on a Nexa FC module designed by Ballard. It is made of 46 cells. Therefore, the proposed requirement is based on a 25 V rated FC voltage and on a 250 V load voltage reference. In addition, the FC voltage is assumed to fluctuate between 25 V and 50 V.

Based on these specifications, a specific DC power converter, adapted to small power requirements, is designed. As far as this scope of appliance is concerned, the key issues are cost and easy implementation. That is the reason why the power structure of this voltage regulator is restricted to single controlled switch topologies. The topology selection criteria are based on two key points. The first one relies on the switch voltage and current constraints. In order to compare each topology, a switch coefficient (F_s) is defined:

$$F_s = \frac{V_s I_s}{P} \quad (2)$$

Where V_s is the maximum switch voltage;
 I_s is the maximum switch current;
 P is the power supplied by the DC converter.

As conduction and switching losses have to be minimized, the lower the switch coefficient F_s is, the better the topology is. **Consequently, in any converter, current ripple has to remain small compared to maximum switch current; the current ripple will hence be neglected in the following survey.** On the other hand, some topologies are based on transformer or coupled inductors. In this case, it is also important to keep the transformer ratio close to one. As a matter of fact, greater or smaller voltage conversion ratio induces larger leakage inductance and also larger parasitic capacitance. Both elements significantly degrade the system performance [13].

2.2 DC-DC converter without transformer

In this application, galvanic isolation is not required. So, the conventional boost converter is a very straightforward way to

implement the voltage regulator function (figure 2). For this topology, the switch coefficient $(F_S)_{boost}$ is:

$$(F_S)_{boost} = \frac{V_{Load} I_{FC}}{V_{FC} I_{FC}} = \frac{V_{Load}}{V_{FC}} \quad (3)$$

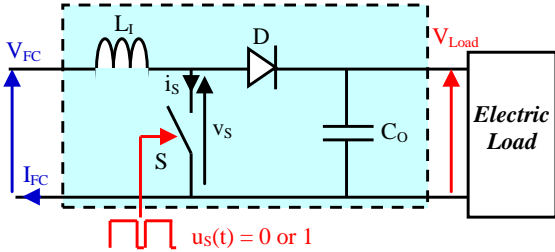


Figure 2. Conventional boost DC-DC converter

As this application requires extreme step-up voltage conversion ratios, $(F_S)_{boost}$ is high ($(F_S)_{boost} = 10$) which means a poor utilization of power components (S and D) and a degradation of the regulator efficiency. Furthermore the boost converter operates with the following duty-cycle $(d)_{boost}$:

$$(d)_{boost} = 1 - \frac{V_{FC}}{V_{Load}} \quad (4)$$

$(d)_{boost} = 0.9$ is very close from its upper limit which implies that it impairs transient response.

Considering this issue, two classic boost converters in cascade is no way to cope with the specifications since this solution needs two power switches which, on top of that, are difficult to drive properly because of a high order under damped resonant circuits [14] [15].

Alternatively, this idea was taken up in designing quadratic converters made of a single power switch and three diodes with D_{SI} synchronized to S switches (figure 3) [16] [17] [18].

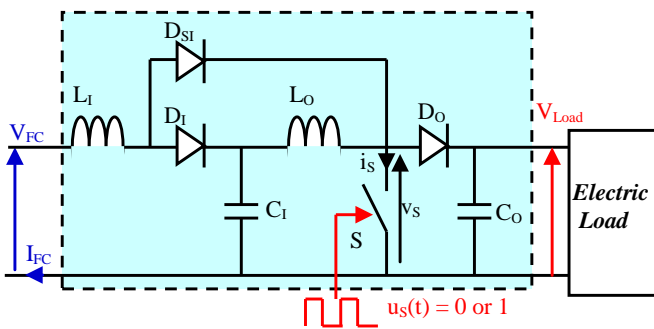


Figure 3. quadratic boost DC-DC converter

Consequently, its duty-cycle $(d)_{quadra}$ is:

$$(d)_{quadra} = 1 - \sqrt{\frac{V_{FC}}{V_{Load}}} \quad (5)$$

which signifies a moderate duty cycle $(d)_{boost} = 0.684$ leading to a much better transient tracking behaviour. But, the switch coefficient $(F_S)_{quadra}$ is in this case:

$$(F_S)_{quadra} = \frac{V_{Load}}{V_{FC}} \left(1 + \sqrt{\frac{V_{FC}}{V_{Load}}} \right) \quad (6)$$

As a result, $(F_S)_{quadra} = 13.2$ is even higher than $(F_S)_{boost} = 10$ which makes this solution out of purpose.

2.3 DC-DC converter with transformer

In order to solve the problem of DC-DC converters with extreme step-up voltage conversion ratio, this sub-section now consider the advantages and disadvantages of using a transformer. With respects to magnetic coupling, two kinds of topologies can be taken into consideration [19]. In the forward topology (figure 4), the transformer allows direct power transfer. The flyback topology uses the transformer as two coupled inductors (figure 5). In both case, the transformer purpose is to decouple electric constraints linked to the source (low voltage / high current) from those linked to the load (high voltage / low current). It allows using suitable power switches in primary and secondary sides.

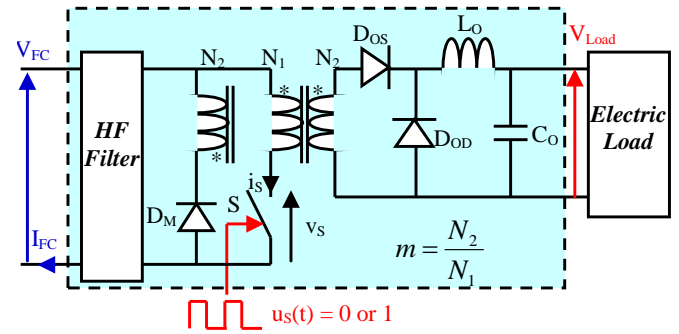


Figure 4. forward DC-DC converter

So as to avoid magnetic saturation, the forward structure duty cycle must not exceed 0.5 [20]. Assuming $m = N_2 / N_1$, the duty cycle $(d)_{for}$ and the switch coefficient $(F_S)_{for}$ can be figured out as follows:

$$(d)_{for} = \frac{V_{FC}}{m V_{Load}} \leq 0.5 \quad (7)$$

$$(F_S)_{for} = \frac{(2V_{FC})(mI_{Load})}{V_{Load} I_{Load}} = \frac{2mV_{FC}}{V_{Load}} \quad (8)$$

The smaller the m transformer ratio is, the smaller the switch coefficient is. As the forward duty cycle is bounded to 0.5, the m coefficient can not go below $m = 2V_{Load} / V_{FC}$. And so this forward topology reveals a much enhanced switch coefficient than the conventional boost one : $(F_S)_{for} > 4$.

Even so, this topology has a transformer with a very large step-up ratio. It ranges $m = 20$ in our specifications case. As a matter of fact, the secondary part of this topology is a buck converter. Consequently, as this latter part behaves as a step-down converter, the transformer needs to be an extreme step-up voltage converter. As a result of this high ratio, the transformer implemented in the forward topology entails an important parasitic capacitance. Utilizing a transformer with such a flaw generates voltage and current spikes and increases

dramatically power loss and noise. This drawback makes this solution unfeasible.

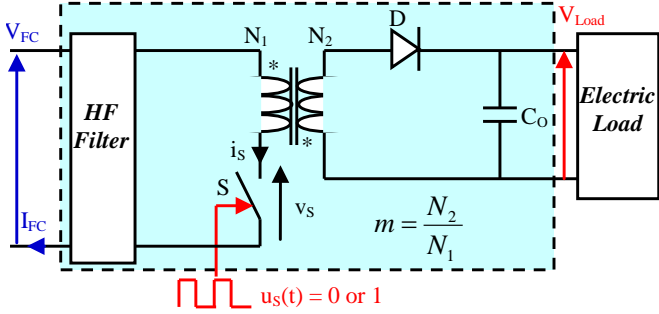


Figure 5. Flyback DC-DC converter

The flyback structure features a basic switching cell (S & D) and its duty cycle (d_{fly}) can range from 0 to 1 [21]. Assuming $m = N_2 / N_1$, the duty cycle (d_{fly}) and the switch coefficient (F_S) $_{fly}$ can be expressed as:

$$(d)_{fly} = \frac{V_{Load}}{V_{Load} + mV_{FC}} \quad (9)$$

$$(F_S)_{fly} = \frac{(V_{FC} + mV_{Load})(I_S)}{(V_{FC})(d_{fly}I_S)} = \frac{1}{(1 - d_{fly})(d_{fly})} \quad (10)$$

As a result, (F_S) $_{fly}$ is minimized for a 0.5 duty cycle. In this optimal design case, the switch coefficient (F_S) $_{fly}$ gets down to 4 and the transformer ratio m is only 10. Despite that, the flyback transformer requires an air gap in its core material causing leakage inductance between the coupled winding. With this implementation, the flyback topology switches suffer from voltage spikes which reduce the structure efficiency.

Thus, the flyback topology requires a non-dissipative ancillary system able to recover the energy stored in the leakage magnetic field. To achieve this function, one takes advantage of the fact no isolation is demanded. Consequently, we suggest the new scheme depicted in figure 6. It is a variation of the high step-up clamp-mode converter proposed by [22].

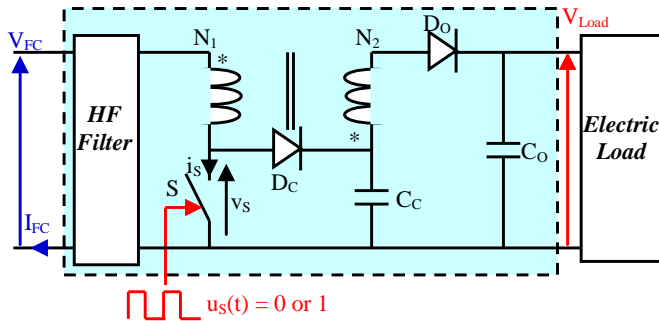


Figure 6. Flyback DC-DC converter with non-dissipative active clamp with galvanic isolation

3 A detailed study of the selected DC-DC converter

In the former section, several topologies have been analysed with respect to the set of requirements of a voltage regulator dedicated to a fuel cell electric generator. Among the DC-DC converter candidates, one design has been down-selected. In this paragraph a modelling of this specific scheme is performed to determine how well the candidate satisfies requirements. Moreover modelling helps the designer to perform an excellent final prototype.

In this study, we only consider the non ideal magnetic coupling of the transformer winding. Hence, the two-winding transformer equations are modelled with topologically equivalent structure including an ideal transformer, a magnetizing inductance referred to primary (called L_m) and a small serial leakage inductance located at the primary side (called L_l) [13]. Figure 7 illustrates the electrical equivalent circuit model used in the following converter steady state analysis. In a modelling iteration (for accurate switches analysis), the parasitic capacitance will be taken into account in the next section.

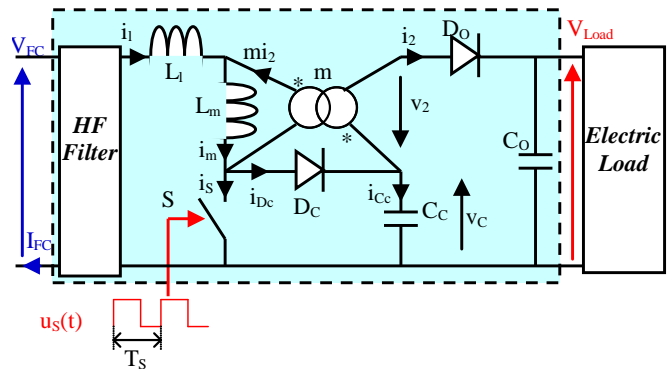


Figure 7. Selected DC-DC converter along a switching period

3.1 Steady state successive stages

The steady state behaviour analysis shows that the converter features four different topologies along switching period T_s . Figure 8 depicts the main electrical waveforms: secondary voltage $v_2(t)$, C_C capacitance current $i_{C_C}(t)$ and the primary and secondary currents $i_1(t)$, $i_2(t)$.

During the first stage, the power switch current $i_s(t)$ rises while the secondary diode current $i_2(t)$ decreases. For a tiny leakage inductance value, the current slope is roughly limited to 500 A/ μ s rate with respect to MOSFET technology. But whatever the transformer we further experiment, the rising slope is actually limited by the leakage inductance. As a consequence, the power device S switches on softly with almost no losses due to negligible switch voltage. Meanwhile, the secondary voltage $v_2(t)$ is equal to $(v_C - V_{load})$. The length

of stage 1 is linked to the transformer leakage inductance by the following expression:

$$d_1 T_s = \frac{L_l I_m}{V_{FC} + \frac{V_{Load} - v_C}{m}} \quad (11)$$

Subsequently, to experiment high switching frequency, L_l value has to remain small in comparison with L_m value.

During the second stage, the FC transfers its power to the transformer and the secondary voltage is now equal to mV_{FC} ($L_l \ll L_m$). The length of stage 2 is monitored by the close loop dedicated to the converter voltage control. So it lasts $(d - d_1)T_s$.

At the end of the second stage, the power device S switches off. At the very beginning of the third stage, its voltage increases promptly as a result of its parasitic capacitance loading. It brings about the on-state of both diodes D_O and D_C . Hence, the power device voltage v_S is clamped to v_C during the stage 3. Therefore, the switch-off losses are shortened all the more since V_C tends to $(V_{FC} + (V_{load} - V_C)/m)$. Next paragraph will give the expression of V_C and next section will show its experimental measurement. The voltage clamping also allows choosing a power device S with smaller rated voltage. This point is mostly significant for MOSFET topology because the conduction resistance R_{DSON} decreases as far as the rated voltage increases. R_{DSON} is indeed more or less proportional to $V^{2/3}$ [23] [24]. On top of switching losses reduction, the switch S benefits from conduction losses decrease. During the third step, leakage inductance transfers its energy to the clamp capacitor. The capacitance value of this latter is high in order to obtain small v_C voltage ripple and hence low switch voltage constraint. That is the reason why the clamp phase, which involves a resonant circuit (L_l and C_C), shows a quite linear behaviour. Consequently the length of stage 3 is linked to the transformer leakage inductance as follows:

$$d_3 T_s = \frac{L_l I_m}{V_C - \left(V_{FC} + \frac{V_{Load} - v_C}{m} \right)} \quad (12)$$

During the fourth and last stage, the energy stored in the transformer as well as the energy stored in the capacitance C_C are restored to the electric load. The secondary voltage is equal to $(v_C - V_{load})$.

3.2 Steady state key values

The selected DC-DC converter has two designing degrees of freedom: its rated duty cycle and the transformer voltage ratio. In order to optimize this choice, key values have to be computed. The previous section explained the converter operation and figure 8 illustrates the significant waveforms in steady state. In this condition, one can state:

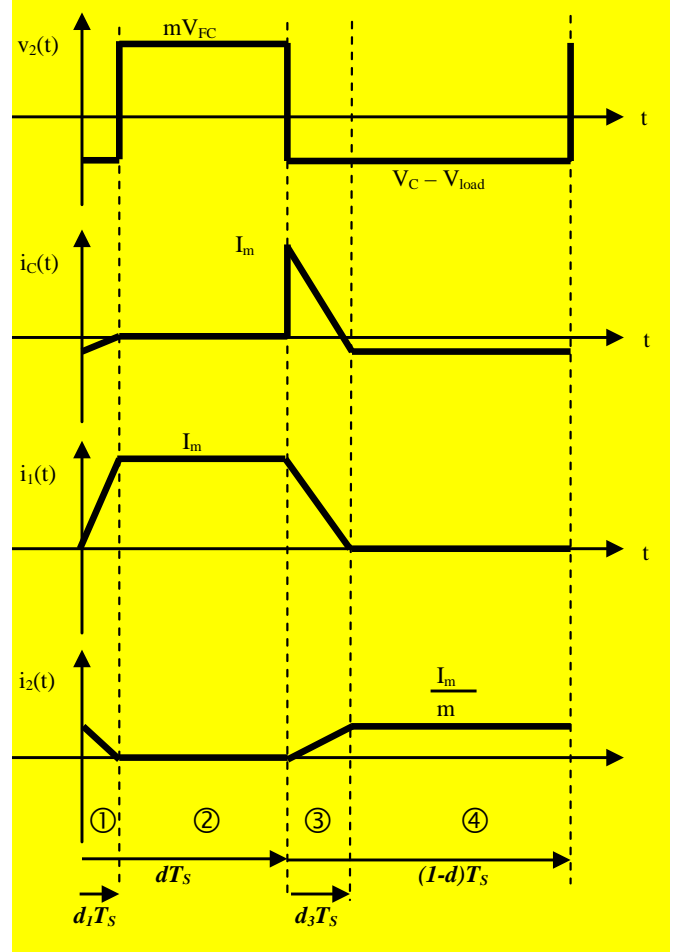


Figure 8. Main waveforms of the DC-DC converter along a switching period

♦ that the transformer average voltage equals zero. According to figure 8, the secondary average voltage is computed as follows:

$$\langle v_2 \rangle = (d - d_1) m V_{FC} - (1 - d - d_1) (V_{Load} - v_C) \quad (13)$$

♦ that the capacitance average current equals zero. This value is calculated using the previous description:

$$\langle i_C \rangle = I_m \left(\frac{d_3}{2} \right) - \frac{I_m}{m} \left(1 - d - \frac{d_3}{2} + \frac{d_1}{2} \right) \quad (14)$$

♦ and that the output power equals the input power. For this purpose, we consider that the input and output filters deliver a constant voltage. Hence, this power balancing depends only on the average values of $i_1(t)$ and $i_2(t)$:

$$V_{FC} I_m \left(d + \frac{d_3}{2} \right) = V_{Load} \frac{I_m}{m} \left(1 - d - \frac{d_3}{2} + \frac{d_1}{2} \right) \quad (15)$$

Assuming that the d_1 is negligible with respect to the three other stages lengths, one finally gets:

$$\frac{V_{Load}}{V_{FC}} = \frac{1+dm}{1-d} \quad (16)$$

$$\frac{V_C}{V_{FC}} = \frac{1}{1-d} \quad (17)$$

$$d_3 = 2 \frac{1-d}{1+m} \quad (18)$$

As a result the switch coefficient (F_s) can be evaluated as follows:

$$(F_s) = \frac{1}{(1-d)(d)} \quad (19)$$

Thus the optimal duty cycle is $d = \frac{1}{2}$ which leads to the best possible switch coefficient $(F_s) = 4$ associated to the transformer voltage ratio $m = 8$ and the theoretical switch maximal value $V_I = 2V_{FC}$.

The above model was simulated in matlab-simulink environment using its dedicated SimPowerSystem application library. This software is convenient to design a converter from the topological point of view to the control design concern. As a matter of fact, the next step of this present work is to elaborate a simple and efficient control algorithm to regulate the output voltage and prevent over-currents. Table 1 lists the main simulation parameters. The solver is based on an Euler method using fixed-step set to 1 ns. Figure 8 depicts most important electric variables: the three currents $i_1(t)$, $i_2(t)$ and $i_{Dc}(t)$ are drawn on the first subplot; the two switch variables $i_s(t)$ and $v_s(t)$ are plotted on the second graph. It can be noticed that the above assumption ($d_1 \ll 1$) is confirmed. Moreover, the maximal switch voltage occurs indeed during the stage 3 and hardly reaches 60 V which is rather closed to the theoretical 50 V and very small compared to the 250 V load voltage. The difference between both values is due to the finite clamp capacitance value C_C leading to a $V_I(t)$ voltage swing.

Table 1: simulation parameters

V_{FC}	25 V	L_m	44 μ H
V_{Load}	250 V	L_l	1 μ H
P	100 W	m	8
F_s	100 kHz	C_C	1 μ F

4 Implementation and experimental results of the selected DC-DC converter

The previous section brought out the theoretical importance of the selected structure. It also exposed its optimized main parameters. The current section presents its implementation and associated experimental results.

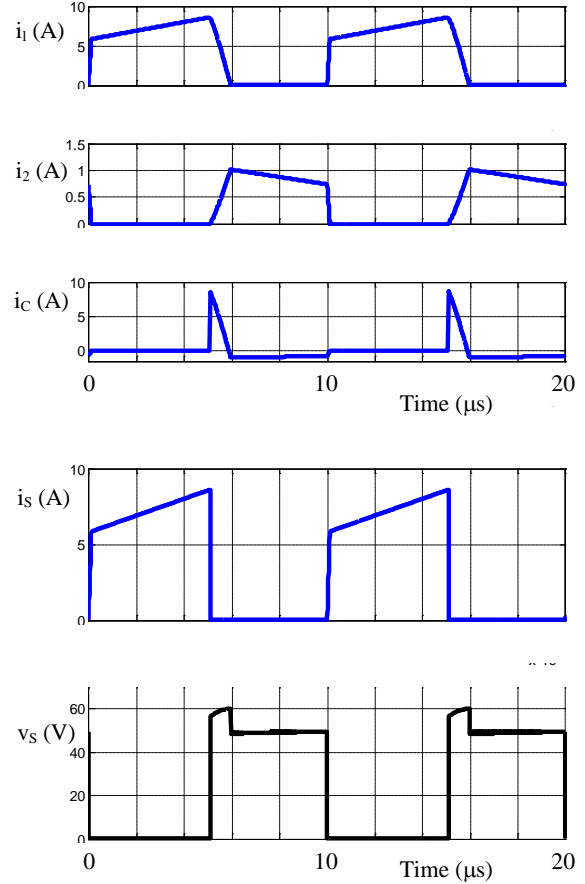


Figure 9. Main variables of the selected converter simulation

4.1 Selected converter implementation

A 100 W / 100 kHz prototype was built using components with characteristic similar to table 1. The transformer was constructed with an ETD39 core made of 3C90 material. The input, output and clamp capacitors (C_I , C_C , C_O) are ceramic capacitors ($C_I = 22 \mu\text{F} / 50 \text{ V}$, $C_C = 4.7 \mu\text{F} / 100 \text{ V}$, $C_O = 0.47 \mu\text{F} / 630 \text{ V}$). The input capacitor is reinforced with an electrolytic capacitor (6800 $\mu\text{F} / 63 \text{ V}$). The switch S is a MOSFET transistor IRFS4610PbF (100 V, 73 A, $R_{DSON} = 14 \text{ m}\Omega$), the output diode D_O is a SDD04S60 (600 V, 4 A, schottky technology) and the clamp diode D_C is a 12WQ10FNPbF (100 V, 12 A, schottky technology). In order to avoid additional voltage stress to the switches and EMI problems, it is essential to design a switching cell length as small as possible (figure 10). Actually the switch off overvoltage spike is due to the product of the switch current slope and the inductance value of the switching cell [25].

$$\Delta V_{MOSFET} = -L_{cell} \left(\frac{di}{dt} \right)_{MOSFET} \quad (20)$$

As it is important to lower the MOSFET voltage constraint, the spike maximum value has to be less than ten percent of its theoretical maximum value, which in our case means no more than 5 to 6 V. With respect to (- 500 A/ μ s) current MOSFET

slope, this leads to realize a switching cell with a self inductance lower than: 10 to 12 nH. Characterizing precisely the connections and the PC board is quite complicated and can be successfully investigated with Partial Element Equivalent Circuit Method [26-27]. However in our case, the switching cell can be approximated by a square PC board (figure 11), with depth $b = 35 \mu\text{m}$ small compared to the other size: the trace D and the trace width $2w = 5 \text{ mm}$. In that condition, the self inductance of the loop can be approximated by the following expression [28]:

$$L = \frac{2\mu_0}{\pi} \left[w\sqrt{2} + (D-w)\sinh^{-1}\left(\frac{D-w}{w}\right) \right] - \frac{2\mu_0}{\pi} \left[w\sinh^{-1}(1) + \sqrt{(D-w)^2 + w^2} \right] \quad (21)$$

This leads to a square side smaller than $D_{\text{MAX}} = 13 \text{ mm}$ (figure 12).

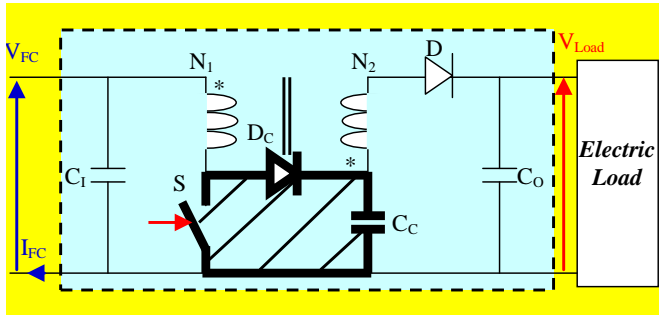


Figure 10. The switching cell of the selected DC-DC converter

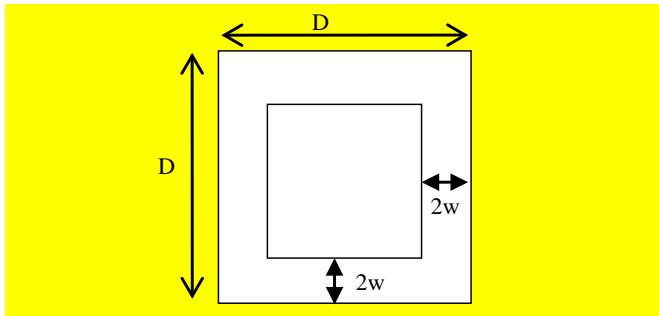


Figure 11. Square coil with rectangular cross section

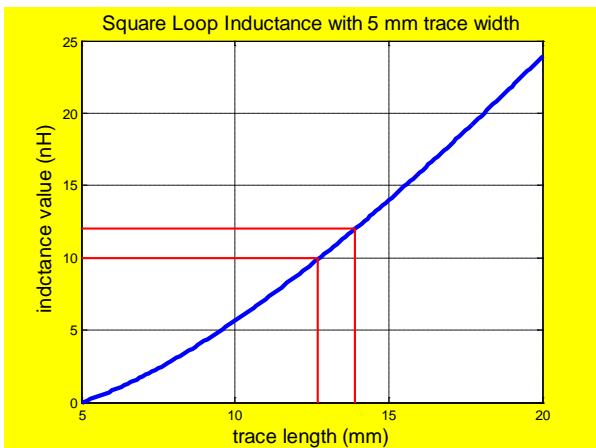


Figure 12. Square coil inductance

4.2 Prototype tests

Figure 13 illustrates prototype behaviour at rated power. Input current $I_i(t)$ and switch voltage $V_s(t)$ are plotted on the same time graph. In general, these waveforms fit well the simulation ones. In particular, no overvoltage occurs when S switches off, confirming that the switching cell is well designed.

However parasitic ringing affects input current $I_i(t)$ during phase 2. Moreover, when phase 3 starts, the input current value $I_i(dT_s^+)$ is smaller than expected. The previous model cannot anticipate these two ringing phenomena. In an attempt to better fit the transformer behaviour, we must indeed take its parasitic capacitor C_{PO} into account (figure 14). In figure 14, R_{PO} represents the ringing damping effect due to value magnetic core loss and wiring conduction loss. This new scheme allows predicting the detailed prototype behaviour. Impedance-meter analysis was conducted with a 4192A (5 Hz – 13 MHz) impedance analyser HP device. It confirms a magnetizing inductance L_m and leakage inductance L_l close to $44 \mu\text{H}$ and a $1 \mu\text{H}$ respectively. It also gives C_{PO} about a hundred pF value. It also validates the ringing frequency of 2 MHz. R_{PO} resistance value is set to $10 \text{ k}\Omega$ after a fitting process while comparing experimental results and simulation ones. Figure 14 illustrates a rated power simulation with the following parameters values: $C_{PO} = 100 \text{ pF}$ and $R_{PO} = 10 \text{ k}\Omega$.

In brief, phase 3 is divided in two phases: phase 3-1 and phase 3-2. During phase 3-1, output diode D_o does not yet conduct and for that reason the parasitic capacitor voltage can evolve freely. As $L_m \gg L_l$, one can assume that L_m behaves as a current source I_m . Similarly, $C_c \gg C_{PO}$ implies C_c can be considered as a voltage source V_c . Consequently, a resonant circuit takes place with L_l in the primary side and C_{PO} in the secondary side. Phase 3-1 ends when diode D_o switches on. At that specific time, the current drop ΔI_l can be computed as:

$$\Delta I_l = m \sqrt{\frac{C_{PO} V_c}{L_l}} \quad (22)$$

This means that a part of the energy stored in the leakage inductor is not transferred to the non-dissipative clamp system but to the parasitic capacitor C_{PO} . This energy is lost during the phase 2 when the same resonant circuit oscillates during several periods: energy dissipation occurs in windings and core material.

As a conclusion, these two parasitic ringing phenomena have a detrimental effect on the converter efficiency. According to equation (22), the smaller C_{PO} value is, the more efficient the clamping system is. Hence the transformer design has to reduce the parasitic capacitance value. That is the reason why the primary and secondary inductors are wound with a winding spacer (figure 16).

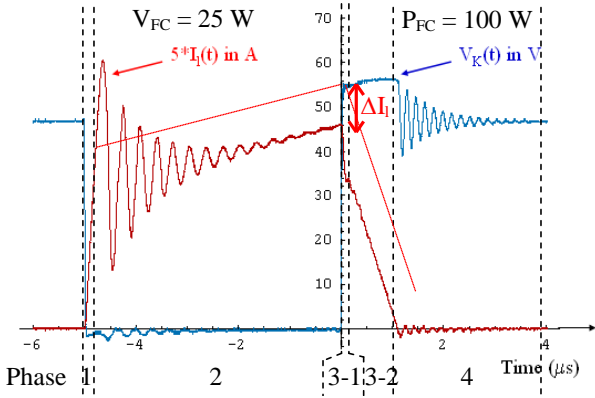


Figure 13. Experimental waveforms of the prototype

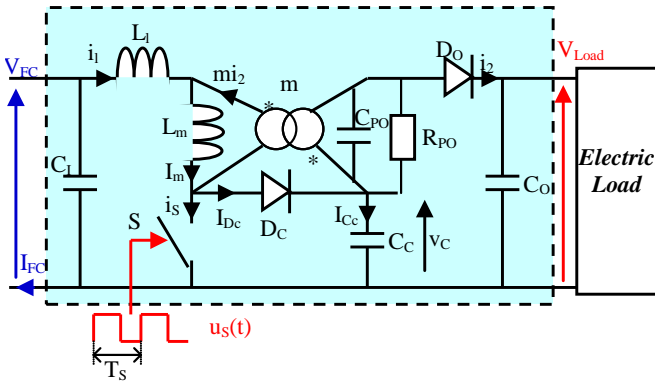


Figure 14. Detailed model of the selected converter

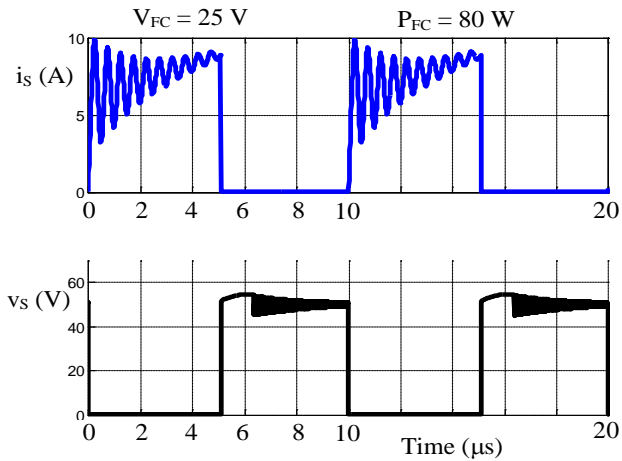


Figure 15. Simulated waveforms of complete model

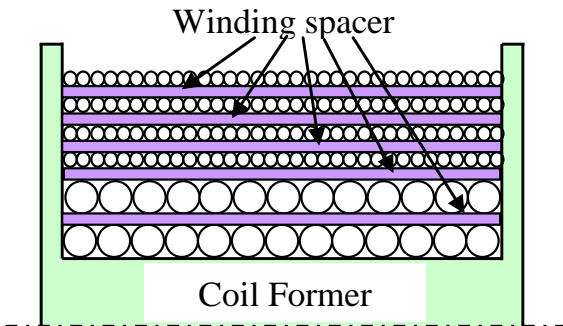


Figure 16. The transformer winding building

5 Experimental comparison of the selected topology and the classic boost converter

The analysis of the selected DC converter experimental waveforms contributed to optimize the transformer design which is one of the key components. In this section, the selected DC converter is compared with the conventional boost converter. For that purpose, two 100 W / 100 kHz prototypes were built, using CMS components, ceramic capacitors and the same core material ETD39 / 3C90 for the transformer and inductor. Table 2 summarizes the main features of each prototype. Figure 17 shows key waveforms of them. Power losses were analysed in detail. The selected DC converter efficiency is far greater than the classic boost one. (Table 3). At rated power, conventional boost has twice more losses than the selected converter. As shown on figure 17, the switch blocking voltage of the selected converter never exceeds 60 V which allows choosing a MOSFET with low rated voltage and hence low on-state resistance $R_{DS(on)}$. On the contrary, boost converter switch suffers from high voltage (250 V) and thus has large conduction loss. On figure 17, $i_1(t)$ waveform also confirms that the selected structure avoids the transistor switch-on losses. The active switch has small switch-off losses because its voltage is clamped to a moderate voltage ($V_c \cong 50$ V). Quite the opposite, the transistor of the boost converter faces important switch losses because of hard switching and large voltage stresses. In addition, a general picture of selected converter validates the four depicted phases and corroborates equation (18). This equation proves that phase 3 length is constant and much smaller than switch off-state length $(1-d)T_s$. Consequently, phase 4 always exists and assures the soft switching of phase 1. Components datasheets enable to calculate switch losses, and temperature sensors permit to measure the heat sink temperature to validate these evaluations. As a matter of fact, active switch losses of selected structure are eight times smaller than boost MOSFET losses. It points out that the selected converter has an efficient topology with respect to switch stresses. This fact is also confirmed when measuring switch cases temperatures. On the other hand, the transformer magnetic core has two to three times more losses than the inductor magnetic core. The ringing phenomena described in section 4 explain this result. But nevertheless, this drawback does not offset the other advantages of the selected structure.

Table 2: prototypes parameters

Boost parameters:

C_1	6800 μ F / 63 V and 22 μ F / 50 V
C_o	0.47 μ F / 630 V
L	150 μ H, ETD39 / 3C90
S	IXFV50N30PS (300 V/52 A/66 m Ω) MOSFET
D	SDD04S60 (600 V, 5.6 A, schottky technology)

Selected converter parameters:

C_1	6800 μ F / 63 V and 22 μ F / 50 V
C_o	0.47 μ F / 630 V
C_c	4.7 μ F / 100 V
Transf.	$L_m = 44$ μ H, $m = 8$, ETD39 / 3C90
S	IRFS4610PbF (100 V, 73 A, $R_{DS(on)} = 14$ m Ω)
D	SDD04S60 (600 V, 5.6 A, schottky technology)

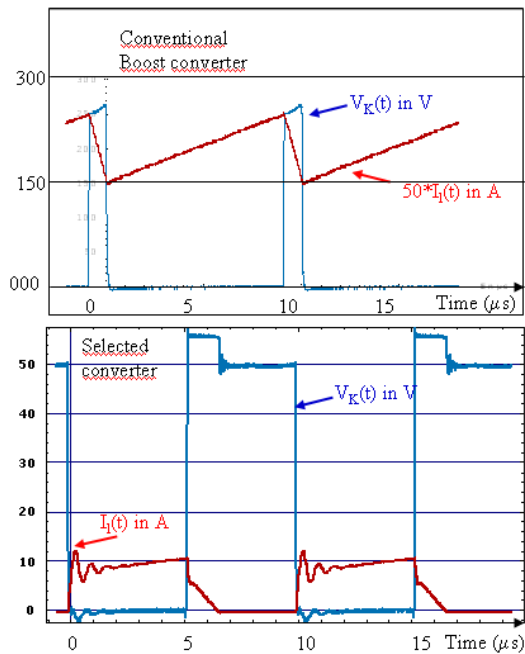


Figure 16. Prototypes key waveforms

Table 3: efficiencies comparison

	P = 68 W	P = 100 W
Boost converter	$\eta = 93.5 \%$	$\eta = 91.5 \%$
Selected converter	$\eta = 97.5 \%$	$\eta = 96.0 \%$

6 Conclusion

This paper focuses on the voltage regulator as a key supporting equipment of a fuel cell electric power supply. As a matter of fact, this device faces severe specifications. The present investigations are limited to small power systems (from a few watts to 1 kW) and allow exhibiting an attractive topology. It is made of a single active switch and coupled inductors. This latter component adds a design degree of freedom. It allows reducing the switch voltage stresses. Consequently, the MOSFET technology fits much better the switch requirements than in other studied topologies. Moreover, the transformer has obviously leakage inductance. In this topology, the magnetic leakage does not induce further voltage spikes but permit the active switch to have soft commutations. Last but not least, this structure is simple and can be easily controlled.

The paper also takes care of designing rules. Experimental prototypes were built to validate the theoretical behaviour. Experimental results proved that the proposed converter is indeed far more efficient than a conventional boost converter.

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