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# A High Efficiency Differential 60 GHz VCO in a 65 nm CMOS Technology for WSN Applications

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and Robert Plana, *Senior Member, IEEE*

**Abstract**—This paper presents a differential voltage controlled oscillator (VCO) implemented in a 65 nm bulk CMOS technology for the unlicensed 60 GHz band. It achieves a record efficiency of 4.9% by generating a maximum differential output power of -0.9 dBm while drawing 16.5 mA from a 1 V supply (including buffers). This VCO is thus perfectly suited for the use in a fully integrated 60 GHz transceiver for battery-powered wireless sensor networks (WSN). The minimum measured phase noise is -90.3 dBc/Hz at 1 MHz offset and -112 dBc/Hz at 10 MHz offset, the measured tuning range reaches from 57.6 GHz to 60.8 GHz.

**Index Terms**—millimeter-wave, 60 GHz, VCO, varactor

## I. INTRODUCTION

Current research topic is the design of low-power radio frequency transceiver front-ends for the unlicensed frequency band around 60 GHz in nanoscale CMOS technologies. Reducing power consumption of the key building blocks hereby is a major issue. When it comes to the design of oscillators, output power is equally important, because mixer performance increases with local oscillator power. Furthermore, the output of an integrated VCO supplies several circuit blocks. When sacrificing VCO output power to reduce its power dissipation, additional, power-hungry circuit blocks become necessary. Thus, in order to minimize transceiver power consumption, the VCO's *efficiency* has to improve.

CMOS VCOs operating around 60 GHz regularly exhibit quite low output power and efficiency (see table I). Even powerful designs like [1] with  $P_{\text{out}} = -6.6$  dBm stay well behind their SiGe counterparts. These VCOs (e.g. [1], [2], [3]) commonly employ cross-coupled architectures (cf. Fig. 1a), or, though less frequently, the differential common-drain Colpitts topology shown in Fig. 1b [4].

This paper proposes the use of an alternative architecture [5], given in Fig. 2, which is to the best of the authors' knowledge not yet employed in the 60 GHz band. Its implementation in 65 nm CMOS shows a record efficiency of 4.9%.

## II. OSCILLATOR CIRCUIT DESIGN

The schematic of the proposed VCO is given in Fig. 2. The chosen architecture can either be considered as the extension

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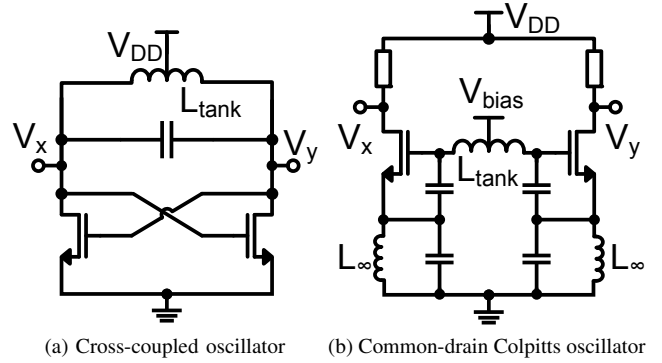


Fig. 1. Commonly used architectures for 60 GHz VCOs

of a cross-coupled oscillator by capacitive voltage dividers. Alternatively, and more consistent with earlier implementations at lower frequencies (e.g. [5]), it can be seen as a differential Colpitts oscillator (whose decisive feature is the feedback using capacitive voltage dividers). The transistors are used in a common source configuration, which, in contrast to the common drain configuration shown in Fig. 1b, inverts the signal. Hence, the output signal is fed back from the other half of the differential circuit, where the drain voltage is available at inverted polarity due to odd-mode operation.

The key differences between the proposed Colpitts VCO and a cross coupled VCO are illustrated in Fig. 3: 3a shows that the cross-coupled VCO's gate voltage is just an inverted version of its drain voltage, implying that gate bias voltage

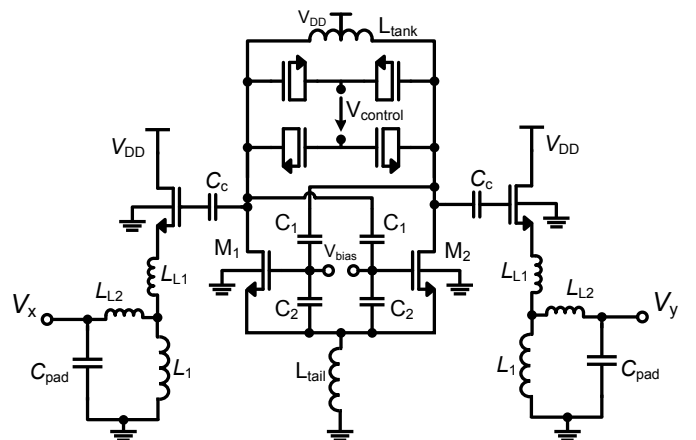


Fig. 2. Proposed differential common-source Colpitts VCO (without bias circuitry), achieving high efficiency at 60 GHz

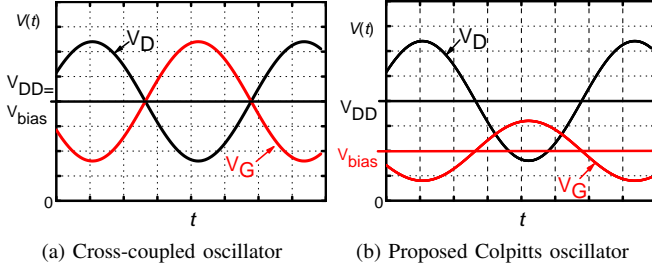


Fig. 3. Illustration of oscillators' gate and drain voltage

and supply voltage are identical. In the case of a large voltage swing, the gate voltage deviates considerably from its initial (already non-ideal) bias point. As a consequence, the transistor is providing less transconductance than possible, eventually even entering the triode region. This limits the drain voltage swing at which a cross-coupled VCO can provide sufficient negative resistance to further increase oscillation amplitude.

In the case of the proposed Colpitts VCO, the capacitive connection between gate and drain allows to independently choose the gate bias voltage as illustrated in Fig. 3b. Hence, a drain current density of around  $0.3 \text{ mA}/\mu\text{m}$  which maximizes the transistor's linearity [6] can be set. The gate voltage swing observed in Fig. 3b is  $\frac{C_1}{C_1+C_2}$  times the drain voltage swing (in the present implementation  $\frac{C_1}{C_1+C_2} \approx 0.5$ ). Thus, the transistor's gate voltage stays close to the initial bias point. The absolute capacitance values of  $C_1$  to  $C_2$  are chosen to achieve, together with parasitics, tank inductor and varactors, a resonance frequency of 60 GHz.

Compared to the cross-coupled case, a Colpitts VCO requires wider transistors: this is because the capacitive voltage division also reduces the negative resistance that is added to the tank per micron of transistor width. The transistors used in the proposed VCO are (minimum channel length) general purpose (GP) devices composed of 14 fingers with  $1 \mu\text{m}$  width. However, as the drain current density of the transistors is much lower than in the cross coupled case, power consumption does not increase. Yet, the higher linearity provided by these larger transistors can be exploited to achieve a higher output power, and thus increase efficiency.

In order to further maximize voltage headroom and minimize phase noise, the usual tail current source is replaced by a tail inductor  $L_{\text{tail}}$ . Its size is chosen to resonate with the transistor's parasitic source-bulk capacitances in order to filter the second harmonic of the oscillation frequency [7].

In comparison to the common-drain Colpitts VCO of Fig. 1b, the proposed common-source VCO has the advantage of a potentially higher tank voltage swing and thus linearity. This is due to the fact that it connects the tank to the transistor's drain rather than to its gate and source. The disadvantage of the proposed solution with respect to the common drain VCO is that the oscillator's output and the tank share the same terminals: the attached load has thus an influence on the tank impedance.

To minimize this loading of the VCO core and to allow the driving of a differential  $100 \Omega$  output, common drain buffers are used [1]. Their single-ended outputs are matched to  $50 \Omega$

by the inductors  $L_1$  and  $L_2$  of value  $200 \text{ pH}$ . The matching takes into account the simulated parasitic pad capacitance  $C_{\text{pad}}$  (around  $25 \text{ fF}$ ) and the parasitic interconnect inductances  $L_L$  (each around  $10 \text{ pH}$ ). The buffer transistors are  $65 \text{ nm}$  GP devices with  $14 \times 1 \mu\text{m}$  channel width.

#### A. Tank Inductor

As the tank inductor  $L_{\text{tank}}$  is connected with both ends to the resonator, its differential performance is more important than its single ended behavior. This has consequences on the optimization of the spiral dimensions in order to obtain a high Q-factor at the specified resonance frequency 60 GHz: slightly larger metal widths than in the case of single ended excitation, as well as shunting of the two topmost thick metal layers is advantageous in this case.

To limit power consumption,  $L_{\text{tank}}$  is chosen to be  $155 \text{ pH}$ , i.e. considerably larger than the minimum value possible (which would minimize phase noise [4]). The tank inductor's differential Q-factor is 19.1 at 60 GHz, while the single-ended Q peaks at that frequency with a value of 14.5 [8].

#### B. Accumulation MOS Varactors

Four accumulation MOS (AMOS) varactors are used to change oscillation frequency. Each of them has a capacitance ranging from  $8.4 \text{ fF}$  to  $12.7 \text{ fF}$ . They are differentially tuned in order to reduce phase noise. The full-custom AMOS varactors are realized by placing an n-channel MOSFET into an n-well. A multi-finger layout is used. The finger width is  $0.78 \mu\text{m}$ , while relying on GP devices with minimum channel length. The measured capacitance variation and Q-factor of the designed varactors are shown in Fig. 4. These values show that the varactors limit the resonator's Q-factor.

### III. MEASUREMENT RESULTS

The fabricated VCO is shown in Fig. 5. Its size of  $0.21 \text{ mm}^2$  is pad-limited. The VCO was characterized on-wafer, using a R&S FSU 67 GHz spectrum analyzer (SA) for frequency, power and phase noise measurements. The SA was connected to one of the VCO's outputs, while the other one was terminated by a  $50 \Omega$  load. Corrections for cable loss and single-ended measurement (in total around  $9 \text{ dB}$ ) are applied.

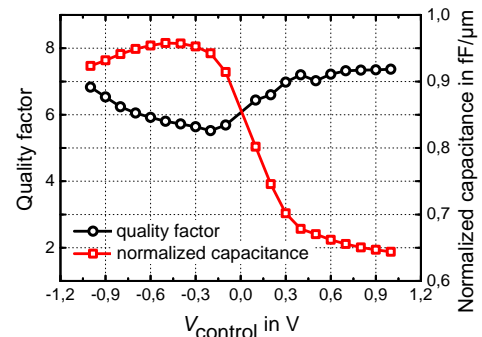


Fig. 4. Quality factor and normalized capacitance versus control voltage measured on a varactor with  $51 \times 0.78 \mu\text{m}$

TABLE I  
PERFORMANCE COMPARISON TO 65 NM AND 90 NM VCOS FOUND IN LITERATURE

Reference	Techn.	$f_0$ [GHz]	Phase Noise [dBc/Hz]	FTR [%]	$P_{DC}$ [mW]	$P_{RF}$ [dBm]	$\frac{P_{RF}}{P_{DC}}$ [%]	FoM = $-10\log_{10} \left[ \left( \frac{f_0}{\Delta f} \frac{FTR}{10\%} \right)^2 \frac{P_{RF}}{P_{DC}} \frac{1}{L[\Delta f]} \right]$ [dB/Hz]
Ellinger, 2004 [1]	90 nm SOI	56	-92 @ 1MHz	14.7	21	-6.6	<b>1.0</b>	-170.3
Kim, 2007 [2]	65 nm SOI	70.2	-106.1 @ 10MHz	9.55	10.1	-35	<b>0.003</b>	-137.4
Jimenez, 2009 [3]	65 nm bulk	56	-99.4 @ 1MHz	17	24.6	-9.3	<b>0.47</b>	-175.7
Tang, 2006 [4]	90 nm bulk	77	-100.3 @ 1 MHz	8.1	37.5	-13.8	<b>0.11</b>	-166.6
this work	65 nm bulk	59	-90.3 @ 1 MHz	5.4	16.5	-0.9	<b>4.9</b>	-167.3

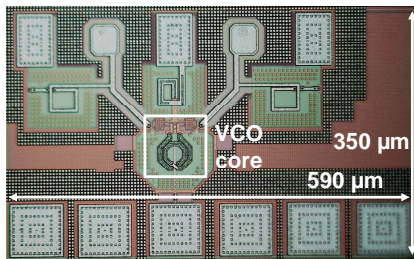


Fig. 5. Die photo (size pad-limited)

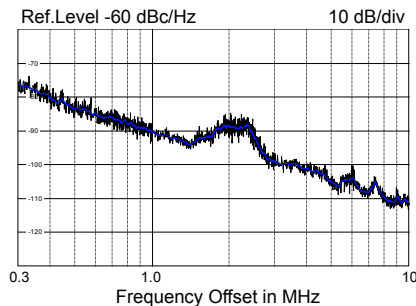


Fig. 6. Phase noise at  $f_0=60.77$  GHz

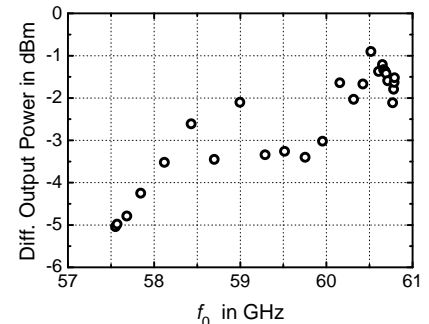


Fig. 7. Measured output power

The VCO starts oscillating at  $I_D \approx 5$  mA. This current is equally split between core and buffers. At the maximum linearity bias point the complete circuit draws 16.5 mA from a 1 V supply, which is the maximum voltage allowed to ensure transistor reliability. The VCO is tuned by a differential voltage  $V_{control}$ , applied by two voltage sources with  $V_{DD} \pm V_{control}/2$ .

The oscillation frequency  $f_0$  reaches from 57.58 GHz to 60.80 GHz, which corresponds to a frequency tuning range (FTR) of 5.4%. This quite small tunability comes from the fact that the tuning range of the full-custom varactors, which could not be characterized before VCO design, is smaller than expected. The VCO's phase noise is decreasing when increasing the frequency of oscillation. Fig. 6 shows the phase noise at 60.77 GHz, where a minimum of -90.3 dBc/Hz at 1 MHz offset is achieved. Phase noise lies around -86 dBc/Hz@1 MHz over the FTR, with a maximum of -83 dBc/Hz@1 MHz at 57.6 GHz.

The major virtue of the presented VCO is its high output power. As illustrated in Fig. 7,  $P_{RF}$  is increasing with increasing frequency. The maximum achieved value is -0.9 dBm.

Table I shows the performance of the VCO in comparison to nanoscale CMOS VCOS found in literature. The ratio between output power  $P_{RF}$  and power dissipation  $P_{DC}$  shows how efficiently the VCO generates RF power. The presented VCO shows record performance with respect to this metric. Additionally, a FoM demonstrates that even when taking into account the other characteristics, the presented VCO exhibits state-of-the-art performance.

#### IV. CONCLUSION

This paper demonstrates the benefits of employing a differential common-source Colpitts architecture for oscillators

operating in the 60 GHz band. A VCO using this topology, fabricated in a 65 nm CMOS technology, achieves an output power of up to  $P_{RF} = -0.9$  dBm at  $V_{DD} = 1.0$  V, while consuming only 16.5 mW of DC power. The achieved efficiency of up to 4.9% is, to the best of the authors' knowledge, the highest found in literature for 60 GHz CMOS VCOS.

#### V. ACKNOWLEDGEMENTS

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