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► **To cite this version:**

Hung Q. Nguyen, Laetitia Pascal, Z. H. Peng, Olivier Buisson, B. Gilles, et al.. Etching suspended superconducting hybrid junctions from a multilayer. 2011. hal-00641292v1

**HAL Id: hal-00641292**

**<https://hal.science/hal-00641292v1>**

Preprint submitted on 15 Nov 2011 (v1), last revised 22 Jun 2012 (v2)

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# Etching suspended superconducting hybrid junctions from a multilayer

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A novel method to fabricate large-area superconducting hybrid tunnel junctions with a suspended central normal metal part is presented. The samples are fabricated by combining photo-lithography and chemical etch of a superconductor - insulator - normal metal multilayer. The process involves few fabrication steps, is reliable and produces extremely high-quality tunnel junctions. Under an appropriate voltage bias, a significant electronic cooling is demonstrated.

PACS numbers:

Tunnel junctions between a superconductor (S) and a normal metal (N) separated by an insulating oxide barrier (I) are a central component to mesoscopic electronic devices. The isothermal conductance of such a NIS junction can give access to the superconductor density of states [1] as well as to the energy distribution of electrons in the normal metal [2]. For SINIS structures with a small metallic island, one can couple superconductivity to single electron effects, which is used for metrological current pumping [3]. Similar structures have demonstrated a high potential for on-chip electronic cooling applications [4]. In this case, the superconductor energy gap suppresses tunneling of low-energy electrons, so that only high-energy electrons can tunnel. The electron population as a whole can reach a quasi-equilibrium state with a temperature lower than the phonon and the substrate temperatures [5]. Starting from a bath temperature of about 300 mK, electronic temperature reduction by more than a factor of 3 has been achieved in aluminum-copper hybrids that are voltage-biased just below the gap of superconducting Al [5–7].

The optimization of on-chip electronic refrigeration in SINIS devices has to tackle the following challenges: (i) Both electrons and phonons in the normal metal are coupled to the thermal environment that is at a higher temperature. An efficient cooling relies therefore on a thermal decoupling from the environment, including the substrate. (ii) The heat current from the normal metal to the superconductor is proportional to the tunnel barriers conductance. Reducing the oxide barrier thickness as to increase their conductance leads to the appearance of two-particle Andreev reflection processes at low energy, which deposit heat in the normal metal [7]. A too high junction transparency is therefore prejudicial to cooling. The obvious alternative is to increase the junction area at a constant transparency, which leads however to the next point. (iii) If not epitaxial, large-area solid state tunnel barriers are subject to local fluctuations of the barrier thickness, which are exponentially amplified in the local current density. In low-quality junctions, most of the current goes actually through so-called pin-holes, giving rise to an unwanted significant sub-gap current.

In this Letter, we present a novel fabrication method

for patterning a large area SINIS device of high quality and with a suspended normal metal. The method bases on a pre-deposited multilayer of metals, which can be prepared at the highest quality. The normal part is suspended in the first lithography, which isolates it from the substrate. The second lithography separately defines the junction area with any geometry of interest. Strikingly, transport measurements on these junctions show excellent characteristics, without any leakage contribution to the sub-gap current.

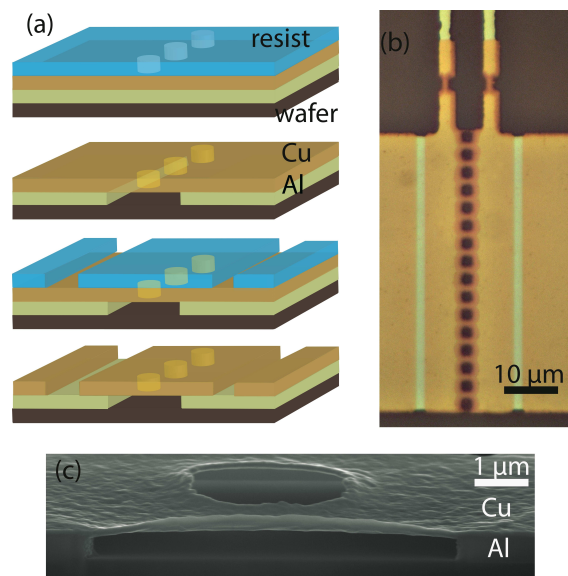


FIG. 1: (a) From top: fabrication starts with a Al/AlO<sub>x</sub>/Cu multilayer, on which a photoresist is patterned with contact pads and holes. Then, Cu and Al are successively etched, leaving a suspended membrane of Cu along the line of adjacent holes. A second lithography and etch define the Cu central island. (b) Optical microscope image showing regions by decreasing brightness: bare Al, Cu on Al, suspended Cu and substrate. On the top, two thermometer junctions are added. (c) Scanning electron micrograph of a sample cut using Focused Ion Beam showing the Cu layer suspended over the holes region. The thickness of Al and Cu is 400 nm and 100 nm respectively.

The fabrication starts with depositing a Al/AlO<sub>x</sub>/Cu multilayer on an oxidized silicon substrate (500 nm SiO<sub>2</sub>). Prior to deposition, the Si wafer is cleaned by baking it to 300° C for 4 hours inside our electron beam evaporator, at a pressure below 10<sup>-9</sup> mbar. The wafer is then let to cool down for one hour before depositing Al. The wafer is afterwards moved to a neighboring chamber where it is exposed to a static pressure of oxygen. The later process is known to produce a high-quality thin oxide barrier. The sample is finally moved back to the UHV chamber so that Cu can be deposited, without breaking vacuum.

A first deep ultra-violet lithography step [8] is used to define the overall device geometry. It includes a series of adjacent holes of diameter 2 μm and with a side-to-side separation of 2 μm, see Fig. 1. The copper layer is then etched away over the open areas using either Ion Beam Etching (IBE) or wet etching (HNO<sub>3</sub>, 65%, diluted 1:40 in DI water). Both approaches proved equally satisfactory. The aluminum is then etched through the same resist mask, using a weak base (Microposit MF CD 26 developer, diluted 1:2 in DI water). The etching time (270 s for an Al thickness of 100 nm, or 520 s for 400 nm) is controlled as to completely remove aluminum from the circular region within a horizontal distance of about 2 μm starting from a hole side. The line of adjacent holes visible in Fig. 1 therefore creates a continuous gap in the Al film, bridged only by a stripe of freely hanging Cu. The resist mask is finally removed.

The area of the NIS junctions is defined in a second lithographic step. Through the open areas, trenches are etched into the copper layer only, using one of the two methods cited above. These trenches allow to isolate a copper island from the outside, which will form the central normal metal part of the SINIS device. A top view of the complete device is pictured in Fig. 1b. Notably, the suspended copper membrane in the vicinity of the line of holes can be identified by its lower reflectivity with respect to the multilayer. Figure 1c shows a side view scanning electron micrograph of a junction after cutting the sample perpendicular to the line of holes, revealing the vertical structure of the SINIS device, as well as the complete removal of Al below the Cu bridge.

Low temperature transport measurements were performed in both a dilution refrigerator and a helium-3 system. Accurate electronic filtering of the lines was taken great care of. Twisted pairs of wires were passed through a single CuNi capillary filled with a two-component paste containing RF absorber [9] over 200 cm at the cryostat base temperature. The later method has proven to provide an effective microwave absorption down to dilution temperatures [10]. Additionally, two stages of π-filters were integrated at room temperature and in the sample holder. Four-point DC measurements are performed using home made electronics, in which a current bias is applied to the sample and the voltage is read out.

Fig. 2 shows the current-voltage characteristic and the

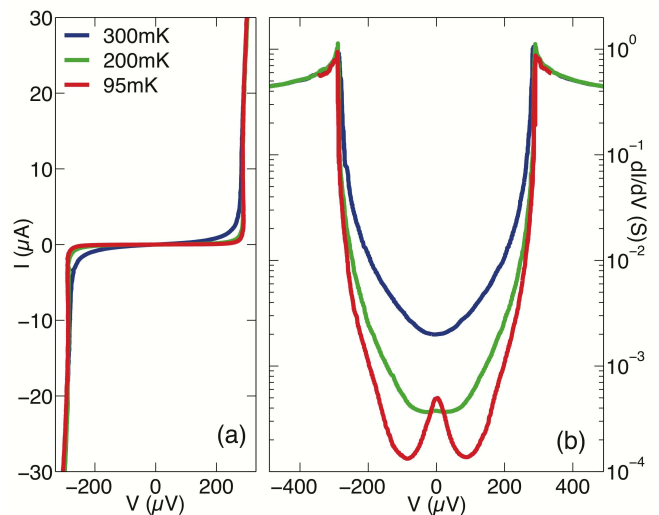


FIG. 2: (a) Current-voltage characteristic and (b) differential conductance of sample D at different cryostat temperatures, see Table 1 for its fabrication parameters.

numerically-derived differential conductance of a typical sample at various cryostat temperatures. These data are actually a combination of multiple curves covering different measurement ranges, extending over several decades of current values. Inside the gap marked by two differential conductance peaks, the sub-gap conductance is found to decrease strongly when temperature is decreased.

Similar results were obtained in a series of samples with different fabrication parameters listed in Table I. We have varied the thickness of the Al and Cu layers, as well as oxidation pressure or time in preparing the multilayers. Either dry etching (IBE) or wet etching of Cu was used, without noticeable difference. Electron beam lithography was employed for the second lithography step in samples B and C. All samples show an energy gap  $2\Delta \sim 350 \mu\text{eV}$ , consistent with the bulk gap of aluminum. The junctions' normal state resistances  $R_N$  roughly scale with the inverse junction area and increase with oxidation pressure.

In a semi-logarithmic representation, an increasing slope of the differential conductance as a function of voltage indicates a decreasing electronic temperature [11]. This behavior is clearly observed in Fig. 2b, which displays a sharp slope increase close to the gap edge. This clearly demonstrates electronic cooling in the normal metal. From our data analysis, we extract that at a bath temperature of 300 mK, electrons are cooled down to below 200 mK at the optimum bias point just below the gap.

At very low temperature, a zero-bias peak of the differential conductance is observed, which is a clear signature of coherent Andreev processes [7]. This defines a higher bound for the ratio  $G_{min}/G_N$  of the minimum differential conductance  $G_{min}$  to the high-bias conductance  $G_N$ .

This allows to estimate the maximum contribution of the leakage current with respect to the quasiparticle tunnel current. In large-area junctions, one expects a higher probability to obtain pin-holes. Based on our measurements of  $G_{min}/G_N$  values in the  $10^{-4}$  to  $10^{-5}$  range, we claim that our junctions, although not epitaxial, are pinhole-free. Furthermore, we were initially concerned that redeposition of the etched metals might shunt the junction, this was not observed. Finally, samples do not show any noticeable sign of aging, even when stored in ambient conditions for months.

The suspension of the normal metal in a SINIS structure is quite promising for electronic refrigeration applications. Inside the normal metal, cooled electrons are mainly coupled to phonons. Thus removing the thermal contact between the cooled metal and the substrate can significantly improve cooling of electrons *and* phonons in the normal metal. Despite this potential interest, thermal studies on micro-scale suspended metallic beams are still rare at the moment. Suspending the normal part in SINIS junctions was achieved with shadow evaporation technique and etch of the underneath layer using high pressure Reactive Ion Etching (RIE) [12–14]. Nevertheless, this approach suffers from several limitations. First, it starts with patterning a resist bilayer, which leaves little room for cleaning of the substrate before deposition. The resist itself can also pollute the metal structures deposited. Moreover, for practical reasons, the junction dimensions cannot usually be pushed well beyond the thickness of the resist. Eventually, the RIE etch dictates some material choices.

In comparison, our approach has several advantages. As fabrication starts with preparing the multilayer, the wafer can be baked in ultra-high vacuum environment, which we believe to be an essential ingredient for obtaining pinhole-free NIS junctions. Deposition can be made at high temperature, which enables epitaxial growth of

| id | $t_{Al}$<br>(nm) | $t_{Cu}$<br>(nm) | $P_{O_2}$<br>(mbar) | Area<br>( $\mu m^2$ ) | $R_N$<br>( $\Omega$ ) | $2\Delta$<br>( $\mu eV$ ) | $G_{min}/G_N$       |
|----|------------------|------------------|---------------------|-----------------------|-----------------------|---------------------------|---------------------|
| A  | 100              | 100              | 4000                | 1200                  | 14.6                  | 355                       | $2.2 \cdot 10^{-5}$ |
| B  | 100              | 50               | 5                   | 100                   | 64                    | 356                       | $5 \cdot 10^{-5}$   |
| C  | 100              | 50               | 100                 | 200                   | 31.8                  | 337                       | $2.1 \cdot 10^{-4}$ |
| D  | 100              | 50               | 1                   | 200                   | 2.8                   | 360                       | $3.7 \cdot 10^{-4}$ |
| E  | 400              | 100              | 100                 | 400                   | 33                    | 346                       | $5.5 \cdot 10^{-5}$ |
| F  | 400              | 100              | 1                   | 200                   | 7.8                   | 321                       | $2 \cdot 10^{-4}$   |
| G  | 400              | 100              | 1                   | 650                   | 1.7                   | 338                       | $8 \cdot 10^{-4}$   |

TABLE I: Parameters of different SINIS devices:  $t_{Al}$  and  $t_{Cu}$  are the thickness of the Al and Cu layers, respectively.  $R_N$  is the  $P_{O_2}$  is the oxidation pressure. All samples were oxidized for 15 minutes, except for sample A that was oxidized for 30 minutes.  $R_N$  is the normal-state resistance. The values of the sub-gap conductance ratio  $G_{min}/G_N$  were extracted from measurements below 100 mK (A to E) or 150 mK (F, G).

Al for an ultimate oxide barrier quality. The thickness of the layers can be increased independently of any resist thickness. The ease, cost-efficiency and flexibility in the etching and lithography techniques are actually promising for volume applications. Other material combinations than Cu and Al may prove interesting, provided an appropriate method of selective etching and over-etching of the two different materials exists.

In summary, we have presented a method for fabricating high-quality and large-area SINIS junctions, combining simple photolithography and etching techniques. The process yields a suspended normal metal membrane, bridging the superconducting leads. The junctions are of high quality with no pin-holes or unwanted shunt. Finally, when voltage-biased just below the superconductor gap, our samples display a significant electronic cooling.

Our work was funded by MICROKELVIN, the EU FRP7 low temperature infrastructure grant 228464, and SOLID project. The samples have been fabricated in the Nanofab facility at Institut Néel. The authors want to thank B. Pannetier, T. Fournier, T. Crozes, J.-F. Motte, S. Dufresnes, J. Muhonen and J. P. Pekola for help and discussions.

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