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► **To cite this version:**

A. Lecavelier Des Etangs-Levallois, Emmanuel Dubois, Marie Leseq, Francois Danneville, L. Poulain, et al.. 150-GHz RF SOI-CMOS technology in ultrathin regime on organic substrate. IEEE Electron Device Letters, 2011, 32 (11), pp.1510-1512. 10.1109/LED.2011.2166241 . hal-00639864

**HAL Id: hal-00639864**

**<https://hal.science/hal-00639864v1>**

Submitted on 16 Sep 2024

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# 150-GHz RF SOI-CMOS Technology in Ultrathin Regime on Organic Substrate

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**Abstract**—This letter provides an experimental demonstration of high-performance industrial MOSFETs thinned down to  $5.7\ \mu\text{m}$  and transferred onto a  $125\text{-}\mu\text{m}$ -thick polyethylene naphthalate foil. The die stack transferred onto the organic substrate comprises the  $200\text{-nm}$ -thick active layer and the  $5.5\text{-}\mu\text{m}$ -thick interconnection multilayer stack resulting in a light, compact, and bendable thin film. We unveil that dc and RF performances are invariant even for ultimate thinning down to the buried oxide layer. Furthermore, n-MOSFET performance is improved by  $1.5\times$  compared with previous work, and the first demonstration of  $100\text{-GHz}$  p-MOSFETs on an organic substrate is presented. Unity-current-gain cutoff and maximum oscillation frequencies as high as  $150/160\ \text{GHz}$  for n-MOSFETs and  $100/130\ \text{GHz}$  for p-MOSFETs on a plastic substrate have been measured, respectively.

**Index Terms**—CMOS, organic substrate, plastic, thin film.

## I. INTRODUCTION

THE field of flexible electronic has been quickly growing during the last decades, giving rise to numerous applications out of reach of conventional silicon microelectronic technologies. Various types of flexible devices have been reported such as OLED displays [2], solar cells [3], memories [4], or sensors [5]. These applications all belong to the so-called domain of macroelectronics that favors large surface and low-cost processing techniques [6]. Flexible electronics is also quasi-exclusively synonymous with organic semiconductors and high-throughput printing techniques whose major deficiencies lie in extremely poor carrier mobility ( $< 1\ \text{cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$  [7]) and coarse patterning resolution ( $\sim 10\ \mu\text{m}$  at best [8]). However, low cost and large surface are of no advantage for certain application classes for which bandwidth above a few megahertz is relevant. To cope with this problem, the proper heterogeneous cointegration of macroelectronics sub-circuits where performance is not required and leading-edge inorganic technologies based on ultrathin-film silicon or III–V

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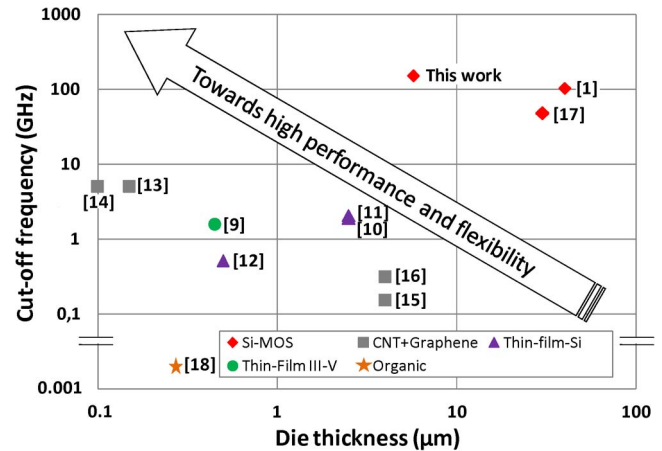


Fig. 1. Flexible electronics state-of-the-art chart reporting the cutoff frequency as a function of the inorganic layer thickness of flexible transistors [1], [9]–[18].

semiconductors has recently emerged as a promising solution [1], [9]–[17]. Along this philosophy, several strategies developed to achieve higher electrical performance are quantitatively compared in Fig. 1 that reports device cutoff frequencies versus die thicknesses, this latter parameter reflecting the ability of thin films to sustain extremely large mechanical deformations. For the sake of comparison, device performance based on organic materials has also been reported in this graph [18]. In the first cointegration flavor, devices are processed directly on a thin-film active material layer that is transfer bonded or deposited on a plastic substrate. Silicon or III–V material thin-film transistors [9]–[12], carbon nanotubes and graphene-based transistors [13]–[16], and ink-jet-printed devices [16], [18] are examples belonging to this category. Although this approach presents the major drawback of extremely low thermal budgets imposed by the organic substrate, cutoff frequencies reaching the gigahertz range have been achieved. However, numerous applications require even higher frequencies in the millimeter-wave range. A second approach has thus been developed by transferring circuit dies originally fabricated on conventional rigid wafers onto organic films. This strategy presents the distinctive advantage to directly give access to the hundreds of gigahertz range [1] at the reasonable extra cost needed to thin and transfer bond on flexible substrate dies originating from, e.g., state-of-the-art CMOS technologies. Based on this approach,  $100\text{-GHz}$  RF transistors originating from  $0.13$  to  $0.18\ \mu\text{m}$  CMOS bulk technologies have been reported after thinning to  $40$  or  $30\ \mu\text{m}$  as reported in [1] and [17], respectively.

The work reported here highlights state-of-the-art RF performance for n- and p-MOSFETs transfer bonded onto a

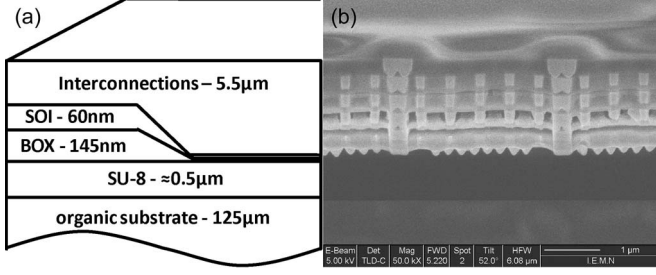


Fig. 2. (a) Stack description after die thinning and transfer onto an organic substrate, and (b) scanning electron microscope cross-sectional view taken in the center of a multigate-finger RF transistor.

plastic substrate, starting from a partially depleted silicon-on-insulator (SOI)-CMOS 65-nm technology. The fabrication process is presented hereinafter along with electrical measurements performed before and after thinning and transferred onto a polyethylene naphthalate (PEN) foil.

## II. DEVICE FABRICATION AND DESCRIPTION

SOI wafers have been used as the initial substrate for the industrial fabrication of multigate-finger 65-nm MOSFETs. The transfer onto an organic substrate requires two main steps: the removal of the initial rigid substrate by etching and the transfer of the thinned die onto an organic film. Silicon etching is conducted by successively using chemical-mechanical lapping and wet etching in HNA solution (HF (50%)/HNO<sub>3</sub> (65%) : 10/90) to quickly etch the main part of the 780- $\mu\text{m}$ -thick silicon handler substrate down to about 20  $\mu\text{m}$ . This method is similar to the one previously reported in [19]. A selective dry etching by xenon difluoride (XeF<sub>2</sub>) that features a Si:SiO<sub>2</sub> selectivity greater than 1000:1 [20] is subsequently used to gently remove the remaining silicon, using the buried oxide (BOX) of the SOI wafer as a stop layer. During the entire process, the front side of the sample is bonded onto a perforated temporary sapphire carrier in order to maintain mechanical rigidity even after reaching a film thickness in the micrometer scale. In the first step, the sapphire wafer is put in contact with a noncompletely polymerized AZ4560 photoresist layer spin coated onto the die. This temporary bonding is subsequently cured for 1 h in a 100 °C oven to achieve enough mechanical strength to withstand the shear stress involved in the lapping step. After thinning, dies are finally composed of the 5.5- $\mu\text{m}$ -thick back-end-of-line interconnect stack, the 60-nm-thick SOI layer, and the 145-nm-thick BOX layer (Fig. 2). The last step of this fabrication process is the transfer bonding of the ultrathin die onto an organic substrate using an SU-8 epoxy photoresist layer deposited on the back side of the thinned sample and thermocompression onto a 125- $\mu\text{m}$ -thick PEN film. The cooling of the bonded die is realized under a controlled temperature ramp (< 1 °C/min) and 500 mbar of applied pressure on both sides of the stack to limit bending due to thermal mismatch. Finally, the temporary carrier is debonded from the die by selective dissolution of the temporary adhesive photoresist layer in acetone, without damaging the organic film. The use of a perforated sapphire wafer allows the dissolution to occur in the whole area of the die, achieving a quick and homogeneous debonding.

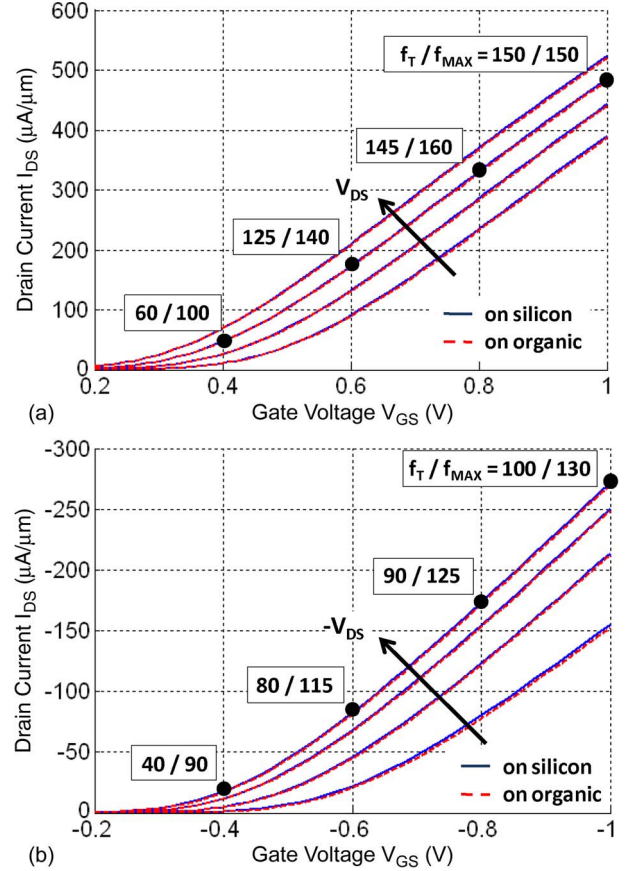


Fig. 3.  $I_{DS}$ - $V_{GS}$  characteristics measured on (blue lines) initial 780- $\mu\text{m}$ -thick SOI wafer and after thinning and transfer onto (red dotted lines) an organic substrate (a) for n-MOSFET under drain voltages  $V_{DS}$  from 0.75 to 1.5 V (step 250 mV) and (b) for p-MOSFET under drain voltages  $V_{DS}$  from -1.5 to 0 V (step -250 mV). Unity gain cutoff ( $f_T$ ) and maximum oscillation ( $f_{MAX}$ ) frequencies are reported for different gate voltages  $V_{GS}$  on the organic substrate.

## III. RESULTS AND DISCUSSION

DC and HF measurements have been performed on several components to obtain statistically representative results. Electrical characteristics presented in this letter focus on 64-gate-finger n- and p-MOSFETs in which the gate length and finger width are 60 nm and 1  $\mu\text{m}$ , respectively. The dc characteristics presented in Fig. 3(a) and (b) show  $I_{DS}$ - $V_{GS}$  characteristics measured on n- and p-MOSFETs, respectively, both on their initial rigid SOI substrate and after transfer bonding onto an organic substrate. It can be observed that static characteristics are perfectly matched, demonstrating that no modification due to the thinning and transfer process is introduced.

In addition, HF measurements reported in Fig. 4 show similar current and Mason's gains on inorganic and organic substrates, for both n- and p-MOSFETs. Cutoff frequencies as high as 150 and 100 GHz for n- and p-MOSFETs, respectively, are measured, for the first time to our knowledge, on an organic substrate. Maximum oscillation frequencies are found to slightly decrease after transfer onto an organic substrate to 160 GHz for the n-MOSFET and 130 GHz for the p-MOSFET. Cutoff and maximum oscillation frequencies measured for different gate voltages are also reported in Fig. 3(a) and (b). Aside from the demonstration of invariant dc characteristics, no HF major

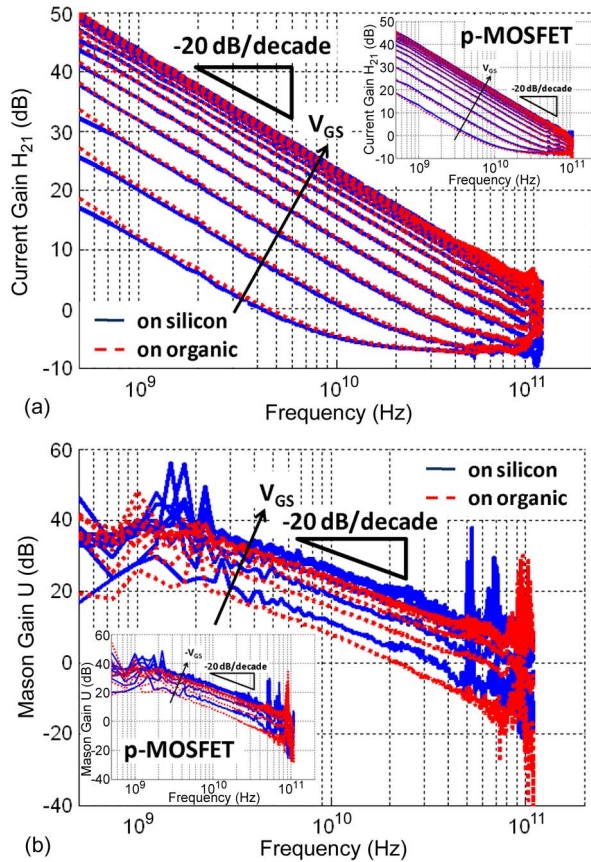


Fig. 4. (a) Current gain  $|H_{21}|$  and (b) Mason's gain  $U$  as a function of frequency for the n-MOSFET (respectively, p-MOSFET in inset) on its (blue lines) initial rigid handler substrate and after thinning and transfer onto (red dotted lines) an organic substrate under gate voltage  $V_{GS}$  from 200 mV to 1 V (step 50 mV) (respectively,  $-200$  mV to  $-1$  V, step  $-100$  mV).

degradations ensue from transfer on the PEN substrate. Only a slight variation of the maximum oscillation frequencies  $f_{MAX}$  that can be explained by an increase of the gate resistance  $R_G$  after transfer bonding on PEN can be observed. This resistance value was extracted using the methodology and small-signal equivalent circuit described in [21]. Gate resistances of  $R_G = 1 \Omega$  and  $R_G = 2 \Omega$  were extracted, respectively, on the initial inorganic substrate and on the organic substrate for the n-MOSFET.

#### IV. CONCLUSION

In this letter, industrial 65-nm partially depleted SOI MOSFETs thinned to the micrometer scale and transferred onto a PEN foil have been characterized in dc and HF modes. High-unity-current-gain cutoff and maximum oscillation frequencies have been demonstrated, i.e., 150/160 GHz for n-MOSFETs and 100/130 GHz for p-MOSFETs, respectively. Devices and circuits operating in this frequency range on a flexible plastic substrate open new perspectives for the development of nomadic and space, weight, and power (SWAP)-constrained applications. Future investigations will bear on the systematic characterization of electrical characteristics under large strain resulting from bending, stretching, and torsion.

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