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Bo Li, Shuibao Guo, Xuefang Lin-Shi, Bruno Allard. Design and implementation of the digital controller for boost converter based on FPGA. IEEE ISIE, Jun 2011, Gdansk, Poland. pp.1549 - 1554, 10.1109/ISIE.2011.5984391 . hal-00629371

HAL Id: hal-00629371

<https://hal.science/hal-00629371v1>

Submitted on 8 Jun 2012

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Design and Implementation of the Digital Controller for Boost Converter based on FPGA

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Abstract—Taking advantage of FPGA’s attractive features, this paper presents an improved digital pulse-width-modulator (DPWM) based sliding-mode controller (SMC) for boost converter that effectively alleviates the quantization effects. The dithering Multi-stage-noise-Shaping (MASH) DPWM is introduced exhibiting a better idle tone suppression effect that achieves relatively higher effective number of bit (ENOB). The Linear Feedback Shift Register (LFSR) replaces the cumbersome pseudo-random generator as the dither generation module that is proven to be more effective. The SMC with the proper sliding coefficients aiming at a better dynamic response than the traditional PID controller cooperates with our proposed DPWM. Two individual boards, an analog-to-digital converter (ADC) and a boost converter, connecting to a Virtex-II FPGA platform compose a close-loop test environment. Experimental results verify the switching-mode-power-supply (SMPS) close-loop operation at 1MHz switching frequency with an 11-bit effective DPWM resolution.

I. INTRODUCTION

Owing to the development of modern integrated circuit technology especially the field-programmable gate array (FPGA), digital controller for switching-mode-power-supply (SMPS) offers many advantages compared to the readily available analog counterparts which still dominate the current portable-device market. Meanwhile integration leads to very high switching frequency. Digital controllers are seldom proven above 10MHz of switching frequency. Electromagnetic interference (EMI) issues also lead to fixed frequency converters. The challenge is to accommodate both constraints and satisfactory dynamic performances but with a reasonable efficiency. Therefore many solutions are proposed to solve the problems of the controller. Figure 1 shows the three main parts of the digital feedback loop for a boost converter. Analog-to-digital converter (ADC) acquires and scales the output of the boost converter and provides digital signal to the controller. Benefiting from the digital approach, the control law block can implement advanced algorithms to reach better control performance. Digital pulse-width-modulator (DPWM) is suitable to convert the control signal to a variable duty cycle signals which drive the switches in the power stage.

A DC-DC converter is a kind of variable structure system (VSS) due to the intrinsic switching nature [1], [2]. Meanwhile, a sliding-mode controller (SMC) is a nonlinear controller which offers an alternative to implement a control action which exploits the inherent variable structure nature of the DC-DC converter as apposed to the analog control implementation. In order to address the requirement of fixed

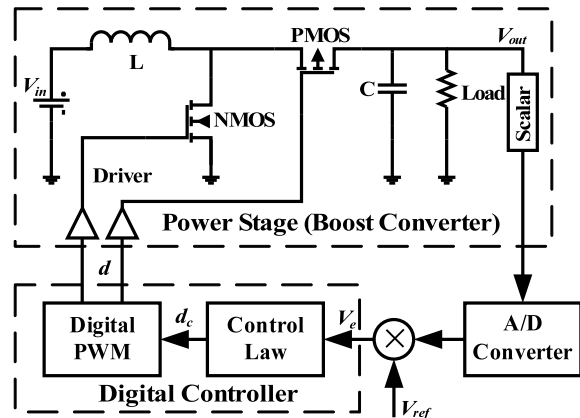


Fig. 1. Circuit structure of digitally controlled boost converter

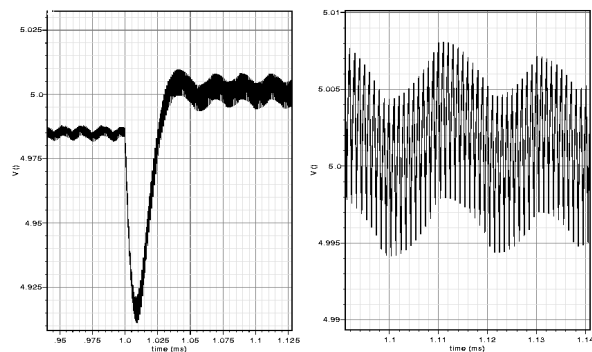


Fig. 2. Simulated LCO output of the boost converter with 10-bit ADC and 8-bit DPWM

and controlled switching frequency, a PWM-based SMC is derived from a Hysteresis Modulator (HM) based SMC [3], [4] and [5]. It has been also proposed in [6] and [7], where the switching frequency is in the range of hundreds of kHz. Unfortunately, most of the published papers only verify SMC in analog approach that limits the bandwidth, as well as reduces the flexibility of implementation [8], [6]. The above-mentioned SMC is the PWM-based SMC that can implement in FPGA to generate a control signal employing the concept of equivalent control [9]. The SMC is relatively fast to achieve desired specification and is robust with respect to matched internal and external disturbances.

Due to the quantization effect that both exists in ADC

and DPWM, an limit-cycle oscillation (LCO) may occur that imposes restrictions on not only the compensator but also DPWM [10], [11]. As shown in figure 2, obvious LCO may be introduced if the quantization step of the DPWM is too coarse. According to the static and dynamic conditions proposed by [10], there is no doubt that a high-resolution DPWM is a necessary condition to avoid the LCO. Relying on the excellent linearity, the advantages of the counter-comparator DPWM is obvious in the time-domain; nevertheless, for a n -bit DPWM dedicating to a boost converter of which the switching frequency is f_s , an external clock must reach $2^n \cdot f_s$ theoretically that is rarely achievable with the current integrated circuit technology or at the risk of large power consumption as well as the necessitate for an elaborate clock tree. In order to overcome the above-mentioned problems and achieve enough precise voltage, a delay-line DPWM [12], a hybrid delay-line [13], a segment delay-line DPWM [14] and a ring-MUX DPWM [15] are proposed to obtain a delay time by adopting a series of tight logic cells. However these approaches suffer from manufacturing variability and occupy large chip area. Based on the “step calculation” principle, the dithering DPWM is proposed to achieve a high-resolution in a software manner without increasing the chip area and power consumption [11], nevertheless, the ripple in the output voltage is aggravated, so the effective number of bit (ENOB) is limited.

Delta-sigma (Δ - Σ) modulator (MOD) is a well-known over-sampling structure that samples at a over-sampling rate (OSR) to realize noise-shaping effect [16]. Referring to the power stage of boost converter as the post-filter in digital-to-analog converter (DAC), DPWM can also adopts the over-sampling technique to pre-process the most-significant-bit (MSB) m -bit of the duty cycle command d_c , in other words, the required external clock frequency can reduce to $2^{n-m} \cdot f_s$, where n is the length of d_c . However the slow convergence due to a low frequency periodic behavior in a first-order Δ - Σ DPWM, which is known as idle tone effects, produces a low-frequency noise in the power stage. Meanwhile higher order implementations may bring potential stability problems [16], [17]. The Multi-stAge-noise-SHaping (MASH) type [18] is an effective trade-off between the first-order and higher-order Δ - Σ DPWM, while low-frequency tone still exists. In this paper, an insight into the idle tone effects for Δ - Σ DPWM, particularly for MASH Δ - Σ DPWM, is presented. Based on the analyses of two solutions that can suppress the idle tone, higher order modulator or dither[16], an efficient dither 1-1 MASH structure is employed.

The paper is organized as follows. Section II gives details on the implementation method of the SMC for the boost converter. Section III analyzes the idle tone suppression technique and describes the proposed DPWM. All proposals are verified experimentally in a FPGA based platform, and the results are discussed in section IV.

II. PWM-BASED SMC FOR BOOST CONVERTER

The small signal and average model for boost converter can be express as

$$\dot{I}_L = -\frac{1-D}{L}V_o + \frac{1}{L}V_{in} \quad (1)$$

$$\dot{V}_o = \frac{1-D}{C}I_L - \frac{1}{RC}V_o \quad (2)$$

where the two state variables I_L and V_o stand for the inductor current and output voltage; C , R and L are the capacitance, load resistance and inductance, respectively; V_{in} and D are the input voltage and duty cycle to the boost converter.

The sliding surface can be introduced as [19], [4] and [20]

$$S(t) = k_1 \cdot e + k_2 \cdot \dot{e} + k_3 \cdot \int e dt \quad (3)$$

where k_1 , k_2 and k_3 represent the control parameters, e is ($V_{ref}-V_o$). V_{ref} and V_o are the reference and output voltage respectively. According to the equivalent control concept, the tracking error will be converged to zero if the invariance conditions are verified. In other words, the system is definitely trapped on the sliding surface leading to

$$S(t) = \dot{S}(t) = 0 \quad (4)$$

For power converters, the duty cycle D can be deduced from the equivalent control function, provided that the switching frequency is relatively high [6], thus the converter is controlled here by varying the duty cycle and keeping the switching frequency constant, that could be expressed as

$$D = \frac{(V_o - V_{in})}{V_o} + \frac{k_3}{k_2} \cdot L \cdot C \cdot \frac{(V_{ref} - V_o)}{V_o} - \left(\frac{k_1}{k_2} - \frac{1}{R \cdot C} \right) \cdot \frac{L \cdot C}{V_o} \cdot \frac{dV_o}{dt} \quad (5)$$

The Lyapunov function can be chosen to determine the motion range [21]. Using the Routh's stability criterion, the stability conditions can be satisfied if all the parameters k_1 , k_2 and k_3 have the same sign. The convergence dynamics can be chosen as a standard second-order system form:

$$s^2 + 2\xi\omega_n s + \omega_n^2 = 0 \quad (6)$$

where the damping ratio ξ and undamped natural frequency ω_n are respectively:

$$\omega_n = \sqrt{k_3/k_2}, \quad \xi = k_1/2\sqrt{k_3k_2} \quad (7)$$

So the sliding parameters can be obtained by

$$\frac{k_3}{k_2} = 4\pi^2 f_n^2 \quad (8)$$

$$\frac{k_1}{k_2} = 4\pi\xi f_n \quad (9)$$

where f_n is the bandwidth of the controller's response. According to the simulation results, we set ξ equals 0.75, and $f_n = \frac{f_s}{60}$ in order to achieve better dynamic response performance.

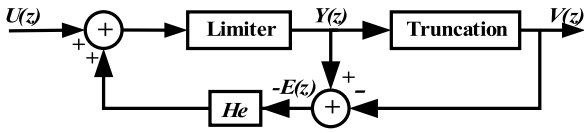


Fig. 3. Error feedback structure for DPWM

III. THE DITHER 1-1 MASH Δ - Σ DPWM

To implement the proposed SMC in digital approach, a digital-PWM must be introduced. Owing to the inherent truncation configuration, the error feedback structure [16] turns out to be an efficient model for Δ - Σ DPWM as shown in figure 3. The corresponding transfer function is

$$V(z) = U(z) + [1 - He(z)] \cdot E(z) \quad (10)$$

The first-order Δ - Σ modulation (MOD1) and the second-order Δ - Σ modulation (MOD2) can be implemented by setting $He(z) = z^{-1}$ and $He(z) = z^{-1} \cdot (2 - z^{-1})$ separately [22], [17]. Taking MOD2 as an example, the signal transfer function (STF) and the noise transfer function (NTF) are given by

$$STF(z) = 1 \quad (11)$$

$$NTF(z) = (1 - Z^{-1})^2 \quad (12)$$

Therefore MOD2 can reach infinite gain at zero frequency as well as lead to the complete elimination of DC quantization errors, so

$$V(z)|_{z=1} = U(z) \quad (13)$$

Although the noise-shaping can reduce the high frequency requirement for the core DPWM to some extent, the consequent idle tone introduces the in-band noise that only associates with DC input for a certain Δ - Σ DPWM. The power stage in SMPS works as the post analog low-pass filter in Δ - Σ DAC to suppress most of the out-of-band noise power in which the corner frequency $f_o = 1/2\pi\sqrt{LC}$ [23] must be sufficiently lower than the switching frequency and even than the frequency of the idle tone.

Higher-order modulator and dither are proven to be two feasible solutions in ADC to suppress the idle tone effects. The same method is compatible with DPWM. Many papers concentrated on the higher-order approach in which [17] exhibits a MOD2 adopting above-mentioned error feedback structure. An increasingly popular structure, MASH MOD, can partially solve the stability problems associated with higher-modulators as shown in [18]. In figure 4, a MASH Δ - Σ DPWM is presented in which both stage contains a first-order internal loop, resulting in a global second-order noise-shaping effect, but preserving the robust stability as the first-order loop. In order to have the same noise-shaping effect as MOD2, the assumption

$$H_1(z) \cdot NTF_1(z) - H_2(z) \cdot STF_2(z) = 0 \quad (14)$$

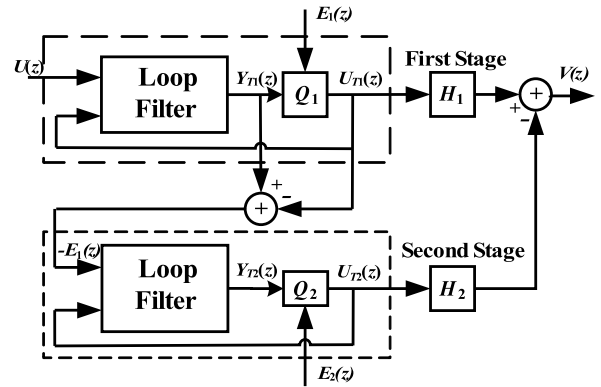


Fig. 4. A cascade structure of two-stage MASH modulators

must be absolutely true. For the 1-1 MASH Δ - Σ DPWM, the digital filter stages H_1 and H_2 are selected as

$$H_1(z) = STF_2(z) = 1 \quad (15)$$

$$H_2(z) = NTF_1(z) = 1 - z^{-1} \quad (16)$$

However it still suffers from the idle tone existing in each stage and particularly the tone's overlapping between the two stages that introduce extra low-frequency interference without any attenuation in the baseband [17].

Figure 5 shows the transient simulation results by feeding 1025 (decimal) to a 11-bit DPWM (5-bit MOD) which indicates that the MOD2 still generates the idle tone compared to the MOD1. To avoid the idle tone, the MOD must be of high order and then have enough quantization levels. Unfortunately, more quantization levels that contain large offsets compared with the base digit will simultaneously lead to the instability problem that also deteriorates the output signal within a certain power stage filter. The undither MASH MOD, the same order as the MOD2, shows almost the same transient performance as MOD2. As shown in figure 6, a serious transient variation occurs because the higher rate of output variations introduces extra digit-levels. So a dither module must be included here aiming to re-create the Δ - Σ sequence as well as suppress the idle tone effects.

According to [16], the input to the latter stage must be scaled to fit within the stable input range. So the bit extension module should be added here for the ease of calculation of the latter stage.

To avoid the large offset of digit, bit distribution through each stage is another important issue for designers. All referred bit distribution proposals belong to multi-bit quantizers. It is inherently more stable, and the no-overload range of the quantizer is increased, meanwhile it may have very high ENOB even at low OSR [16]. So two multi-bit quantizers are adopted in our design. Figure 7 shows the power spectral density (PSD) for 2+4 (2MSB at the output of the first stage and 4MSB at the output of the second stage, similarly hereafter), 3+3, 4+2. Here the switching frequency is 1MHz, meanwhile the

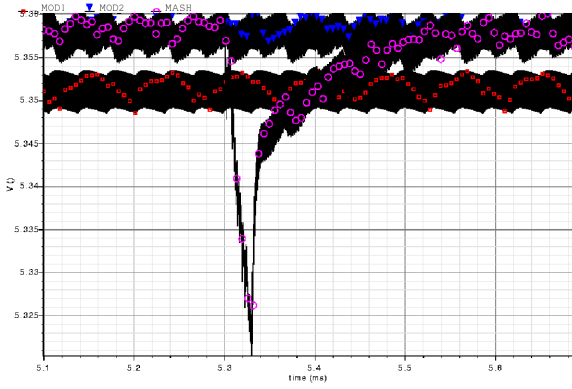


Fig. 5. Idle tone interferences within the simulation of MOD1, MOD2 and undither MASH MOD by feeding a constant DPWM input signal (1025 of 11-bit DPWM)

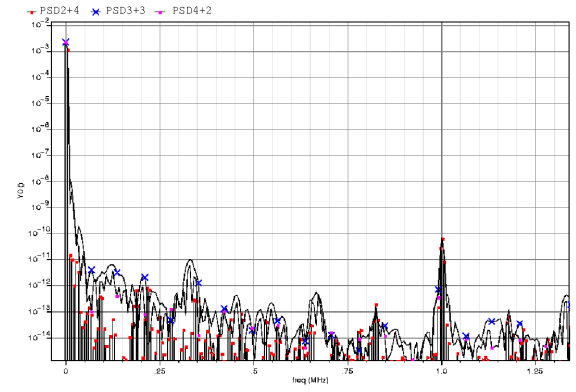


Fig. 7. Noise-shaping comparison between three types 1-1 MASH Δ - Σ modulations

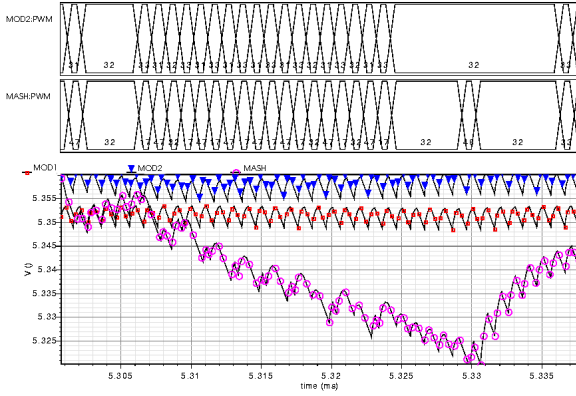


Fig. 6. Enlarged waveform of the transient variation point

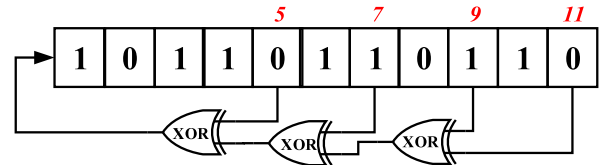


Fig. 9. Proposed dither 1-1 MASH Δ - Σ DPWM

$$V(z) = U(z) + (1 - z^{-1})^2 E_2(z) + \frac{1}{n-1} (1 - z^{-1})^2 D(z) \quad (18)$$

where $D(z)$ is the dither signal, $E_2(z)$ is the truncation error of the second stage. As above-mentioned, we set $m_1 = 2$ and $m_2 = 4$. The output spectrum indicates the idle tone attenuation effects as shown in figure 10.

IV. EXPERIMENTAL RESULTS

To verify the function and timing issues of the proposed MASH Δ - Σ DPWM with SMC, a low voltage boost converter is connected to a Virtex-II Pro XC2VP30 FPGA board as

core frequency is around 18.6KHz in our design. According to figure 7, 2+4 modulation structure is a better choice.

According to figure 7, some noise signals below corner frequency still exist due to the idle tone effects, although they are significantly attenuated. Therefore dither method is proposed here to further suppress the idle tone, also known as improving the noise-shaping effect. Inspired by [24], a $(n-1)$ -bit linear feedback shift register (LFSR) is added to generate the dither signal to the second stage as shown in figure 8. The dither module is placed just before the quantizer because the dithering signal can behave as the same manner as the quantization noise and then permit a large amount of dithering. The Fibonacci LFSR is adopted here as show in figure 9. Here "01101101101" is set as the initial code in register array. The corresponding feedback polynomial is

$$x^{11} + x^9 + x^7 + x^5 + 1 \quad (17)$$

where '1' corresponds to the input of the first bit. Finally the overall $m=6$ bits are sent to a 6-bit core DPWM which is implemented by the counter-comparator DPWM that brings down the maximum frequency from $2^{11} \cdot f_{sw}$ to $2^6 \cdot f_{sw}$.

So the overall output signal is given by

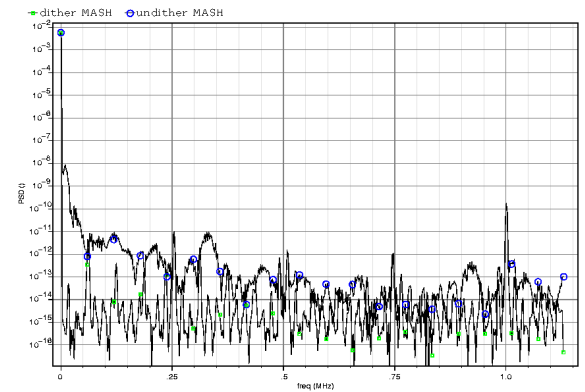


Fig. 10. Idle tone attenuation comparison between dither and undither 1-1 MASH modulator

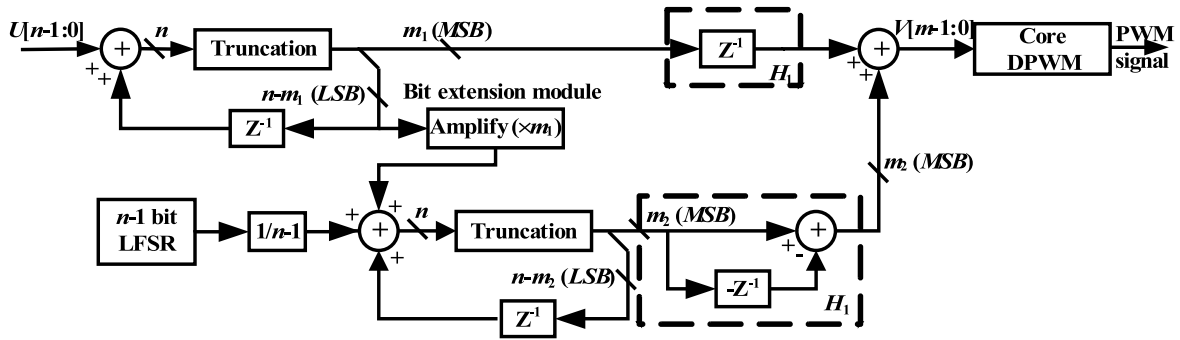


Fig. 8. Proposed dither 1-1 MASH Δ - Σ DPWM

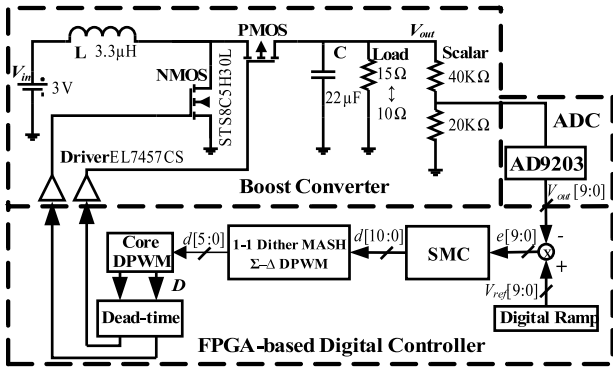


Fig. 11. Circuit configuration of the FPGA-based digital controller for boost converter

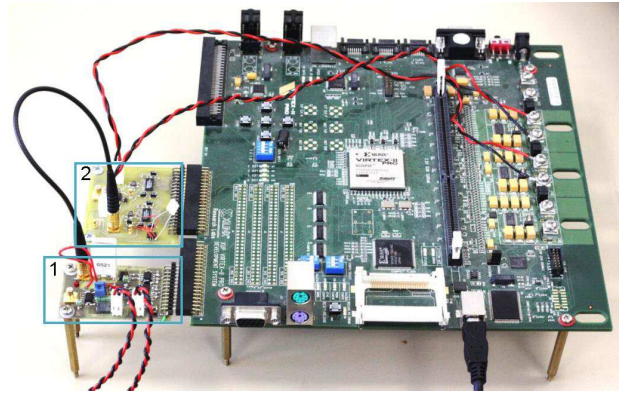


Fig. 12. The FPGA-based experiment platform for the proposed digital controller

TABLE I
PARAMETERS OF THE DIGITALLY CONTROLLED BOOST CONVERTER

R	Nominal load	15 Ω
L	Inductor	3.3 μH
C	Capacitor	22 μF
V_{in}	Input voltage	3.0V
V_{out}	Output voltage	5.0V
f_{sw}	Switching frequency	1MHz
ADC	AD9203	10-bit
$N_{\Sigma-\Delta}$	MASH Σ - Δ resolution	5-bit
$N_{Core.DPWM}$	Core DPWM resolution	6-bit

shown in Figure 11. Subtracting the quantized output of the boost converter, the digital ramp module generates a ramp signal that assures a smooth start process. Dead-time module handles the output of the DPWM to avoid the shoot-through issue. Briefly speaking, it is necessary to preserve an actual safe interval between the two ON-states of the power MOSFETs. From the device utilization report, the total equivalent gate count for design is 42288 with 1776 additional JTAG gates for IOBs. Figure 12 is the experiment platform in which board 1 is the boost converter and board 2 is the ADC. Basic configuration parameters are shown in Table I.

Figure 13 shows the output voltage and the corresponding high-side PWM signal of the digital SMC controller in steady-state operation at 1MHz. It exhibits sufficient stability in the output voltage. Figure 14 shows the transient output voltage

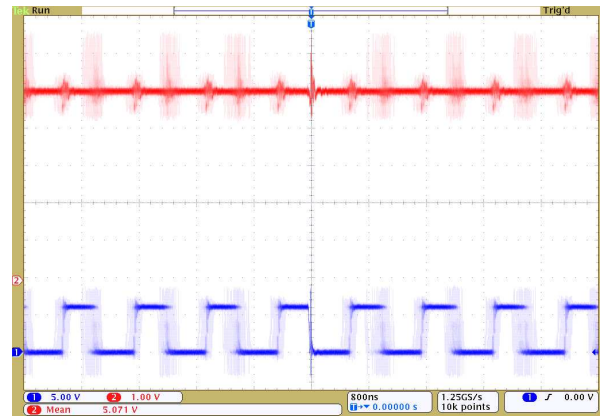


Fig. 13. High-side PWM and output voltage in steady state at $f_{sw}=1\text{MHz}$

response when load varies from 15 Ω to 10 Ω (using dither 1-1 MASH Δ - Σ DPWM). It indicates that the proposed SMC has satisfactory dynamic performances. These results prove that the dynamic response is very fast ($<25 \mu s$) and the undershoot on the output voltage is also very small ($<70\text{mV}$) which is less than 1.4% of the output voltage (5V). The performance of SMC is summarized in Table II compared with a PID controller. Nevertheless, this test executes a conservative load variation exclusively in order to guarantee to work in the

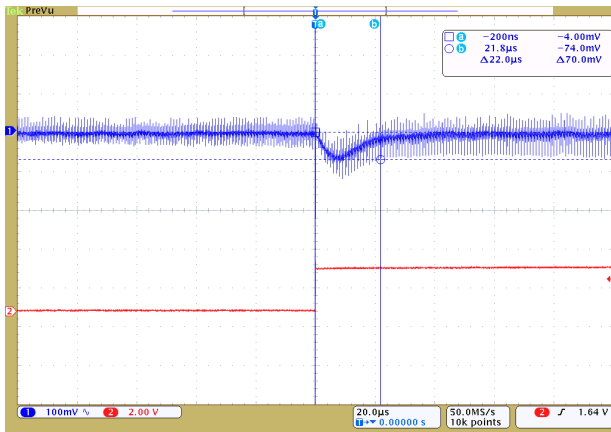


Fig. 14. Transient output voltage response when load goes from 15Ω to 10Ω

TABLE II
PERFORMANCE SUMMARY

Load change	Performance index	SMC	PID Controller
15Ω to 10Ω	Recovery time	25μs	80μs
	Undershoot	70mV	86mV
10Ω to 15Ω	Output ripple	30mV	30mV
	Recovery time	42μs	102μs
	Overshoot	90mV	92mV
	Output ripple	30mV	30mV

continuous current mode (CCM). In effect, a load variation from 45Ω to 10Ω is available in a serious condition test. Moreover as a further improvement, it is possible to add an observer to obtain load change information which helps to further ameliorate the control performance.

V. CONCLUSION

Cooperating with optimized SMC, a dither module is added to the 1-1 MASH Δ - Σ DPWM to restrain the idle tone effects. The FPGA-prototype is implemented in the Virtex-II Pro XC2VP30 platform serving a 1MHz boost converter. The experimental results are satisfactory. Other nonlinear controller algorithms are under consideration so as to make a comparison with the controller proposed in this paper. A further ASIC in a 0.35μm CMOS process is estimated to occupy 0.32mm² of silicon area on condition that the core utilization ratio is 75%, and the current consumption is roughly 100μA/MHz. Therefore this approach anticipates a better performance and estimates to archive higher power efficiency in ASIC.

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