Efficient Low Cost Process For Single Step Metal Forming of 3D Interconnected Above-IC Inductors

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Abstract— **This paper presents a novel and efficient low cost process capable of integrating high-Q above-IC inductors and their interconnects using a single electroplating step. It relies on the SU8 and BPN resist as well as an optimized electroplating technique to form the 3D interconnected inductor. The SU8 is used to form a thick layer located underneath the inductor to elevate it from the substrate. Then, the BPN is used as a high resolution mold (16:1) for copper electroplating. Standard or time optimized electroplating is later used to grow copper in a 3D manner, making the transition between all metallic layers straight forward. High-Q (55 @ 5 GHz) power inductors have been designed and integrated above an RF power LDMOS device using this process. Finally, the process capabilities are demonstrated by integrating a solenoid inductor using only two lithography masks and a single electroplating step.**

I. INTRODUCTION

The limited availability of low-loss integrated inductor structures has long hindered the development of integrated circuits such as passive filters, matching networks, transformers, etc. Been mostly planar, these inductors tend to suffer from high losses and low quality factors (Q) at RF frequencies. These losses result generally from dielectric and/or magnetic losses incurred from coupling between the inductor and the host substrate, as well as from resistive losses due to the use of thin and relatively high resistivity conductors. Generally, the substrate poses the main challenge for High-Q inductor design and integration when its resistivity is very low, which is the case of high power RF devices like LDMOS.

Some approaches have been proposed to address the above issues for enhancing the overall performance of inductors. High resistivity silicon [1] or SOI [2] substrates offer an ideal solution, but they either aren't an option for all silicon technologies or present major drawbacks like high cost, limited heat dissipation and difficult implementation of backside source contact. Etching the silicon under the inductor [3], micromachining suspended planar coils or 3D structures [4][5] are alternatives but they suffer from high process complexity/cost and from incompatibility with above-IC processing. Inserting a patterned ground shield between the inductor and the substrate [6][7] enhances the performance, but, this solution appears ineffective for very low resistivity substrates [8].

Therefore, a single yet efficient technology for inductors integration that can reply to both RF performance and industrial needs and compatible with existing IC technologies is required. Moreover, to meet the requirements for various applications, the process must allow depositing a dielectric with thicknesses ranging from few microns to more than 100 µm as well as ribbons with different widths and thicknesses. For example, unlike low power inductors, High-Q power inductors requires both thick dielectric and metallic layer [8], which was always a blocking point for inductor integration on high power devices.

In a previous work [8], we demonstrated means to optimize Above-IC inductors and presented a low cost SU8 based Above-IC process [9] capable of integrating High-Q RF power inductors. However, this process was mainly optimized for planar inductors and like other processes, its complexity rises drastically if complex shaped interconnects or structures like multilevel or 3D inductors have to be integrated. Figure 1 illustrates the technological steps of a typical planar process [9] used to integrate a distributed above-IC inductor. The technological steps are the following:

(a) Sputtering the first seed layer and depositing the first negative photoresist layer. The openings in the resist will be used as a mold for copper electroplating of pads.
(b) Electroplating copper to form the first metal level.
(c) Dissolving the negative resist.
(d) Depositing a second negative resist to form via holes.
(e) Electroplating copper vias.
(f) Dissolving the negative resist and etching the seed layer.
(g) Depositing the SU8 layer which is used as dielectric. The presence of vias during spinoff results an uneven SU8 surface which then requires mechanical polishing.
(h) Sputtering the second seed layer and depositing the third negative photoresist layer.
(i) Electroplating the third metallic layer.

(j) Dissolving the negative resist and etching the seed layer.

Therefore, for 3D integration, this process suffers from several drawbacks such as:

- The relatively high number of technological steps that increases cost and processing time.
- The presence of a mechanical polishing step to level the SU8's surface, which increases the risk of wafer break and the processing time, is critical for manufacturing.
- The high mechanical strain on the wafer due to the presence of the SU8 on its whole surface (20 MPa for 90 µm thick SU8 [10]).
- The presence of the seed layer at the interface between interconnects and the inductor, which can be broken during a mechanical stress (during backside thinning, for example).

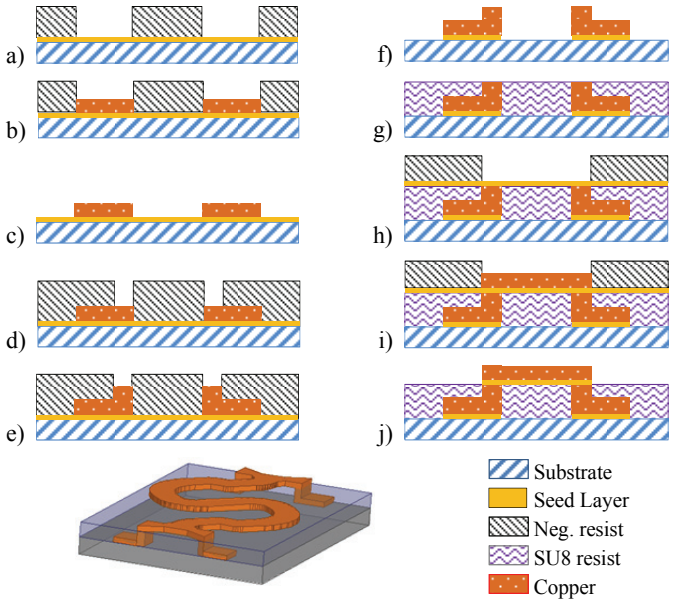

Figure 1. Interconnected inductor integration steps using a planar Above-IC process

In this work, we present a novel and efficient low cost SU8 based process that overcomes all previous drawbacks and that leads to Above-IC integration of 3D interconnected inductors using a single metal electroplating step. The process relies on SU8 patterning, 3D seed layer deposit and 3D copper electroplating to form the inductor with its interconnects in a single metallization step. As a result, the number of technological steps and cost is reduced while enhancing both mechanical properties and electrical performance of the inductors. Moreover, the process is compatible with standard lithography and electroplating techniques, which makes its industrial implementation easy and straightforward. The process was used to integrate RF power inductors above a 50 W RF LDMOS transistor. Its capability is also demonstrated by integrating a solenoid inductor using two lithography masks and a single electroplating step.

II. PROCESS AND RESULTS

A. 3D interconnected inductor forming technique

Three-dimensionally copper electroplating is the key point to create the 3D interconnected inductor in a single metallization step. To achieve this, three prerequisites must be met which are: 1/ the dielectric must be patterned at specific locations; 2/ the seed layer deposit must be 3D; 3/ the copper electroplating needs a thick photoresist mold with a good resolution (high aspect ratio).

1) Dielectric resist choice and patterning

In this work, the SU8 resist was used as a dielectric for its good electrical characteristics for frequencies up to 7 GHz [11] and for its convenient technological properties. This resist allows depositing a dielectric layer with a wide range of thicknesses in a single spin-coat. Shapes with aspect ratios higher than 16:1 and vertical sidewalls can be realized.

Patterning and locating the dielectric under the inductor allows its elevation from the substrate while enabling direct access to the underlying substrate (metallic pads) (Figure 2.a). Therefore, after successful deposit of a 3D seed layer, both the substrate and the dielectric surfaces/faces will be electrically connected. This electrical continuity allows 3D copper electroplating of the inductor, vias (interconnects) and pads in a single step. This process presents a lot of advantages such as mainly the elimination of the mechanical polishing of the SU8, the reduction of mechanical strain, the large improvement of cost and processing time, etc.

The process isn't limited to a single dielectric layer since, if needed, multi-layers can be interconnected in a single electroplating step by simply adding additional SU8 layers as shown on Figure 2.b. As illustrated, two SU8 layers are used, one deposited on the entire wafer surface with via openings, and the other one only located under the inductor. This kind of topology poses a challenge for seed layer deposit as highlighted in the next paragraph.

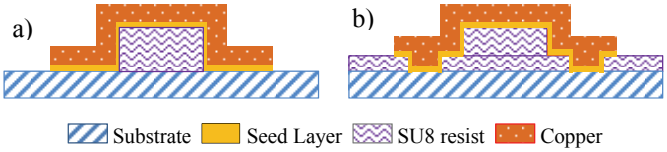

Figure 2. Methods of forming a 3D interconnected inductor: a) SU8 only under the inductor. b) two layers of SU8

2) 3D Seed layer deposit

For copper growing with a single electroplating step, a 3D seed layer must be deposited insuring the electrical continuity between the substrate and the dielectric surfaces. This step poses a great challenge because of the vertical nature of the SU8's sidewalls. Furthermore, depending on the pattern's shape (pillar like or hollows), size, density and the used equipment (evaporation, sputtering), the seed layer deposit can be fairly easy or quite difficult. In fact, if evaporation technique is used, the presence of a high vertical sidewall might create an amber-like (shadow) effect which can produce a seed layer locally thinner or even voids (Figure 3.a). Such thin or inhomogeneous seed layer can fuse while applying the

electroplating current. Sputtering technique can enhance the seed layer thickness homogeneity. However, in some severe cases, like the presence of narrow hollows (Figure 2.b), approaches like seed layer enhancement (SLE) must be used [12]. This SLE is done using a chemical solution for deposition of a thin 3D conductive layer on all the surfaces.

When the seed layer is homogenous, the electroplating current will circulate in a 3D matter allowing copper growing on all exposed surfaces and sidewalls which are bound into the electroplating mold.

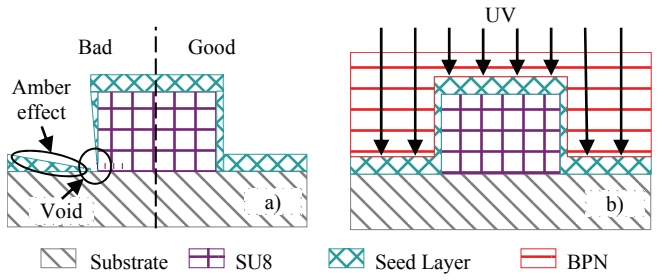

Figure 3. Process difficulties: a) Seed layer. b) BPN lithography

3) *Photoresist for thick mold formation*

The choice of resist for mold formation is related to two major parameters. Firstly, it must be capable to reach high thicknesses as well as high aspect ratios. Secondly, it must be easily strippable. Under these conditions, the BPN negative resist appears the best choice. This resin has been optimized in our clean room to reach thicknesses as high as 160 µm with an aspect ratio of 16: 1 [10]. The main difficulties were to find the correct annealing temperatures/time, UV dose and development time since the presence of pillars/hollows creates two (or more) distinctive thicknesses to insulate (Figure 3.b).

B. Experimentation and results

For experimentation, 3D interconnected high-Q power inductors similar to the one presented on Figure 1 have been designed and integrated above a very low resistivity substrate using the following technological steps (Figure 4):

a) Deposit of an 85 µm thick SU8 layer by spin coating and lithography to locate the SU8 under the future inductor.
b) Evaporation of a titanium/gold seed layer followed by the deposit of a 100 µm thick BPN layer using spin coating, and apply photolithography to create molds for electroplating.
c) Copper electroplating.
d) BPN dissolution and seed layer etching.

The process used for an 85 µm thick SU8 layer deposit is the following:

- Coating of SU8 3050: 8 ml spun at 1500 RPM for 30s.
- Pre-anneal: 1 min @ 65 °C then 40 min @ 95 °C.
- Exposure: 360 mj/cm².
- Post exposure bake: 1 min @ 65 °C then 3 min @ 95 °C.
- Development: 15 min using PGMEA.
- Final anneal: 1 min @ 65 °C then 2 min @ 125 °C.

For molds, we deposited a 100 µm thick BPN layer using the following steps:

- Coating of BPN: 8 ml spun at 750 RPM for 30s.
- Pre-anneal: 3 min @ 60 °C then 4 min @ 120 °C.
- Exposure: 1350 mj/cm².
- Development: 5 min using TMAH.

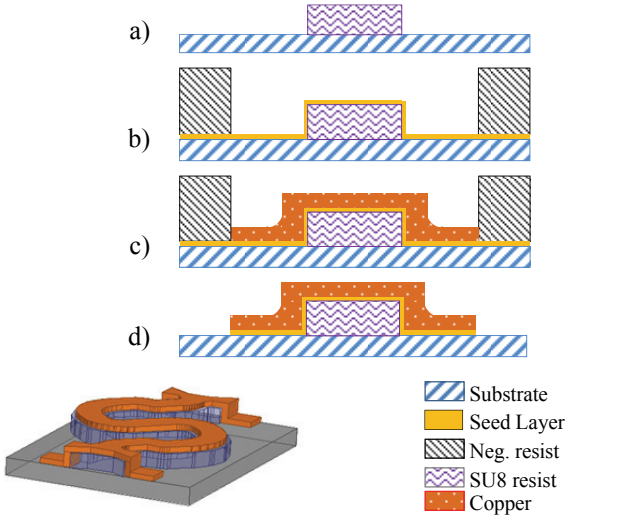

Figure 4. 3D interconnected inductor integration steps using the novel process

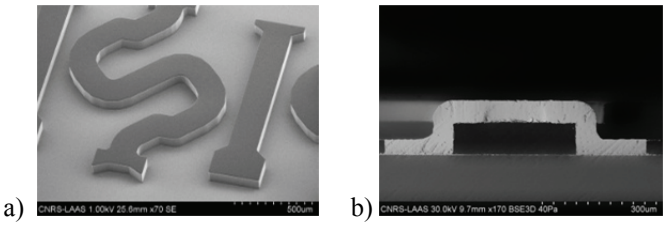

Figure 5. SEM micrographs of: a) the patterned SU8. b) cross-section of the interconnected inductor

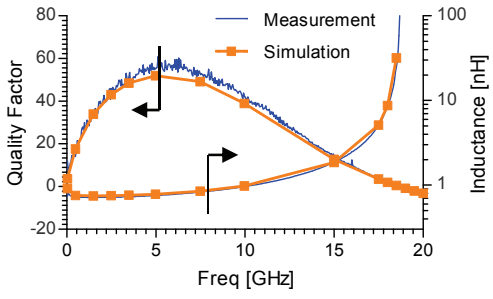

Figure 6. Measurement vs. simulation of the inductor's Q factor and inductance value

Under probes measurements of these inductors exhibit a Q value of 55 at 5 GHz for a total inductance value of 0.8 nH (Figure 6). The good agreement between measurements and simulations must be pointed out, which validates both our inductor optimization and the technological process control.

1) Inductors above 50W LDMOS transistor

After validation, these inductors are applied above a low resistivity (8 mΩ.cm) power LDMOS silicon substrate. The inductor's ribbons are 110 µm wide and 40 µm thick. For their integration, two layers of SU8 with total thickness of 85 µm are deposited. The first layer is covering the entire wafer and integrates via openings, whereas the second one is located underneath each inductor (Figure 7). This design uses a pillar/hollow combination to demonstrate the effectiveness of the process. Figure 7 shows the excellent transition between all levels and the good filling of the vias.

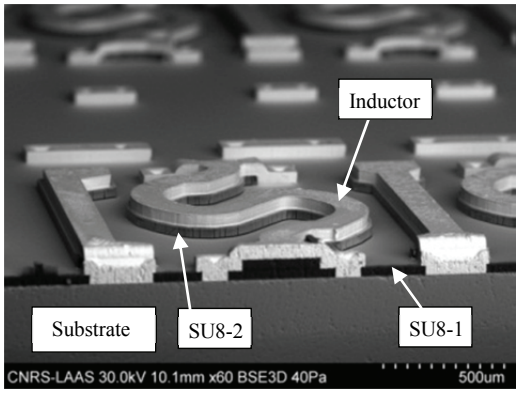

Figure 7. SEM micrograph 3D interconnected inductors integrated above a 50 W LDMOS transistor

2) Solenoid inductor

For further illustration of the new process capabilities, we integrated 3D solenoid inductors using only two lithography masks and a single electroplating step. These inductors are implemented using 90 µm thick SU8 pillars for realization of the upper parts of the ribbon. After copper electroplating, SU8 is removed.

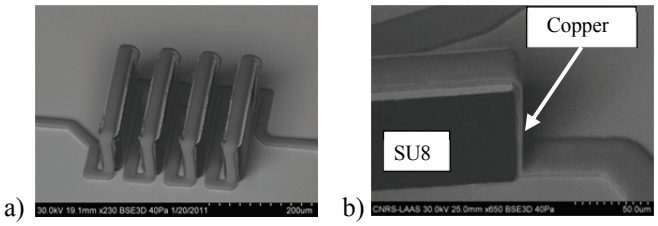

Figure 8. SEM micrographs of a 3D inductor fabricated using the new process

Figure 8.a shows an overall view of the integrated 3D solenoid inductor. Figure 8.b gives detail where the vertical copper transition from the substrate to the SU8 must be pointed out. On this example, the copper thickness is only 8 µm. One can also notice the excellent homogeneity of the ribbon's thickness on all surfaces and sidewalls.

III. CONCLUSION

An efficient and low cost above-IC process for the realization of 3D interconnected inductors using a single copper electroplating step is proposed. This process relies on three main developments: patterning of the SU8 based dielectric at specific locations, 3D deposit of a void free and homogenous seed layer thickness for 3D copper electroplating on all surfaces and sidewalls, and finally formation of thick molds using the BPN resist for keeping a good ribbon resolution. Inductors with vertical interconnections have been integrated on an 85 µm thick SU8 dielectric layer deposited on a very low resistivity silicon substrate. An excellent electroforming of the 3D copper ribbons has been demonstrated, and inductor measurements show a Q of 55 at 5 GHz. Furthermore, capabilities of the new process are fully applied for 3D integration of solenoid inductors using only two masks and a single metallic step. Finally, this technology appears of strong interest for passive device manufacturing since it can fit a large range of applications, like on chip antenna integration, packaging, baluns/transformers... and since it is fully compatible with standard IC process.

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