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Dry plasma processing for industrial crystalline silicon solar cell production

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Abstract:

This paper gives an overview on the standard crystalline silicon solar cell manufacturing processes typically applied in industry. Main focus has been put on plasma processes which can replace existing, mainly wet chemical processes within the standard process flow. Finally, additional plasma processes are presented which are suited for higher-efficient solar cells, i.e. for the "passivated emitter and rear cell" concept (PERC) or the "heterojunction with intrinsic thin layer" approach (HIT). Plasma processes for the deposition of thin dielectric or semiconducting layers for surface passivation, emitter deposition or anti-reflective coating purposes are presented. Plasma etching processes for the removal of phosphorus silicate glass or parasitic emitters, for wafer cleaning and masked and mask-free surface texturisation are discussed.

1 Introduction

Photovoltaics (PV) supply a steadily increasing amount of primary energy. The world-wide PV market is growing each year. Further information on this topic can be found in the study "Solar Generation V" [2], i.e.. Fig. 1 shows the PV market increase within the last years.

A few different studies are trying to predict the primary energy supply situation in the future. One is the well-known study of the "Wissenschaftlicher Beirat der Bundesregierung Global Umweltveränderungen" (WBGU) [3], a board of scientists asked by the German government to provide this study. Here, it is forecasted that solar energy (PV and solar thermal) will play a major role in 2050 and an even more pronounced role in 2100 (see Fig. 2). Of course, this is quite a large time frame and there are lots of unknowns in the calculations. However, reality shows that the production increase of the PV industry and at the same time the incline of the PV market in the last years have topped the assumptions made in 2003 when the WBGU study was finalised and published. A further increase of the PV market can be expected as the need for low-CO₂ electricity, a lack of fossil resources, pollution, increasing support by governments around the world and nevertheless an increasing demand for electrical energy are all facing in this direction.

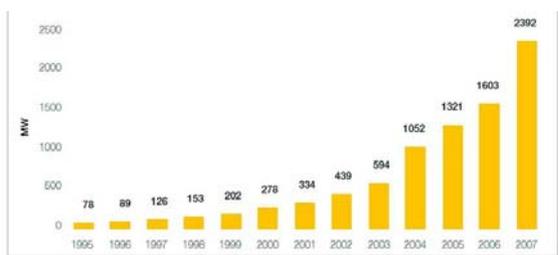


Fig. 1: Global annual PV market [2].

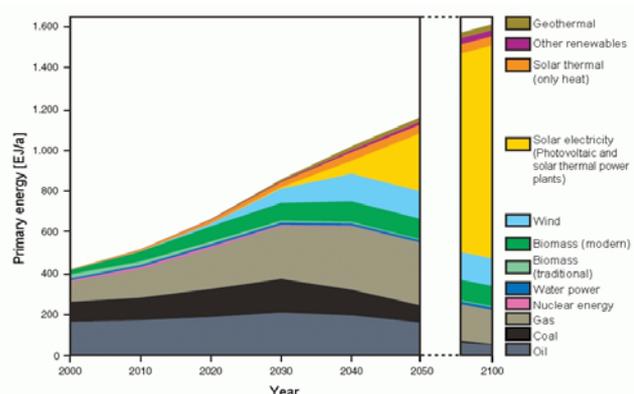


Fig. 2: Forecast of the primary energy sources [3].

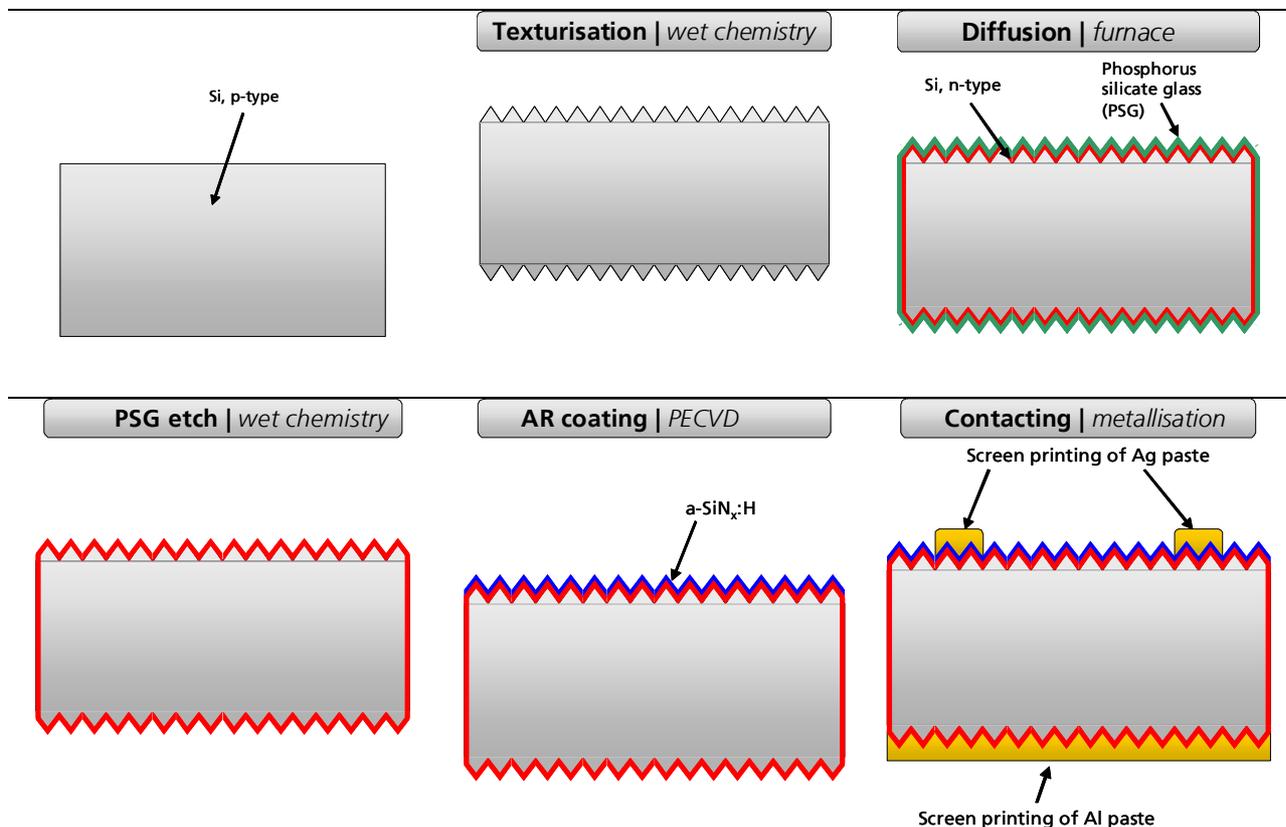
Crystalline silicon solar cell technology is a major work horse of the PV industry and takes up by far the largest share of the PV market. In the following sections, an overview will be given on a typical industrial crystalline silicon solar cell production process, typical plasma process applications as well as on plasma processes potentially replacing existing processes or being added to the process sequence. Two general targets are focussed on: the increase of energy conversion efficiency (sun light → electrical power) and the reduction of production cost.

2 Standard industrial crystalline silicon solar cell production process

The typical industrial crystalline silicon solar cell production process is based on crystalline silicon wafers (either mono (CZ) or multicrystalline (mc) silicon). In the standard case, boron pre-doped wafers are used (p-type). Since these wafers were produced by an abrasive process out of silicon blocks, the crystal damage at the wafer surface that is due to the interaction of the abrasive with the silicon surface has to be removed at first. At the same time, the wafer surface is roughened, receiving a so-called "texture". See Fig. 3 for sketches of the process sequence.

Next, the pn junction is formed by introducing the wafers into a furnace in which POCl_3 forms a phosphorus containing glass layer (phosphorus silicate glass, PSG) as dopant source (batch process) or diluted phosphoric acid is deposited within inline deposition systems. Emitter formation takes place within the same furnace for batch processes or within inline diffusion furnaces at roughly 800-900 °C. From this PSG phosphorus is diffusing into the underlying Si surfaces of the wafer. This PSG layer is removed wet chemically in a lowly concentrated hydrofluoric acid (HF) solution. An anti-reflection coating (ARC) is deposited to the front surface of the wafer. Typically, plasma-enhanced chemical vapour deposition (PECVD) is used to form a hydrogenated amorphous silicon nitride ($\text{a-SiN}_x\text{:H}$) layer with a refractive index real part $n_{632\text{ nm}}=2.1$ at a wavelength of 632 nm and a physical thickness of around 70 nm. The deposition process will be discussed further below. The contact formation on front and rear surface is performed by screen-printing an Al-containing paste on the full rear, except small areas where an Ag and Al containing paste is printed for solar cell interconnection pads. On the front, a Ag containing paste is printed in a H-pattern-like grid structure. Subsequently, the wafers are subjected to a so-called firing process applying a temperature ramp with a peak wafer temperature of around 800 °C. During this firing process, the front paste etches through the $\text{a-SiN}_x\text{:H}$ layer to form an ohmic contact to the underlying n-type silicon emitter. At the rear, Al is alloyed into Si. Additionally, Al is diffusing into the Si. This overcompensates the phosphorus of the n^+ layer at the rear surface, leading to an inversion of n^+ to p^+ and forming a so-called aluminium back-surface field (Al-BSF). Additionally, a good ohmic large-area contact is created at the rear. In case of using laser techniques, isolation of p- and n-type areas at the wafer edge is carried out forming a narrow trench around the wafers front side near the edges.

Surface cleaning, drying, annealing or handling steps were neglected in this description. A good discussion of the industrially applied processes can for instance be found in [4].



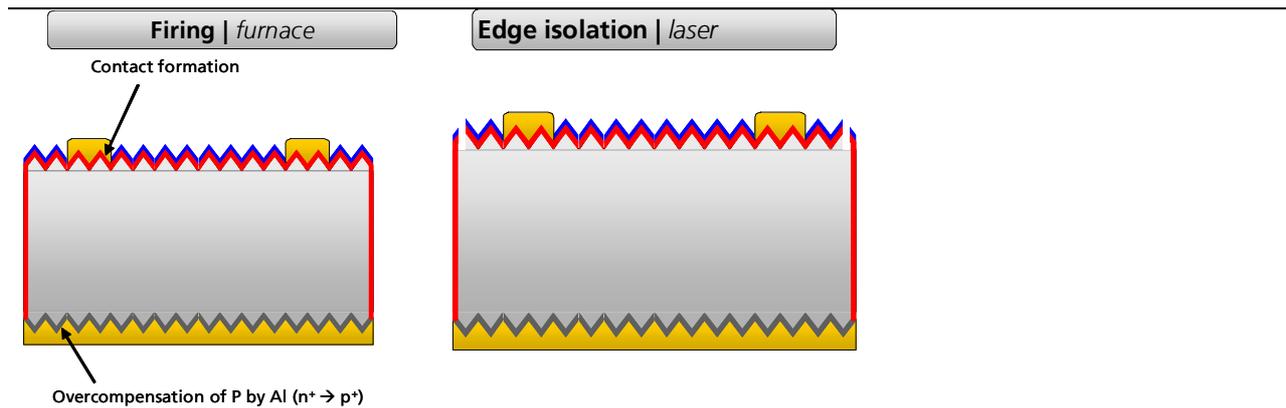


Fig. 3: Process sequence of a standard industrial crystalline silicon solar cell manufacturing line.

The only plasma process involved in the typical industrial crystalline silicon solar cell production process is therefore the deposition of the ARC. This is typically performed by PECVD. One means to perform the deposition is the application of a microwave (MW) plasma by using a linear antenna in an equipment that allows for the inline transport of the substrates through the deposition zone. This concept enables for a high throughput in industrial production. The linear antenna concept is outlined in Fig. 4. The linear antenna (copper) is fixed across a vacuum chamber. A microwave generator feeds both sides of the antenna. When process gas is introduced into the chamber, the MW penetration will lead to a strong increase of the gas dissociation and, subsequently, to a reaction of gas particles with the substrate surface. A layer deposition or a substrate etching are the consequence. The substrates are held by carriers which are moving constantly through the plasma zone of the reactor.

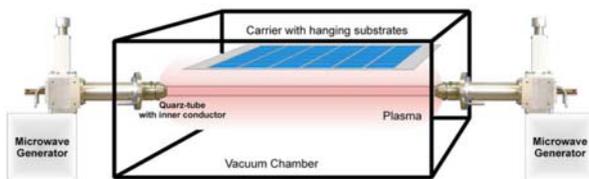


Fig. 4: Basic setup of an inline MW PECVD system with hanging substrates [5].

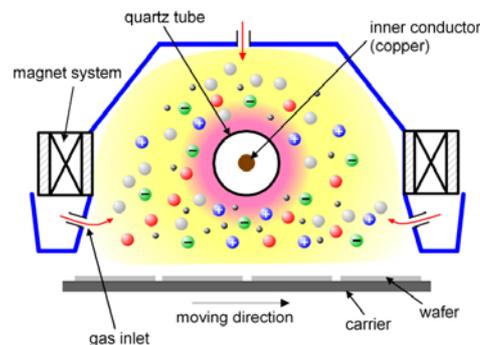


Fig. 5: Sketch of the working principle of a MW linear antenna plasma with moving substrates [1].

Fig. 5 shows a cross section of the antenna, plasma zone and carrier with substrates. Here, the substrates are passing through the plasma zone underneath the antenna. It is also possible to move above the antenna as shown in Fig. 4. The throughput of a MW inline PECVD tool can be increased by placing several MW linear antennas in series. For such PECVD processes typical process gases are monosilane (SiH_4) and ammonia (NH_3). The targeted anti-reflection coating typically has a refractive index of $n_{632\text{nm}} \approx 2.1$ at a light wavelength of 632 nm as outlined above. The absorption (extinction coefficient) should be as low as possible. The typical ARC thickness is ≈ 70 nm. Such ARC can also be deposited by the alternative techniques of rf sputtering [6, 7], low pressure chemical vapour deposition (LPCVD) or expanding thermal plasma (ETP) [8]. Also PECVD offers different options like direct or remote configurations.

3 Plasma processes for replacement of standard processes

Plasma processes can replace process steps currently applying wet chemical technology. An overview on such replacements will be given in the following sections.

Plasma technology offers several potential benefits compared to wet processing. Single-sided processing of the wafers is possible, no principal limitations concerning the wafer thickness occur, an in-line design of the plasma tools is possible/ already industrially available and only a small amount of (DI) water is needed. Hence, the application of plasma processes seems beneficial for very thin high-efficiency silicon solar cells.

3.1 Surface texturisation

Increased collection of photons can be achieved by a texturisation of the silicon wafer surface. This surface roughening increases the probability for reflected photons to hit the silicon surface a second time. Plasma process technology has brought up two different approaches, masked and mask-free, which will be sketched in the following.

3.1.1. Mask-free texturisation

Mask-free texturisation of silicon surfaces is possible by means of a sulfur hexafluoride (SF_6) + oxygen (O_2) gas mixture. It was shown that the application of the same inline MW linear antenna plasma tool as used for the deposition of $\text{a-SiN}_x\text{:H}$ can also be used for surface texturisation [1]. The application of such a plasma texturisation process leads to a dramatic decrease of the reflection properties. See Fig. 6.

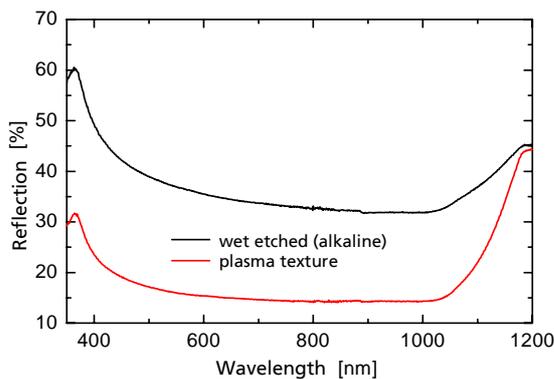


Fig. 6: Reflection values of alkaline etched and of a plasma textured mc wafer [1].

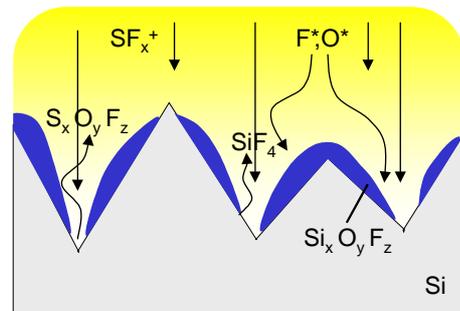


Fig. 7: Mask-free texturisation principle of in-situ micromasking [9].

This result was obtained by a gas ratio SF_6/O_2 of 3:1. The effect of a change in this gas ratio is presented in Fig. 8. Here, the oxygen content was varied from 5% (Fig. 8 a)) to 40% (Fig. 8 c)). The surface topography is changing from rather big crater-like structures (Fig. 8 a)) to small structures and an enhanced surface roughening (Fig. 8 c)).

The mask-free texturisation process is based on a micro-masking inherent to the substrate and plasma-process conditions as sketched in Fig. 7. $\text{Si}_x\text{O}_y\text{F}_z$ or $\text{S}_x\text{O}_y\text{F}_z$ compound layers are formed locally at the Si surface. The formation of these local adsorbate layers is the result of a simultaneous influence of an isotropic chemical and a directed physical etching component and is only present for certain combinations of process pressure, substrate temperature and, mainly, energy distribution of the incoming ions. If the ion energy is too high, the thickness of the adsorbate layers is lower or a formation of such adsorbate layers is prevented. If the local adsorbate layers are present, the Si etch rate will vary locally depending on the adsorbate thickness [1, 9]. As a matter of fact, the specific etching process leaves adsorbate films at the Si surface also after the etching process. These adsorbates have to be removed prior to the deposition of an ARC to allow for best electrical surface passivation. It was shown that excellent surface passivation is achievable when the adsorbates are removed [1]. This shows additionally that the potential Si crystal damage which might occur due to the plasma texturisation process is quite low.

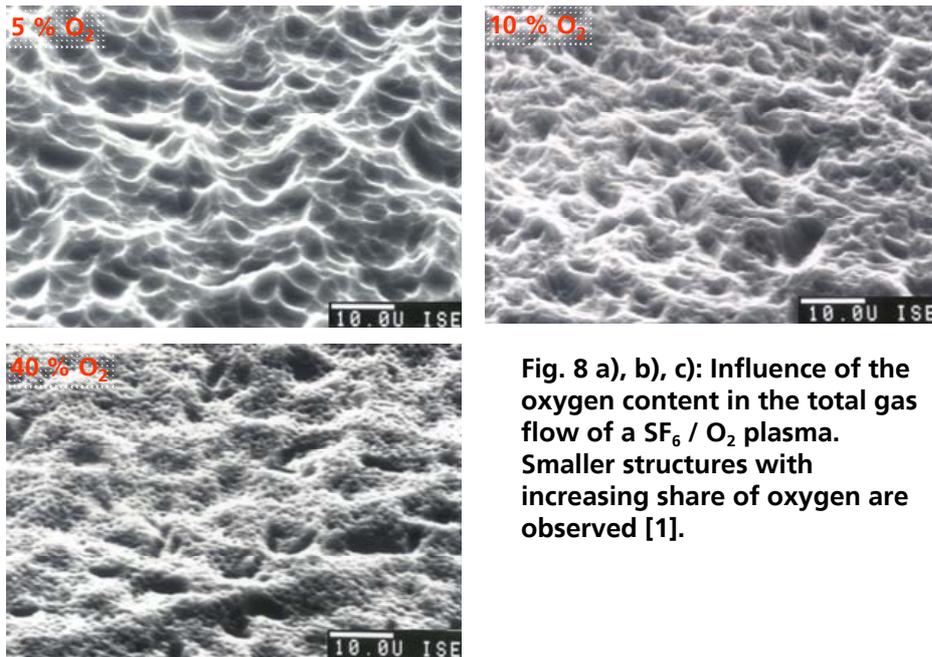


Fig. 8 a), b), c): Influence of the oxygen content in the total gas flow of a SF_6 / O_2 plasma. Smaller structures with increasing share of oxygen are observed [1].

A wet chemical alkaline anisotropically etching solution leads to the pyramidal surface topography as shown in the scanning electron microscopy images presented in Fig. 9 if applied to (100) oriented Si surfaces. (111) oriented Si crystal planes remain at the surface forming the pyramids. When such a surface is additionally treated with a specific texturing plasma process a micro-roughness is formed at the planes leading to an increased light trapping (Fig. 10). Hence, the reflection is decreased even further. On the other hand, for an optimum surface passivation, the surface should be as flat as possible. Hence, a trade off between the optical and electrical (recombination) properties has to be found for an optimum solar cell.

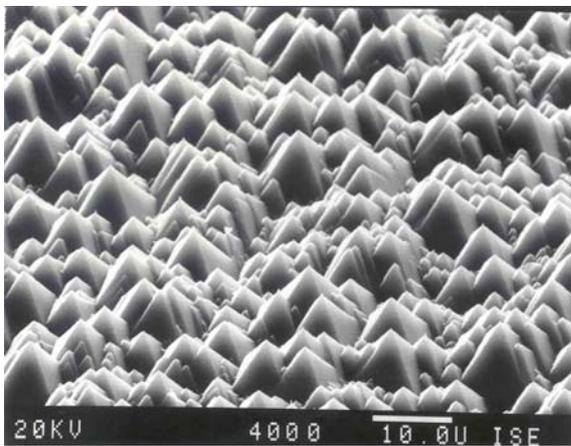


Fig. 9: Surface of a (100)-oriented monocrystalline Si wafer after anisotropic wet chemical etching leaving (111) planes.

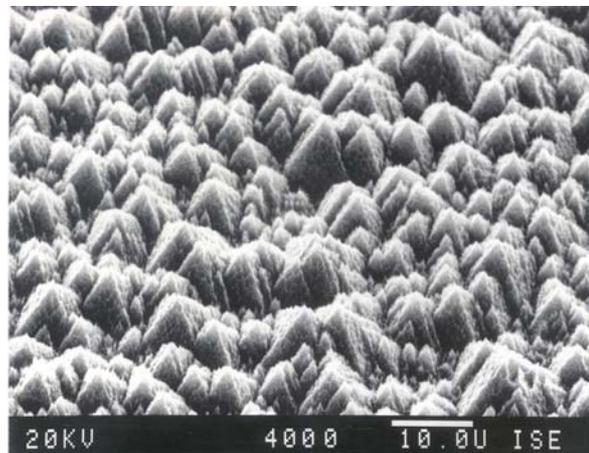


Fig. 10: Surface of the same type as in Fig. 9 (wet textured) with additional plasma microtexture.

3.1.2. Masked texturisation

Besides the mask-free processes described above it is also possible to apply a plasma etching process to a Si surface which is locally masked. The masking can be done by photolithography. A mask as outlined in Fig. 11 was used by O. Schultz [10].

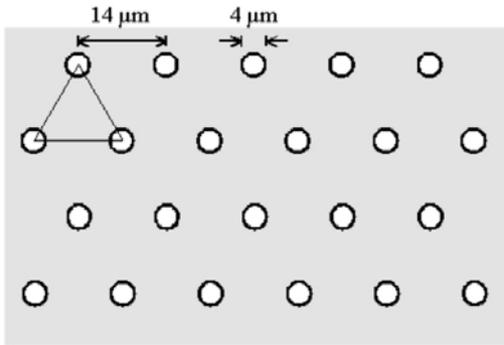


Fig. 11: Sketch of the photolithography mask with 4 μm wide openings for masked plasma texturisation [10].

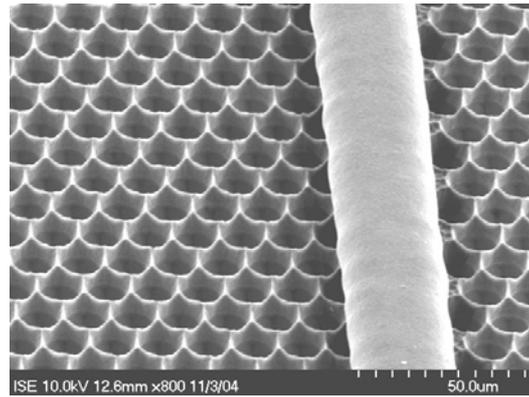


Fig. 12: Scanning electron microscope image of the surface of a multicrystalline wafer with a honeycomb texture and a contact finger [10].

After applying the mask, a plasma etching was performed in a single-wafer reactor applying a reactive ion etching (RIE) plasma with a gas mixture of SF_6 and O_2 . After removing the mask, a so-called honeycomb structure was created. The process sequence is sketched in Fig. 13. Schultz discusses also the optimum process parameters which lead to the optimum texturisation process as shown in Fig. 12. Using such a front surface texturisation process it was possible to manufacture the most efficient solar cell applying a multicrystalline (mc) Si substrate [10].

A great advantage of a plasma texturisation process (masked or mask-free) is its independence of the crystal orientation of the substrate. Hence, also low-cost mc Si wafers can be effectively textured. Fig. 12 shows the result of the masked etching process for a mc Si solar cell. For industrial application, the preparation has to be transferred to a low-cost solution.

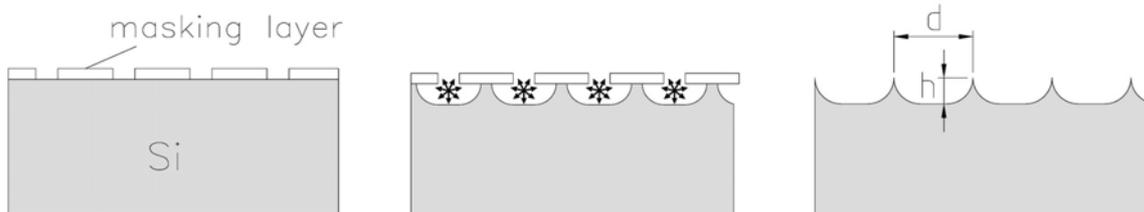


Fig. 13: Process sequence (from left to right) for masked plasma texturisation: (i) application of the masking layer, (ii) plasma etching in the local areas without mask, (iii) removal of the mask [10].

3.2 Surface cleaning

The removal of residuals from a crystalline Si wafer surface is an important process needed typically i.e. before the deposition of thin layers. This surface cleaning process can be done by means of Si removal by etching with fluorine containing gases like SF_6 . The etching of Si surfaces by an MW plasma with solely SF_6 as precursor gas applying the above mentioned linear antenna inline industrial-type plasma tool with the subsequential deposition of a hydrogenated amorphous silicon (a-Si:H) passivation layer within the same vacuum has lead to excellent surface passivation in the range of 700 μs at a minority carrier density $\Delta n = 5 \times 10^{14} \text{ cm}^{-3}$ using substrates of p-type float-zone silicon (shiny etched surfaces, (100) oriented, 250 μm thick, Boron doped, 1 Ω cm) [11, 12]. The physical limit of the minority carrier lifetime of such a crystalline silicon wafer is at ~2300 μs assuming only Auger recombination taking place (neglecting radiative recombination and Shockley-Read-Hall recombination, neither in the bulk nor at the surfaces), applying the Auger recombination model of Glunz et al. [13]. Hence, one can calculate the effective surface recombination velocity S_{eff} via [14]

$$\frac{1}{\tau_{\text{eff}}} = \frac{1}{\tau_b} + \left(\frac{W}{2S_{\text{eff}}} + \frac{1}{D_n} \left(\frac{W}{\pi} \right)^2 \right)^{-1} \quad (3.1)$$

with the measured effective minority carrier lifetime τ_{eff} , the minority carrier lifetime in the bulk τ_{bulk} , the wafer thickness W and the electron diffusion coefficient D_n . The surface passivation level of $S_{\text{eff}} \approx 13 \text{ cm/s}$ would allow for excellent solar cell efficiencies. Applying a plasma etching process as presented here is also providing an excellent means to remove a parasitic rear emitter.

3.3 PSG removal

In the standard solar cell production sequence, the phosphorus silicate glass (PSG) which is formed during the phosphorus diffusion at the Si surface is removed by diluted hydrofluoric acid (HF). This process can also be replaced by a plasma etching process. It was shown that the application of a low-frequency plasma source built into an inline industrial-type plasma tool is capable to provide a means to selectively etch PSG [1, 15]. A selectivity of >10 (etch rate of PSG / etch rate of Si) was achieved by a process gas mixture of CF_4 and H_2 . See Fig. 14.

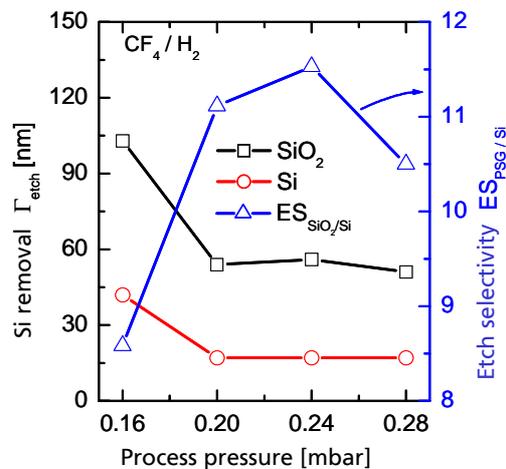


Fig. 14: Si removal and etch selectivity (PSG/Si) for the selective LF plasma etching process [1].

The PSG layer can be described as a doped SiO_2 layer. For the fast plasma etching of SiO_2 typically high ion energies are necessary since it is chemically relatively stable. To allow for a selective process, the creation of a selective polymeric protection layer is pronounced. This polymer layer (CH_x) builds up mainly on top of the Si surface. The oxygen out of the PSG layer reacts with the CH_x to form CO_x and HO_x and hence prevents the formation of the polymer layer at the surface. The etching of the Si surface is thus mainly limited by the diffusion of F_x through the polymer layer. Highly energetic ions are physically etching the PSG layer at the same time [1, 16-18].

The incorporation of a PSG plasma etching process in a crystalline silicon solar cell production line is of highest interest when a combination of a sequence of plasma processes can be combined to a cluster tool as described in section 4.4. Thus, such a plasma etching process can be included at relatively low cost.

4 Additional plasma processes

Solar cell structures that allow for higher energy conversion efficiencies than the industrial standard can benefit from additional plasma processes. A solar cell structure for which the industrialisation is currently ongoing is the "passivated emitter and rear cell" (PERC) concept [19, 20]. The cell structure is sketched in Fig. 15 and shows in principal the same front design as the industrial standard but a few differences at the rear. Here, a passivation layer which takes up more than 90% of the rear surface is applied. The passivation layer typically provides only a very low conductivity. Periodic local rear contacts are formed for current transport.

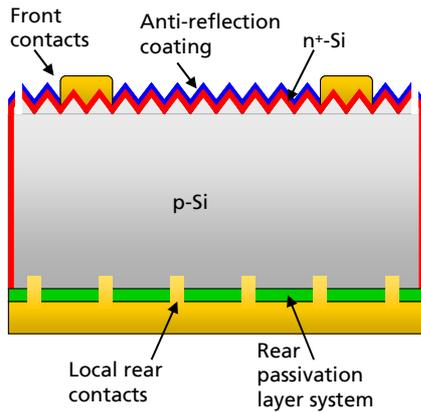


Fig. 15: Scheme of a PERC-type solar cell.

4.1 Rear passivation layers

Thin layers that allow for an efficient electrical passivation of crystalline silicon surfaces (reduction of recombination rate of electrons and holes) make use of two main physical principles. First, the reduction of the density of states D_{it} at the interface c-Si / passivation layer leads to a lower probability of electron-hole recombination. The second principle is the lowering of the concentration of one kind of charge carrier at the c-Si surface. This can be achieved by the incorporation of fixed charges in the passivation layer which leads to a band bending at the c-Si surface. More details can for instance be found in the work of A. Aberle [21]. Best passivation can be expected for layers that allow for a very low D_{it} and a strong band bending at the c-Si surface. Since the typical passivation layers are isolators or at least show only low conductivity, a periodic local contact formation at the solar cell's rear surface is required, leading to the PERC structure. A discussion on the impact of the rear surface passivation quality on the solar cell efficiency is for example presented in [22] and [23].

Passivation layers for the rear surface can be prepared by means of thermal oxidation [21]. This approach can be called highly efficient combined with typically high cost and rather low throughput. In comparison, the deposition of thin layers by means of PECVD would be beneficial. Thin layers which are currently under investigation are amorphous hydrogenated silicon nitride ($a\text{-SiN}_x\text{:H}$) [24-33], amorphous hydrogenated silicon oxide ($a\text{-SiO}_x\text{:H}$) [23, 34, 35], amorphous hydrogenated silicon carbide ($a\text{-SiC}_x\text{:H}$) [36-40], hydrogenated amorphous silicon ($a\text{-Si}_x\text{:H}$) [41-44], aluminium oxide (AlO_x) [45-50] and stacks of these layers. Two examples will briefly be presented here:

A stack of $a\text{-Si:H}$ + $a\text{-SiO}_x\text{:H}$ in combination with local laser-fired contacts (LFC) at the rear lead to energy conversion efficiencies of up to 21.7% of PERC-type solar cells [51, 52]. Internal quantum efficiency (IQE) measurements showed that the passivation at the rear surface is stable up to a post-process annealing temperature of 400°C. At 450°C the passivation quality strongly deteriorates. See Fig. 16. The short wavelength regime shows the passivation at the front surface, the long wavelength part shows the bulk and rear passivation quality. Since excellent bulk material was used, differences in IQE at long wavelengths are due to variations of the rear passivation.

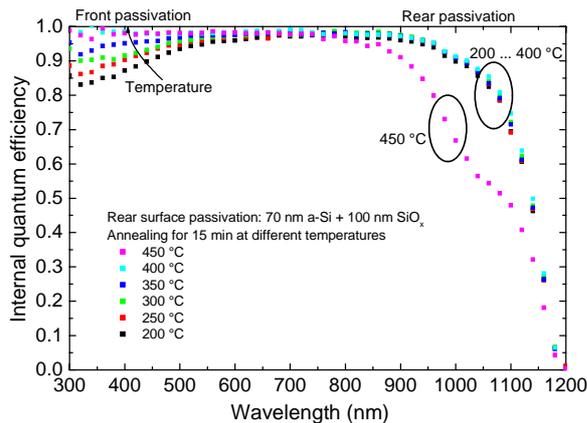


Fig. 16: Internal quantum efficiencies of PERC-type solar cells with a-Si:H + a-SiO_x:H rear passivation and laser-fired rear contacts [52].

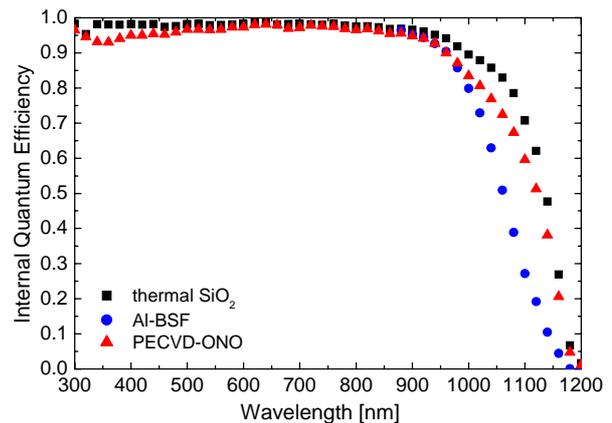


Fig. 17: Internal quantum efficiencies of PERC-type solar cells with a rear passivation stack of a-SiO_x:H + a-SiN_x:H + a-SiO_x:H (in short: ONO) in comparison to thermal SiO₂ and Al-BSF [23].

Since the passivation at the rear when a-Si:H is applied was found to be excellent but not stable for temperatures above 400°C for long processes and it additionally was found that also short high-temperature steps like a contact firing process would harm the passivation effect strongly, an alternative approach for high-temperature processes is needed. A solution was found by the stacking of PECVD a-SiO_x:H + a-SiN_x:H [23, 34, 53]. This stack system was shown to be able to provide good surface passivation after a typical firing of screen-printed contacts of industrial-type crystalline silicon solar cells. An additional a-SiO_x:H layer showed additional benefits, leading to a SiO_x/SiN_x/SiO_x (ONO) stack. The IQE in the long wavelength regime exhibits a lower performance of the ONO stack compared to the high-end reference thermal SiO₂ but a significant improvement to the industry standard Al-BSF. See Fig. 17.

4.2 Front passivation layers

Also the passivation of the front of solar cells is a current research topic. Three main characteristics should be fulfilled to achieve an optimum front passivation:

1. A refractive index of 2.1 at a wavelength of 632 nm suits the refractive index surrounding of the solar cell within a module including a glass front encapsulation.
2. The absorption should be as low as possible (best: none).
3. The silicon surface passivation should be as effective as possible.

For front passivation all layer types and stacks presented in the previous chapter are possible as well. Two examples will be discussed shortly here: Plagwitz [54] has shown that a stack of a-Si:H and a-SiN_x:H is able to passivate effectively the surface of a p-type emitter at the front surface of a solar cell. The main idea is that the surface passivation will be provided by the a-Si:H and the optics will be provided by the a-SiN_x:H. Fig. 18 shows that the emitter saturation current (75 Ω/sq. emitter) is lowered for a-Si:H layers of a thickness of 5 nm or more. Since a-Si:H layers are absorbing light it is beneficial to deposit a-Si:H layers as thin as possible. Plagwitz showed that an a-Si:H layer of 5 to 10 nm is a good compromise which allows good surface passivation and low absorption at the same time.

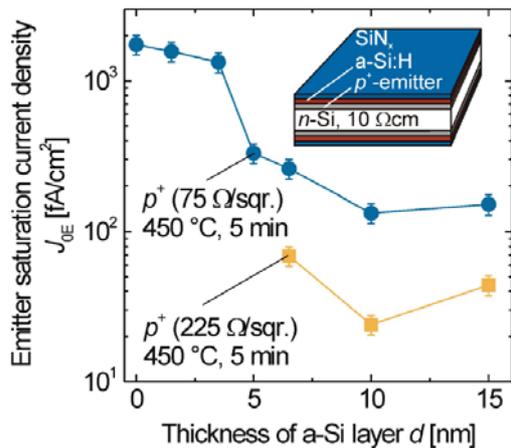


Fig. 18: Emitter saturation current of a p^+ emitter passivated with a-Si:H of different thickness [54].

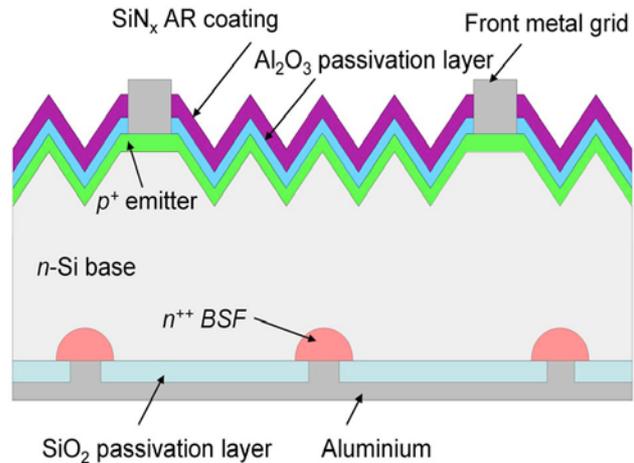


Fig. 19: Scheme of the solar cell as presented by Benick et al. [55]. A thin Al_2O_3 layer provides the front surface passivation of the p^+ emitter.

Another example was presented by Benick et al. [55]. Plasma-assisted atomic layer deposited (PA-ALD) thin aluminium oxide (Al_2O_3) was applied to a p-type emitter at the front of a solar cell to provide the surface passivation. The anti-reflection properties in this case were supplied by a $a-SiN_x:H$ layer on top of the Al_2O_3 . See Fig. 19. Energy conversion efficiencies of up to 23.2% were achieved.

4.3 Deposited phosphorus sources

Besides the formation of n-type emitters in a furnace applying a $POCl_3$ containing atmosphere, it was presented by Benick et al. [56] that it is possible to deposit a phosphorus-containing silicon oxide layer by PECVD which can provide phosphorus to diffuse into the silicon surface when a high-temperature process is applied subsequently. The results were at the same performance level as the standard $POCl_3$ references. An advantage is that the deposition can be provided in a single-sided way. This would allow for an easier fabrication of PERC-type solar cells because the rear emitter does not have to be removed (since it was not formed). The deposition of the phosphorus-doped silicon oxide layer was performed using a gas mixture of tetramethylcyclotetrasiloxane (ZTMCTS), trimethyl phosphite (TMPI) and oxygen (O_2). During the mentioned high-temperature process the rear surface of the wafer can be treated differently than the front. For example, a thermal oxidation of the rear surface can be achieved at the same time.

4.4 Plasma cluster tools

If more than one plasma process is present within a solar cell manufacturing process line, it makes sense from a cost and energy-consumption point of view to cluster the plasma processes. This leads to a big plasma tool with one entering and one exiting load lock and vacuum processes in between. The preparation of a prototype system was presented implementing many different plasma processes which represent a main part for producing a PERC-type structure in an industrial way [57]. The processes included are the rear emitter removal by a SF_6 MW plasma, the removal of the PSG on the front, surface cleaning on front and rear and the deposition of a front ARC and a rear passivation stack of $a-SiO_x:H$ and $a-SiN_x:H$. The system is an inline tool with the same basic characteristics as the MW linear antenna PECVD tool used for the $a-SiN_x:H$ deposition described above. Fig. 20 shows a sketch of the system and the included main processes. It was calculated that the manufacturing cost of a crystalline silicon solar cell would be slightly lower than the current industrial standard [57].

The plasma cluster system can be designed in such a way that the industrial production throughput requirements are met. Inline plasma processing allows for the processing of only one side of the substrate. No principal limitations for the processing of very thin wafers ($<100 \mu m$) apply. Thus, plasma cluster processing becomes increasingly interesting for new highly efficient low-cost solar cells on thin substrates.

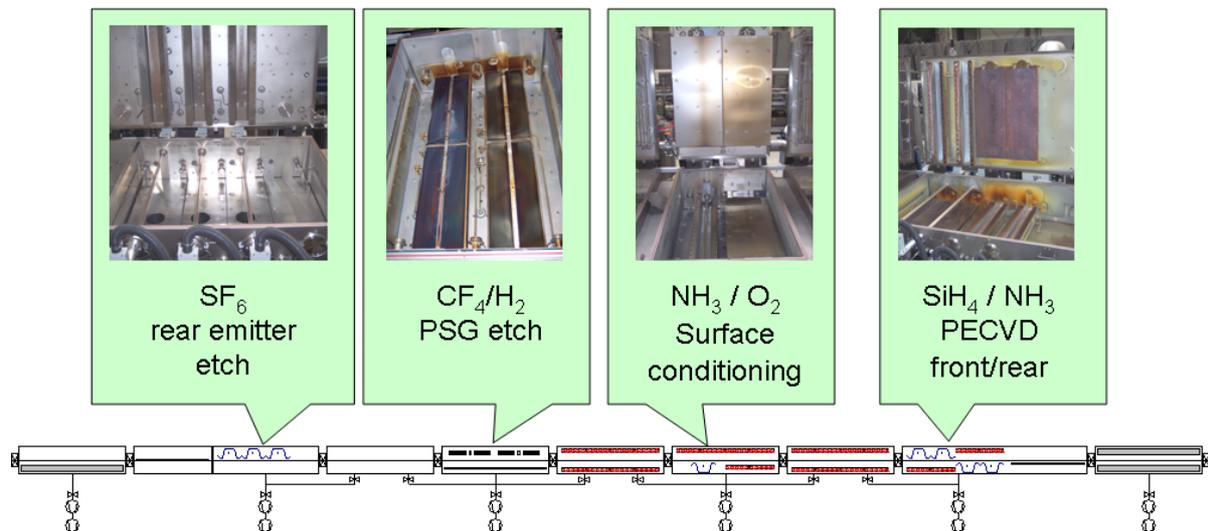


Fig. 20: Prototype of an industrial-type plasma cluster tool allowing for plasma etching and deposition processes within one vacuum [57].

4.5 Deposited emitters

Knowing that a-Si:H layers are able to provide excellent surface passivation qualities and also knowing about the possibility to dope a-Si:H layers it seems possible to deposit an a-Si:H p-type emitter on a n-type c-Si substrate providing a heterojunction. Sanyo Electric [58] has shown that such an approach applying additional a-Si:H layers to front and rear c-Si surface for surface passivation and an additional n⁺-a-Si:H layer to the rear can lead to efficiencies of up to 23.0% as recently communicated by a press release of Sanyo. This approach is of course in need of a totally different process workflow compared to standard industrial wafer-based crystalline silicon cell technology.

5 Conclusion

Although there is only one plasma process typically included in the industrial fabrication of crystalline silicon solar cells, it was shown that a variety of other plasma processes are available to replace existing standard processes. Aiming more efficient solar cell structures, more complex process sequences have to be addressed and more plasma processes can be introduced to the production workflow. Such dry processes offer several potential benefits compared to wet processing. Single-sided processing of the wafers is possible, no principal limitations concerning the wafer thickness occur, an in-line design of the plasma tools is possible/ already industrially available and only a small amount of (DI) water is needed. Plasma processes should be clustered in a production line to allow for lowest cost and energy consumption.

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