Stress mapping in strain-engineered silicon p-type MOSFET device: A comparison between process simulation and experiments

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Stress mapping in strain-engineered silicon pMOSFET device using process simulation

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Strain engineering is the main technological booster used by semiconductor companies for the 65 and 45nm technology nodes to improve the channel mobility and the electrical performance of logic devices. For 32 and 22nm nodes, intense research work focuses on the integration and optimisation of these different techniques by cumulating the effects of different stressors. To estimate the level and the distribution of the stress field generated in the transistor channel by such multiple processing steps is a complex issue. Process simulation has a role to play in order to face the many challenges in term of scalability, yield and design. The objective of this paper is first to evaluate the stress distribution generated by the two most usual processing steps: Contact Etch Stop Liner (CESL) and embedded SiGe Stressors (eSiGe). Next, the final stress field in nanoscale device resulting of these intentionally but also parasitic sources are evaluated. Process simulations have been able to quantify the global trend observed in these stressors in relatively close correlation with experiment.

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I. INTRODUCTION

For CMOS devices downscaling, sharp requirements have been defined by the International Technology Roadmap for Semiconductors (ITRS) in terms of drive current, off state current, power density, making the geometric scaling a challenging task[3]. The new vector adopted to extend the Moore's law is the channel mobility enhancement through the introduction of stress in the channel[4]. Different method of stress engineering have been introduced to boost the electrical performance of the logic devices. Intense research work has been devoted in the last decade to increase the channel mobility by biaxial layer but it has been observed to be difficult to implement for technical and cost issues. Local mechanical stress control[5] and uniaxial stress are on the fundamental point of view more favourable on the band structure engineering and the resulting mobility enhancement[6] and easier to implement on the technological point of view[7].

Several technological stress-transfer techniques have been developed in order to introduce such uniaxial stress in the channel device. First, embedded SiGe stressors (eSiGe) in the source/drain regions have been proposed to induce a compressive stress in the pMOS channel[8–12]. The filling of the source/drain by a SiGe material with a lattice spacing larger than silicon leads to a large compressive stress in the channel and drive current improvement[13]. Next, an another technique is the deposition of a stress material on top of the gate stack after silicide formation. If one single liner is used, the electrical performance of the opposite type of device will be degraded. With the possibility to engineer compressive or tensile stress depending on the process conditions with nitride film[14], successful integration of dual Contact Etch Stop Liner (CESL) have been reported[15]. Uniaxial strain boosters have been widely adopted in order to increase the performance of logic device for the 90nm[8] down to 45nm technology nodes[16]. Some studies focuses on the optimisation of these different techniques in order to enhance the stress level generated and also on the integration with the main aim to cumulate the effect of different stressor[12]. Research activities are also dedicated to enhance the stress level generated by these different uniaxial stress techniques. Despite these large technological progress, many challenges are faced by the uniaxial stress engineering approach for 32nm technology nodes and below in terms of scalability since the stress coupling effect between the gate pitch and the various stressors like eSiGe and CESL is expected to be smaller for decreasing nodes[17]. Next the yield is also concerned with the

integration of multiple sources of local and global stress in such a way that the channel mobility is enhanced without exceeding the local critical shear where defects appears. Finally, circuit design is also pitch-and layout-dependent effects must be taken into account as the device geometries shrink and strain distribution should be investigated on a larger scale.

Therefore, intense research work have been dedicated the last few years to develop or improve ex-situ or in-situ characterisation techniques in order to quantify the strain introduced in nanoelectronics device. MicroRaman Spectroscopy (μ-RS)[18] and Coherent Beam Electron Diffraction (CBED)[19] analysis are the most often usual characterisation technique[20]. However with these two techniques, the stress field can only be investigated in a few points of the structure. Significant progress have been achieved with the development of the Geometric Phase Analysis (GPA) technique[21] which enable a more complete two dimensional mapping of strain field component in silicon crystalline on relatively large scale $\sim \mu m$ with a resolution of a few nanometers. On the other side, a direct confrontation between CBED and GPA analysis using High-Angle Annular-Dark-Field Scanning Transmission Electron Microscopy (HAADF STEM) shows that the difference in absolute strain measured could exceed 300 MPa[22]. In the present case, the difficulty to define a strain reference relative to the unstress level is probably the main source of discrepancy. An other study also stress the influence of sampling preparations in stress evaluation[23]. Even if these remarkable experimental achievements clearly improve the understanding on how stress is generated and distributed in the silicon channel of the nanodevice, some limitations are faced.

In order to address these challenges associated to downscaling, process simulation and TCAD tools have probably a significant and complementary role to play in order to provide guidelines for process optimisation. In comparison to dopant diffusion modelling[24], very few studies have been dedicated to the stress simulation. The modelling of the stress by TCAD tools was introduced in the 90's in order to estimate the stress generated by silicon oxidation in the case of LOCOS (LOCal Oxidation of Silicon) and next STI (Shallow Trench Isolation) fabrication. The aim was to make predictive simulations in order to provide guidelines for the stress minimisation generated by various process steps such as oxidation, nitride deposition, densification, implantation, silicidation[25,26] and also to minimize defects formation. As discussed previously, the philosophy has radically changed as stress engineering is now the principal technology booster to improve electrical device performance for logic nanodevice.

This approach impacts largely process simulation tools as it is critical to evaluate layout dependent stress variations and to take into account the influence on the design information flow[27]. Some recent research work have been undertaken for the simulation of the stress field generated by these technological booster. Different strained-silicon options have been analysed with simple stress simulations[28]. The amount of stress generated in the channel by eSiGe stressor has been estimated[29,30]. Eneman *et al.* also investigate the scalability of eSiGe stressor[31,32]. Stress transfer has been found to be highly dependent on downscaling and to decrease with the dimension of the active area. However, some questions remain open concerning the predictivity of these results. For example, in the case of the stress field generated by CESL, Loiko *et al.*[33] criticises the method often used for the modelling of the stress introduced by the deposition step. Orain *et al.*[34] perform a complete 3D mechanical simulation study using a pseudo-3D structure in order to investigate the complex mechanisms responsible of the stress transfer for CESL. The main objective of this work is first to investigate the stress field generated for several front-end key step and next to evaluate the stress mapping for a stress-engineered pMOSFET.

In this study, the paper is organised as follow : in the first section, the stress modelling and the rheological parameters used are briefly presented. The stress distribution for eSiGe and CESL stress booster on simple test structures are simulated and confront to available experimental characterisation. Finally, a simplified complete process flow matching as far as possible, a realistic one is performed in order to estimate the stress mapping generated in such nanoscale stress engineered MOSFET device.

II. METHODOLOGY

A. Stress modelling

Various sources of mechanical stress can be modelled using a process simulator such as i) the intrinsic stress generated by deposition step ii) the etching or material removal iii) the growth iv) the thermal stress and finally the stress generated by material structuring. All these different steps modify the stress equilibrium of the structure and the forces balance. A macroscopic modelling of the mechanical deformation associated with these process. With

the knowledge of the initial mechanical state and the modelling of the stress generated by the different step, the stress distribution σ can be estimated thanks to the following equation :

$$\{\sigma\} = [D](\{\epsilon\} - \{\epsilon_0\}) + \{\sigma_0\}$$

where $[D]$ is the elasticity matrix, $\{\epsilon\}$ is the effective strain tensor representing the various stress components in the device structure and $\{\epsilon_0\}$ (resp. σ_0) the sources of initial deformation (resp. stress).

In order to calculate the evolution of this equation during the simulation of a front-end process flow, a Finite Element (FE) based method is usually used. Bi-dimensional finite element based simulations have been perform using the Sentaurus Process simulator in the Z-2007.03 release[35]. A specific set of mechanical parameters has been used as described in the next section. All the plane strain simulations performed in this study have been done assuming free boundary conditions and an initial stress-free state for the structure.

B. Rheological parameters

A large number of materials are used in front-end processing with a large number of complex of rheological behaviour. For example, silicon is considered in all the studies as an anisotropic elastic material with Young's modulus equals to 131 GPa along [100], 169 GPa [110] and 187 GPa [111] with a thermal expansion coefficient given by the following relationship as function of the temperature T (in Kelvin) : $\alpha(\mathrm{T}) = 3.05 + 1.24 \cdot 10^{-03}\mathrm{T}$.

The deformation generated by the thermal expansion can often be described by a simple elastic rheologicial behaviour. On the other side, amorphous material like SiO_2 or Si_3N_4 exhibit a viscoelastic behaviour. A common set of mechanical parameters are used for the description of the rheological behaviour of the different materials. This database describing the rheological behaviour is the result of Brillouin Light Scattering or beam bending experiment from literature[25]. Table I summarises the various mechanical parameters used in the study.

III. RESULTS

The main objective of this section is to estimate the stress distribution generated by the two main front-end process steps : embedded SiGe stressor (eSiGe) and Contact Etch Stop Liner (CESL) separately.

A. Simulation of eSiGe stress distribution

The epitaxy of this SiGe layer is known to generate a lattice stress mismatch at the silicon interface since the lattice parameter of the $Si_{1-x}Ge_x$ alloy has a larger lattice parameter $a_{Si_{(1-x)}Ge_{(x)}} = xa_{Ge} + (1-x)a_{SiGe}$ according to Vegard's law. This biaxial strain generated can be estimated thanks to the following relation :

$$\epsilon_0 = \frac{xa_{Ge} + (1-x)a_{Si}}{a_{Si}} \tag{1}$$

as a function of the Germanium concentration x. This biaxial strain generates in reaction large forces in the silicon substrate. In order to estimate these two dimensional stress distribution, different test structures have been considered matching as far as possible several experimental study of the literature[21,36]. First, silicon pads stressed by SiGe thin layer and characterised by Microraman technique and next a comb structure by the Dark Field Holographic technique.

1. Stress distribution and Microraman characterisation

Planar structures made of $Si/SiO_2/Si_3N_4$ pads of Nouri *et al.*[36] has been simulated with surrounding trenches where a SiGe layer is deposited. Fig. 1 shows that the experimental configuration where large enough to allow Microraman characterisation and to estimate the stress level near the silicon surface. Fig 2 shows that the experimental variation of the mean lateral stress is strongly influenced by the topological parameters such as the silicon width or the etch depth on the magnitude of the compressive stress in the silicon part. Fig. 2 also provides the lateral stress distribution for this large structure of 36 μm width considering a 20% Ge concentration for the SiGe stressor. The silicon etch depth for this simulation 150nm. Standard intrinsic stress of table I are being considered for SiO_2 and Si_3N_4. The

lateral stress distribution σ_{xx} is of particular relevance. For the largest silicon pad $5\mu m$, a small lateral compressive stress is generated at the corner whereas a compressive maximum located at the middle of each silicon pad is created. This stress increases with decreasing line-width to reach a 280 MPa stress for the smallest one in agreement with the stress level extracted from Raman measurements. The situation is completely different just under the SiGe stressor as a tensile stress is generated in the silicon with the larger lattice parameter of SiGe. Using the approach of Pinardi *et al.*[37], the Raman spectra has been estimated by calculating the secular equation using the component of the previous stress tensors. The FE simulation is able to reproduce the variation in term of frequency shift induced by the different SiGe stressors in the silicon part. However, some significative differences can be easily observed in term of magnitude of the frequency shift and the width of the different peak. As point out in an other study, the correspondence and the modelling between the strain induced by frequency shift and the stress field in non-uniformly strained layer is not straightforward[38].

2. Stress distribution and Dark Field Electron Holographic

Fig. 3 presents the periodic structure with $Si_{0.8}Ge_{0.2}$ sources/drains and a simplified gate stack matching the experimental one of reference[21]. The main objective of this subsection is to confront the map predicted by simulation and those obtained by the Dark Field Electron Holographic technique. The lateral and vertical two dimensional stress map are reported in the figure 3. Despite various approximations, these stress maps can be compare to the geometric phase variations obtained by Hÿtch *et al.*[21]. Concerning the variation of the lateral strain predicted by simulation, a close agreement has been obtained as shown in figure 4. The average lateral variation of ϵ_{xx} over 60nm in the silicon part can be directly compard to those predicted by the process simulator. Near the gate oxide, the maximum lateral compressive strain is -1.34 % compared to -1.4 % estimated by the GPA technique.

3. Strain, CBED and GPA distribution

In a recent work, a comparison between CBED and GPA measurements on $Si_{0.82}Ge_{0.18}$ stressors have been performed by Diercks *et al.*[22]. The differences between the two mea-

surements methods are illustrated in Fig. 5. For the lateral strain, the agreement between the FEM simulations and CBED measurements could be emphasised whereas GPA gives a higher stress level of about one third. For the vertical strain, a nice agreement is also observed for distance below 50nm. It could noticed that the stress relaxation towards a free stress state for the domain where only GPA measurements are available is also well described.

B. Simulation of CESL stress distribution

As previously discussed, the Contact Etch Stop Liner technique (CESL) has been intensively integrated as a low cost technique to introduce strain for both pMOSFET and nMOSFET device. The modelling of the stress field generated by compressive stress liner for a pMOSFET device is undertaken. For such purpose, an intrinsic stress component σ_{int} is introduced in the process simulator in order to modelize the stress distribution generated by the stress liner deposition. The deformation introduced to take into account the intrinsic stress is given by the following equation:

$$\epsilon_0 = \frac{1-\nu}{E}\sigma_{int} \tag{2}$$

A simple device test structure with a polysilicon gate (width 50nm) and a nitride spacer (width 7nm) has been considered. A 50nm nitride stress liner with a 1.5 GPa intrinsic compressive stress has been introduced on top of the structure. As pointed out by Loiko *et al.*[33] with refined structural mechanical simulations, the method used for the deposition step modelling is important for the quality of the resulting stress field. A multi-step deposition operation is considered using five elementary steps where for each one 10nm is deposited. Fig. 6 reports the stress mapping in the structure for the different stress components σ_{xx}, σ_{yy}. Using this particular approach, a non uniform stress field is created in the CESL particularly in the gate stack region a shown by the figure 6. A larger tensile stress is generated around the polysilicon gate as the stress level reaches 600 MPa. As pointed out by Orain *et al.*[34] the lateral part of the CESL in mechanical interaction with the silicon has a direct influence on the stress generated in the channel. Therefore, the channel is directly impacted as the stress generated in the channel is much more important and a lateral compressive stress of 590 MPa just below the gate oxide is observed. The vertical stress generated in the channel

is much lower, around 260 MPa just under the gate, whereas a large compressive peak for the shear stress of 560 MPa is observed near the nitride spacer.

IV. STRESS MODELLING OF ESIGE/CESL PMOS DEVICE

A. Modelling aspect

In order to simulate the final stress field resulting of the integration of several stress liners, a simplified process flow has been considered. This subsection describes the various assumptions used for the modelling of the stress field generated by the addition of several uniaxial source of stress for pMOSFET. The experimental split is based on different eSiGe stressors and on the use of CESL as shown in table II matching the experimental work of Verheyen *et al.*[12]. In this work, a significant improvement of the drive current was observed as function of the different stressors. The stress generated by the STI formation is approximated by the introduction of a 140 MPa residual stress to match the stress field obtained after the densification step of the deposited chemical oxide. The stress generated by the thin oxide gate and the high-κ (HfO_2) is obtained by an intrinsic isotropic compressive stress of 400 MPa. The standard thermal budget and the intrinsic stress for PECVD nitride is used for the gate stack. A particular attention is made on the modelling of the etching step in order to match as fine as possible the shape of the source/drain recess regions. A similar approach to section III A is followed for the modelling of the SiGe epitaxy. As no reliable silicidation step modelling is available, a deposition of NiSi is used considering an intrinsic stress of 800 MPa to take into account the tensile stress generated during the temperature ramp down. Standard thermal budget are used for the various deposition step and an annealing at 1030°C is considered for the junction activation step[12]. Finally, the method used in section III B for the modelling of CESL is also adopted. As clearly shown here, all the previous work on simple test structures in order to evaluate the stress field by each uniaxial stress technique is beneficial.

B. Results

Fig. 7 reports the evolution from the top to the bottom of respectively σ_{xx}, σ_{xy} and σ_{yy} component for $eSi_{0.75}Ge_{0.25}$ stressor and a 1.5 GPa compressive stress liner which is

expected to exhibit the maximum stress in the channel. A large compressive lateral and vertical tensile stress confined by the two embedded SiGe stressors in the silicon channel is observed. For the shear stress σ_{xy}, large peaks of about 600 MPa are observed at the convex corner of the e$Si_{0.8}Ge_{0.2}$ stressors and at the extremity of the gate stack spacer. Table II presents the variation of the σ_{xx} and σ_{yy} components for various experimental conditions. The parasitic stress level in the absence of intentional stressors has been estimated as well other then MPa but might be subject to large errors given the numerous assumption. The impact of the different stressors combination is however clearly emphasise. In the case where a 15% Ge content SiGe stressor is integrated, a lateral stress of 460 MPa is observed 10nm just under the gate oxide. The stress level is higher compared to the previous results of section III A 1 observed in μ-RS experiment as the silicon channel width of the device about 30nm is much smaller here. As shown previously, an increase of the Ge concentration is clearly beneficial, as the lateral stress is estimated to be increased by a factor 1.7 to reach 720 MPa. A 1.5 GPa compressive stress liner is also observed to increase the stress peak of 650 MPa in the silicon channel. The maximum lateral stress of 920 MPa is obtained in the case of a 25 % Ge concentration with a 1.5 GPa CESL. The same behaviour can be observed for the other component σ_{yy}. Whereas a tensile component is created for σ_{yy}, the same conclusions apply as function of the stress liner combination. It could be noticed that the additive effect of the different stressors are relatively well described by simulation and the stress enhancement could be correlated with the increase of the drive current observed experimentally[12]. The hole mobility enhancement $\frac{\Delta\mu}{\mu}$ is often assumed[39] to be linearly dependent on the piezoresistance coefficients by the following equation:

$$\frac{\Delta\mu}{\mu} \approx |\pi_{\parallel}\sigma_{xx} + \pi_{\perp}(\sigma_{yy} + \sigma_{zz})| \tag{3}$$

where $\pi_{\parallel} = 718 \times 10^{-12}$ Pa^{-1} and $\pi_{\perp} = -663 \times 10^{-12} Pa^{-1}$. Using the maximum strain level predicted in the experimental split ($\sigma_{xx} = -920$ MPa and $\sigma_{yy} = 610$ MPa) predicted would lead to a theoretical 106 % increase of the hole mobility at the top center of the gate oxide. However, it has been clearly shown by the stress mapping that it decreases rapidly far from the gate oxide in the silicon channel which could explain reasonably that the total drive current is not enhanced to the same level.

V. CONCLUSION

Given the complexity, the cost and the various experimental limitations to estimate the stress field in the silicon channel by using only experimental technique, process simulation is a complementary interesting approach. In the case of eSiGe embedded stressors, the simulation and the confrontation to three different experimental configurations and various experimental characterisation have been undertaken. Despite some limitations in the approach due to the plane strain approximations for two dimensional FEM simulations, a relatively good agreement is obtained for the stress estimated by the different characterisation technique. Some significative difference are observed in the case of μ-RS measurements but the peak deconvolution by the Pinardi's approach is a complex task and an relative issue. A nice agreement for CBED and GPA has been obtained with the FEM simulations. Basically for simple stress technology booster like eSiGe stressor or CESL, first order stress modelling based on the introduction of an intrinsic or lattice mismatch stress can provide some insight about the level and the distribution of the stress field generated in the silicon channel after the different processing steps. The possibility to describe additive effects of intentional and parasitic stress sources for a pMOSFET device with several stress sources have been underlined. A link can be made between the enhancement of the drive current observed experimentally and the increase in term of stress level in the channel predicted by process simulation. It shows the interest for process simulation combined with experimental characterisation to investigate the stress map in the channel device. However, some limitations have been also be discussed on the way to model the deposition step for stress liners and on the influence of the silicidation step on the global stress field. This step has been observed to decrease significantly the level of stress generated by eSiGe stressor[23]. Many new and complex uniaxial stress techniques are under optimisation in the stress engineering approach. Such complex techniques like stress memorisation[40] are very difficult to modelise even empirically and are interesting challenges for future research work.

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Material	Equip -ment	Young Modulus [GPa]	Poisson Ratio	α	Intrinsic Stress [MPa]	Rheolo -gical
SiO_2	Thermal	66	0.17	0.5	-400	VE
	HDP	80	0.2	0.5	0	VE
	TEOS	60	0.25	0.6	0	VE
Si_3N_4	PECVD	143	0.28	3.0	-150	VE
	LPCVD	290	0.28	3.0	1200	VE
PolySi	LPCVD	180	0.27	3.05	-350	E
TiN	Sputtering	410	0.3	9.6	N/A	E
NiSi	Thermal	112	0.3	9.5		VE

TABLE I. Mechanical parameters and rheological behaviour of the different materials considered. E correspond to an elastic material whereas VE to a viscoelastic behaviour.

Split	σ_{xx} (MPa)	σ_{yy} (MPa)	ϵ_{xx} (%)	ϵ_{yy} (%)	ΔI_{on} (%)
Reference	$\sim$ -50	$\sim$ -30	$\sim$ -0.01	$\sim$ -0.01	-
$eSi_{0.85}Ge_{0.15}$	-460	150	-0.29	0.21	20 %
$eSi_{0.75}Ge_{0.25}$	-720	320	-0.50	0.35	40 %
CESL	-210	260	-0.18	0.23	30 %
$eSi_{0.85}Ge_{0.15}$ & CESL	-650	460	-0.48	0.46	50 %
$eSi_{0.75}Ge_{0.25}$ & CESL	-920	610	-0.68	0.63	65 %

TABLE II. Various technological stress sources and stress component observed at the top center of the silicon channel 10nm just below the gate oxide. The last column reports the experimental increase in terms of drive current observed experimentally[12].

CAPTIONS

Fig. 1 Experimental structure of Nouri *et al.* where each $Si/SiO_2/Si_3N_4$ pad is separated by a SiGe layer. Each layer has a length of 5μm and a variable depth between 30-150 nm.

Fig. 2 The top figure presents the lateral stress distribution estimated in the structure. A $Si_{0.8}Ge_{0.2}$ layer of 150nm is considered corresponding to the maximum stress level possible

in the experimental conditions range. At the bottom, the comparison between the experimental μ-RS, a theoretical estimation using Pinardi and coworkers approach[37]. A standard wavelength of 2.71 eV, a lateral deviation of 0.22 μm and a depth penetration of 320nm has been assumed for the simulation of the strained induced frequency shift in the silicon layer. The phonon deformation potential constants are : $K_{11} = -1.43$, $K_{12} = -1.89$ and $K_{44} = -0.59$.

Fig. 3 Respectively lateral (top figure) and vertical (bottom) stress distribution estimated by process simulation in the structure matching those used by Hÿtch *et al.*[21] for the Dark Field Electron Holographic technique. In relative agreement with the experimental result, the maximum lateral strain ϵ_{xx} near the oxide gate predicted by FEM simulations is -1.34 % corresponding to a lateral stress σ_{xx} of 1.3 GPa.

Fig. 4 Comparison between the mean lateral cross section of the ϵ_{xx} component reported by Hÿtch *et al.*[21] and the results of FEM simulations also averaged on several depth over 60nm. The lateral strain variations along the structure are relatively well described by process simulation.

Fig. 5 Comparison between the lateral and vertical strain distribution of Diercks *et al.* using CBED and GPA and FEM simulations. The strain relaxation as function of the distance from the base of the gate oxide is well described and in nice agreement with CBED experiments with a maximum error less than 15 %.

Fig. 6 Lateral and vertical stress distribution generated by a 1.5 GPa intrinsic compressive stress liner. The interaction between the CESL nitride layer and the gate generate mostly an uniaxial stress in the channel

Fig. 7 This figure presents respectively (from the top to the bottom) the σ_{xx}, σ_{xy} and σ_{yy} stress distribution generated by the various stress sources. The reference roughly estimates the parasitic stress that should originate from undesired sources such as STI and silicidation. The interaction between the CESL nitride layer and the gate increases the uniaxial stress generated by the eSiGe stressors in the channel.

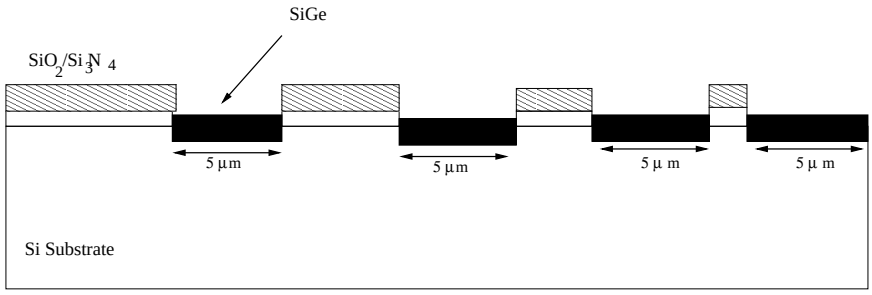


FIG. 1.

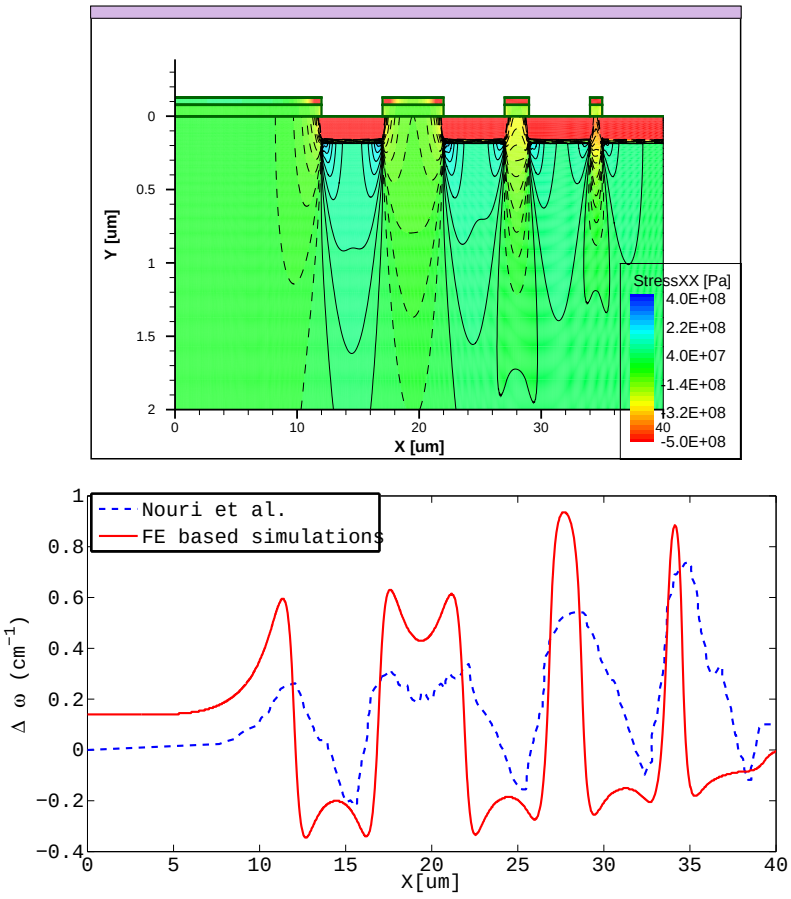
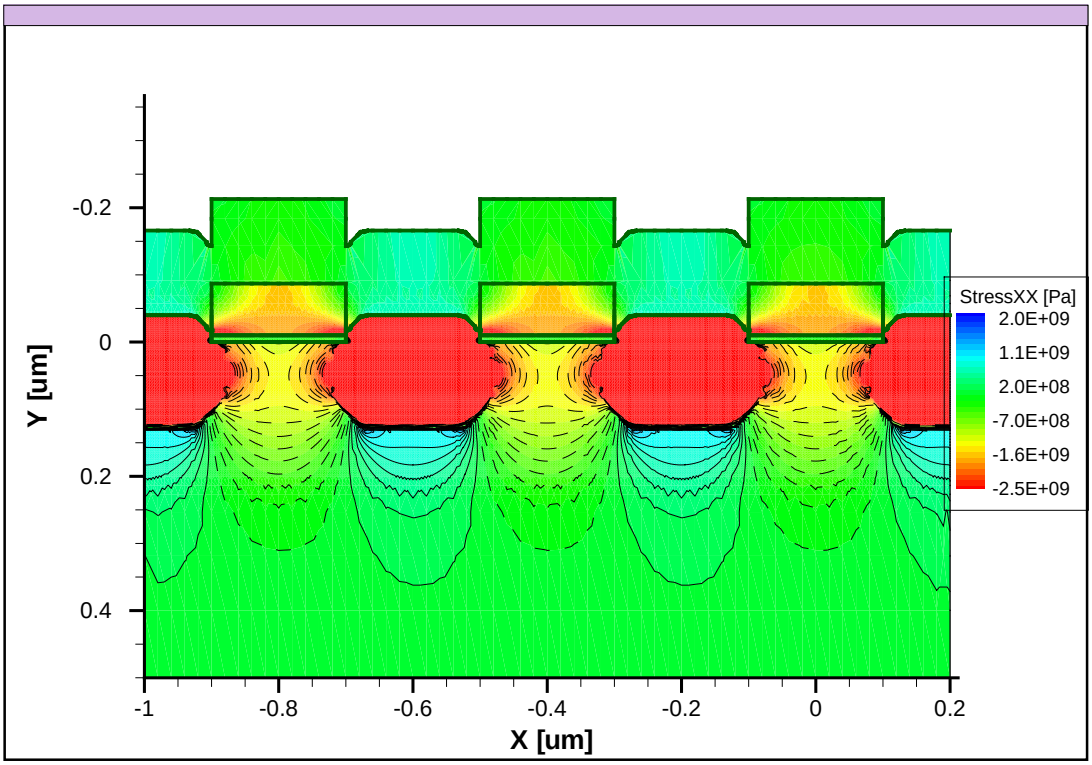

Y [um]
X [um]
StressXX [Pa]
4.0E+08
2.2E+08
4.0E+07
-1.4E+08
-3.2E+08
-5.0E+08
Nouri et al.
FE based simulations
Δ ω (cm^{-1})
X[um]

FIG. 2.


StressXX [Pa]
2.0E+09
1.1E+09
2.0E+08
-7.0E+08
-1.6E+09
-2.5E+09
Y [um]
-0.2
0
0.2
0.4
-1
-0.8
-0.6
-0.4
-0.2
0
0.2
X [um]

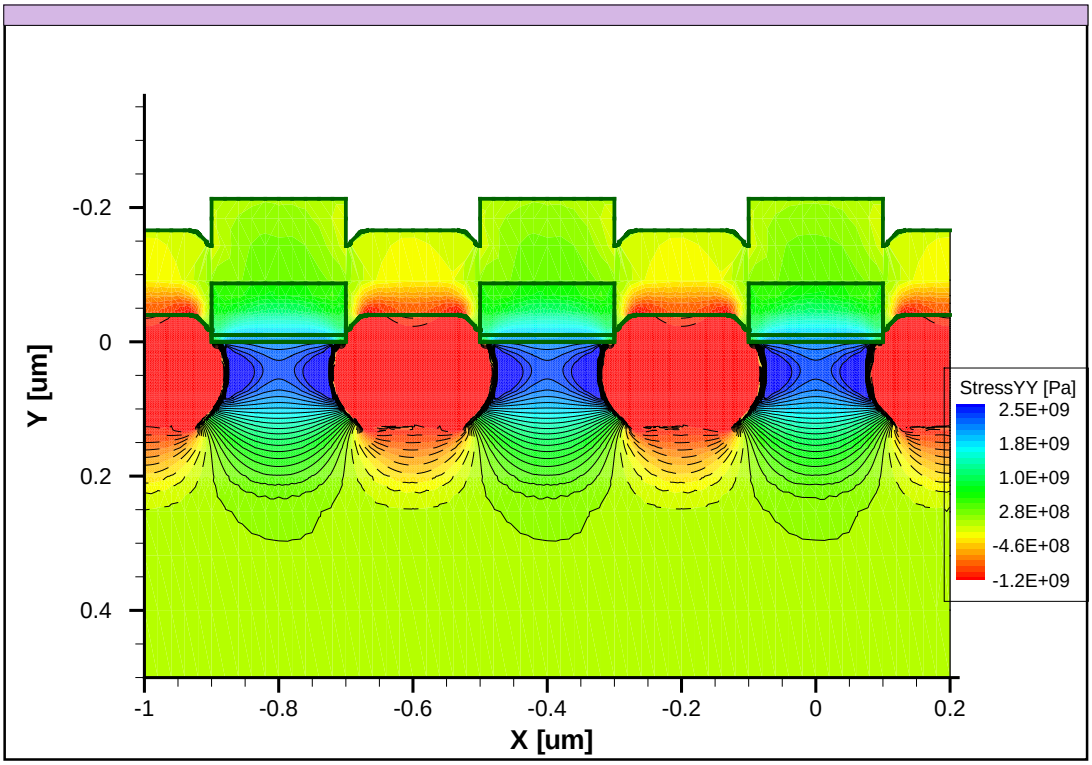

StressYY [Pa]
2.5E+09
1.8E+09
1.0E+09
2.8E+08
-4.6E+08
-1.2E+09
Y [um]
-0.2
0
0.2
0.4
-1
-0.8
-0.6
-0.4
-0.2
0
0.2
X [um]

FIG. 3.

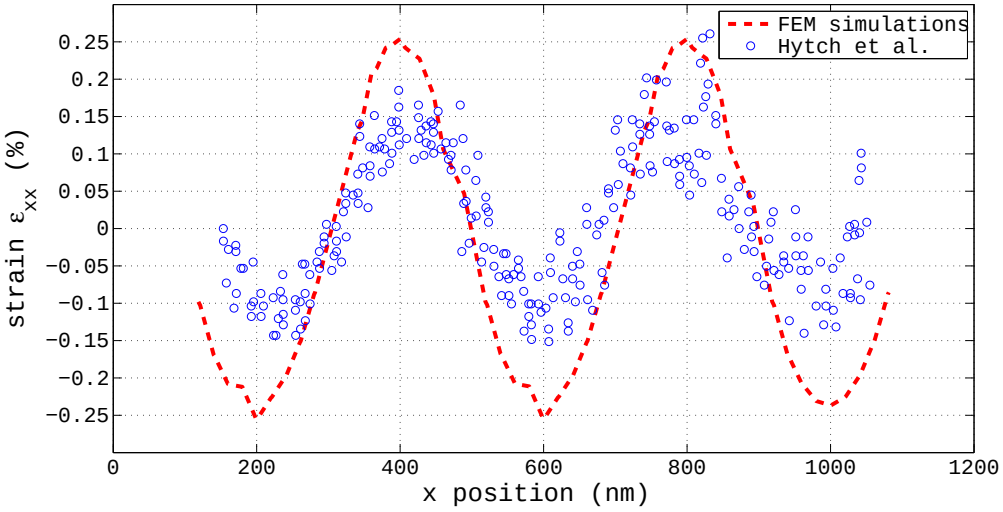

FEM simulations
Hytch et al.
strain ε_{xx} (%)
x position (nm)
0.25
0.2
0.15
0.1
0.05
0
−0.05
−0.1
−0.15
−0.2
−0.25
0
200
400
600
800
1000
1200

FIG. 4.

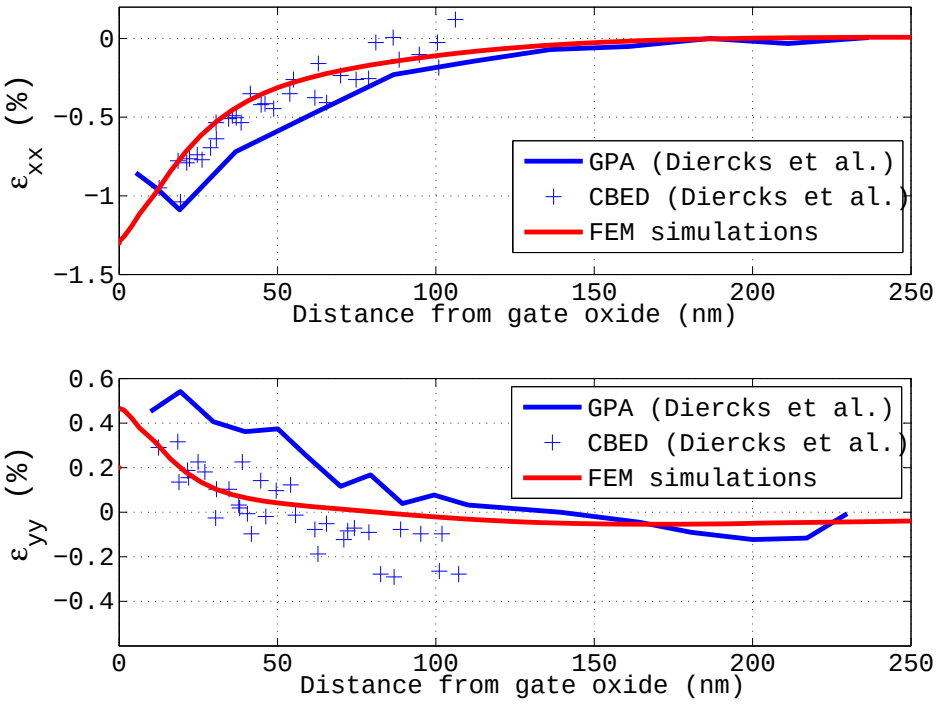

0
−0.5
−1
−1.5
ε_{xx} (%)
0
50
100
150
200
250
Distance from gate oxide (nm)
GPA (Diercks et al.)
CBED (Diercks et al.)
FEM simulations
0.6
0.4
0.2
0
−0.2
−0.4
ε_{yy} (%)
0
50
100
150
200
250
Distance from gate oxide (nm)
GPA (Diercks et al.)
CBED (Diercks et al.)
FEM simulations

FIG. 5.

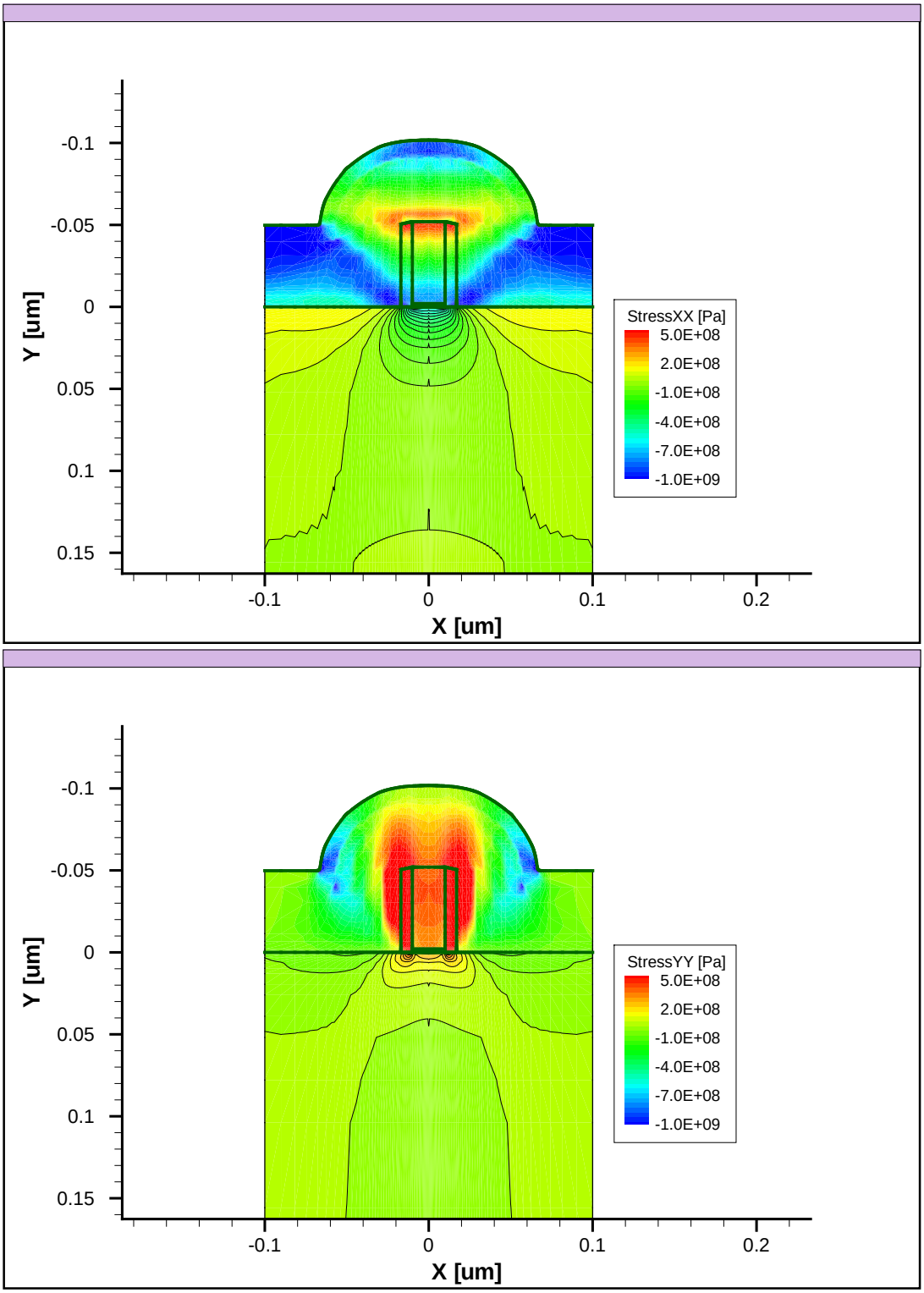

-0.1
-0.05
0
0.05
0.1
0.15
Y [um]
-0.1
0
0.1
0.2
X [um]
StressXX [Pa]
5.0E+08
2.0E+08
-1.0E+08
-4.0E+08
-7.0E+08
-1.0E+09
StressYY [Pa]
5.0E+08
2.0E+08
-1.0E+08
-4.0E+08
-7.0E+08
-1.0E+09

FIG. 6.

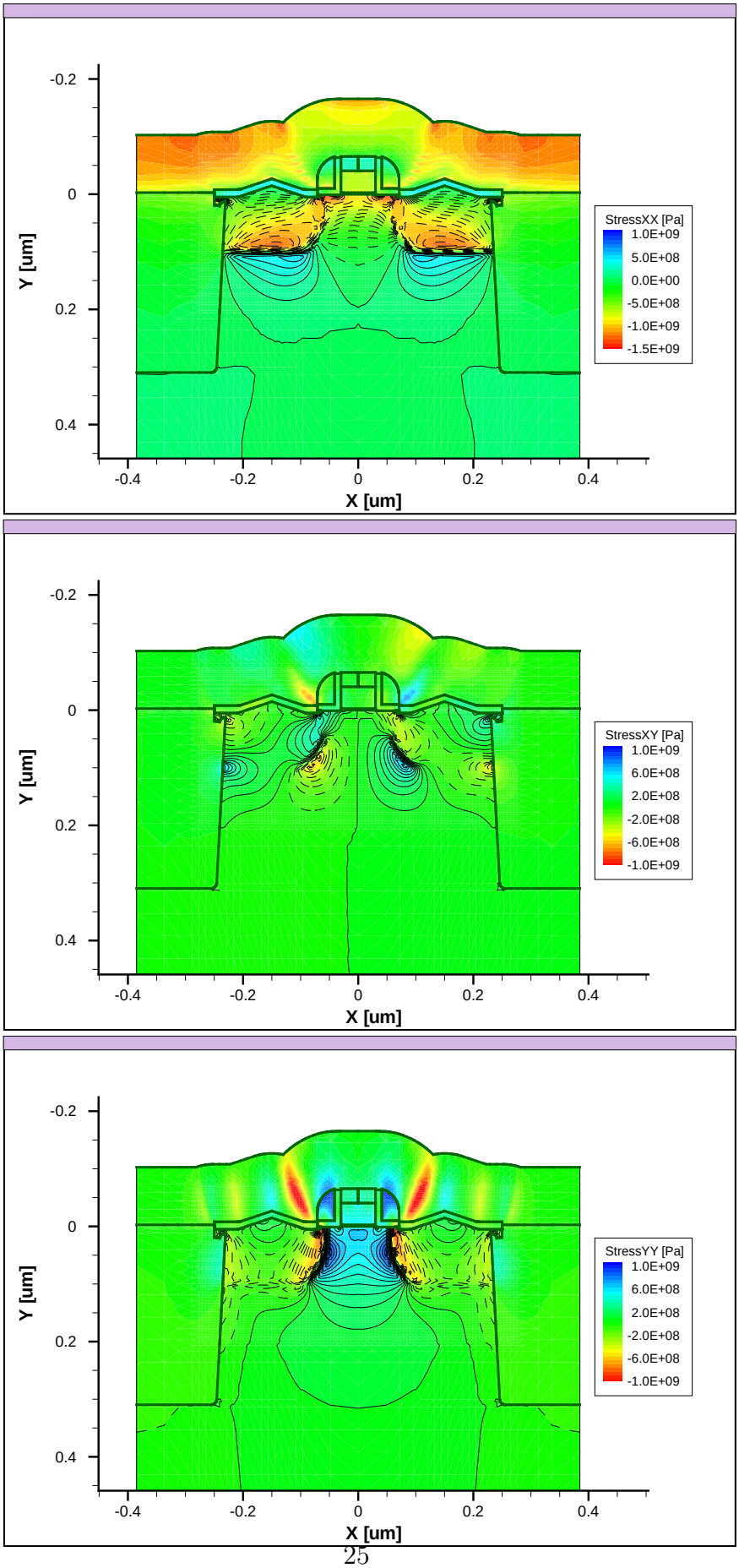

StressXX [Pa]
1.0E+09
5.0E+08
0.0E+00
-5.0E+08
-1.0E+09
-1.5E+09
StressXY [Pa]
1.0E+09
6.0E+08
2.0E+08
-2.0E+08
-6.0E+08
-1.0E+09
StressYY [Pa]
1.0E+09
6.0E+08
2.0E+08
-2.0E+08
-6.0E+08
-1.0E+09
Y [um]
X [um]
-0.2
0
0.2
0.4
-0.4
-0.2
0
0.2
0.4

FIG. 7.