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Reducing damage to Si substrates during gate etching processes by synchronous plasma pulsing

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Plasma oxidation of the c-Si substrate through a very thin gate oxide layer can be observed during HBr/O₂/Ar based plasma overetch steps of gate etch processes. This phenomenon generates the so-called silicon recess in the channel and source/drain regions of the transistors. In this work, the authors compare the silicon recess generated by continuous wave HBr/O₂/Ar plasmas and synchronous pulsed HBr/O₂/Ar plasmas. Thin SiO₂ layers are exposed to continuous and pulsed HBr/O₂/Ar plasmas, reproducing the overetch process conditions of a typical gate etch process. Using *in situ* ellipsometry and angle resolved X-ray photoelectron spectroscopy, the authors demonstrate that the oxidized layer which leads to silicon recess can be reduced from 4 to 0.8 nm by pulsing the plasma in synchronous mode. © 2010 American Vacuum Society.
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I. INTRODUCTION

For the next technological generations of integrated circuits, the challenges faced by etch plasmas (e.g., profile control, selectivity, critical dimension control, uniformity, defects, etc.) are intensified by the use of new materials, the limitations of lithography, and the recent introduction of new device structures and integration schemes.¹ Chemical composition of the plasma can be tuned by modifying the gas mixture, ion flux can be partly controlled by source power (either coupled inductively or capacitively) but not independently from radicals' production, and ion energy can be adjusted thanks to the rf bias power applied to the wafer. However, these parameters are not always sufficient to reach the appropriate etching characteristics² and new knobs are always added to improve plasma performance and more particularly to improve the critical dimension control of the patterned nanostructures.¹

There are many ways to modify the plasma regime. For example, one can modify temporally the parameters of the plasma. Parameter ramping can be used to progressively modify one parameter such as a gas flow during the process.³ Gas chopping or time multiplexing may be used to pulse the gas injection in the time scale of seconds, as it is done in the Bosch process.⁴ However, these techniques necessitate a significant change in the hardware of current 300 mm tools. Turning on and off the plasma chamber generators in a 1 ms time scale—also called plasma pulsing—leads to a major plasma modification while requiring only a minor hardware modification. In the following, pulsed plasmas will refer to plasmas where the generators are pulsed, whereas all the other parameters (gas flow, temperature, pressure, etc.) are kept constant.

Pulsing the plasma source power and/or the substrate bias power offers new degrees of freedom to tune the neutral species concentration as well as charged particle concentration in the plasma. The main advantages of pulsed plasma processes reported in the literature are the improvement in etch selectivity and the reduction of charge-up damage and defects by reducing the electron shading phenomena and controlling the dissociation of radicals in the plasma.^{5–8} However, even if a significant number of studies have been published, capabilities of pulsed plasma processes still need to be carefully addressed and understood for real etch processes.

A polysilicon gate etch process is typically composed of three different steps:⁹ a main etch step which must deliver straight polysilicon profiles with a minimum etch rate dependence with the aspect ratio of the structures, a low hard mask erosion, and a minimum profile difference between dense and isolated structures. It is followed by the so-called soft landing step, a brief step during which the plasma lands on the gate oxide under reduced ion bombardment energy conditions with the objective to cut the foot left at the bottom of the gate by the main etch step of the process. In this step, the notching capabilities of the plasma that are attributed to the positive charging that builds up on the thin gate oxide are important. Finally, the role of the overetch step is to remove polysilicon etch residues remaining after the soft landing step in dense silicon structures where the etch rate is the lowest.² Plasma operating conditions and chemistry of the overetch step must generate extremely selective etch conditions to the very thin gate oxide (typically in the nanometer range in thickness) when the gate oxide is exposed to the plasma. State of the art plasma operating conditions are usually obtained in low-power, high-pressure HBr/O₂ plasmas. It is important to point out that even if HBr/O₂ plasmas leave intact the original gate oxide grown on the c-Si sub-

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strate, oxidation of the underlying silicon substrate can occur during the overetch step as mentioned in previous studies.^{10,11} In fact, it has already been demonstrated that during the HBr/O₂ plasma, an ion assisted radical diffusion through the thin gate oxide leads to the oxidation of the underlying silicon, forming a 2–5 nm SiO_x layer below the gate oxide.¹¹ This plasma silicon oxidation leads to the so-called Si recess after oxide removal in the active regions of the transistor and is detrimental to device reliability and performance.¹² This phenomenon has been described and investigated several times in the literature^{10–15} and is a major issue for thin silicon channel metal-oxide-semiconductor field-effect transistor integration. In this paper, we evaluate the potential of HBr/O₂/Ar synchronized pulsed plasmas to minimize the silicon recess formation.

II. EXPERIMENT

To explore the impact of the synchronous pulsed plasmas on the etch characteristics, the HBr/O₂/Ar overetch process for silicon gate application is considered. The plasma is operated at 50 mT, with a HBr/O₂/Ar gas flow of 200/5/150 SCCM (SCCM denotes cubic centimeter per minute at STP), and with a source and bias power of 500 and 100 W, respectively. Those plasma conditions are typically used in continuous wave (cw) mode to achieve high poly-Si/SiO₂ selectivity (selectivity is defined as the ratio between the poly-Si and SiO₂ etch rates) for the fabrication of poly-Si gate electrodes.

The etching of blanket samples of poly-Si and SiO₂ is investigated for various pulsing conditions. 300 mm silicon wafers coated with 50 nm of thermally grown SiO₂ and 300 nm of polysilicon are used for poly-Si etch rate measurements, while blanket silicon wafers coated with 10 nm of thermally grown oxide are used for SiO₂ etch rate measurements. Blanket wafers coated with a thin (2.5 nm) thermally grown silicon oxide are used for silicon damage characterization.

The experiments are performed in a 300 mm AdvantEdge™ inductively coupled plasma (ICP) etch tool from Applied Materials. The ICP reactor chamber walls are coated by Al₂O₃. The plasma is excited inductively via two rf coils (13.56 MHz) to improve the ion flux uniformity. Applied Materials has modified its rf system to the Pulsync™ system, which provides full pulsing capabilities at frequencies between 100 Hz and 20 kHz, with duty cycles between 10% and 90%. More details of the plasma chamber can be found in the literature.⁵ The system is capable of pulsing both source and/or bias independently or in a fully synchronized manner. Even if a delay can be introduced between the source and the bias pulsing, only synchronous mode (with simultaneous pulsing of source and bias in phase) is studied in this paper.

The etch reactor is equipped with a multiwavelength ellipsometer Uvisel from Jobin Yvon. This phase modulated ellipsometer enables *in situ* spectroscopic ellipsometry between 1.5 and 5 eV and real-time kinetic measurements using 16 wavelengths.

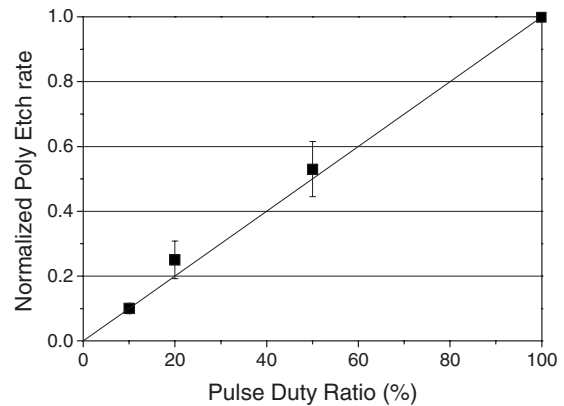


FIG. 1. Blanket polysilicon etch rates normalized to cw baseline as a function of duty cycle for synchronous pulsed plasma operated at 1 kHz.

X-ray photoemission spectroscopy (XPS) measurements are performed on a customized Thermo Electron Theta 300 spectrometer, directly interfaced to the etch platform via a vacuum transfer chamber.¹⁶ The XPS system is equipped with a high resolution monochromatic Al K_α x-ray source (1486.6 eV photons). The angle resolved capability of the Theta 300 is used for all analyses, with eight angles regularly spaced between 23.75° and 76.25° referred to the normal of the wafer. A genetic algorithm based on the maximum entropy method is used to reconstruct depth profiles from angle resolved XPS data.^{17,18} The fitting procedure assumed that photoelectrons coming from the underlying silicon bulk are detected at least at 23.75° emission angle. In other words, with a Si 2*p* photoelectron attenuation length in SiO₂ of 3.45 nm,¹⁹ the final overlayer thickness is assumed to be lower than ~9 nm whatever the process used. This allows maximizing the profile information content.²⁰ Since the overlayer density is unknown after plasma treatment, the depth scale should be interpreted in a qualitative way.²¹

III. RESULTS

A. Etch rate

The etch rates of blanket polysilicon wafers are investigated by kinetic ellipsometry. Under our conditions, the poly-Si etch rate is about 60 nm min⁻¹ in cw mode. As shown in Fig. 1, the etch rate in synchronized pulsed conditions is lower than in cw and presents a linear decrease with the duty cycle. This result suggests that polysilicon etching proceeds mostly during the on time period of the plasma at the same rate as the one obtained in cw mode (60 nm min⁻¹), while neither significant oxidation nor deposition occurs during the off time, which does not block or enhance the etch rate.⁶

When thick SiO₂ wafers (10 nm of SiO₂ on silicon wafers) are exposed to the same plasma conditions (pulsed or cw), no measurable etching of the oxide is observed, indicating that the selectivity of the HBr/O₂/Ar etch process can be considered as infinite.

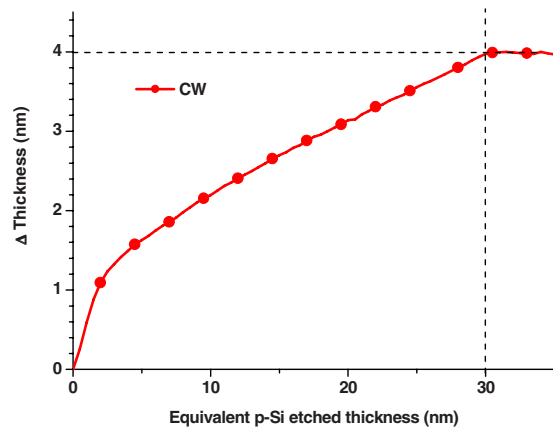


FIG. 2. (Color online) Damaged thickness measured by kinetic *in situ* ellipsometry as a function of plasma exposure time in cw mode.

B. Degradation of Si substrate

In our process conditions, we have shown that the selectivity between polysilicon and SiO_2 is infinite. However, etch rates have been measured on thick films, while the silicon recess phenomenon is observed only through ultrathin gate oxide showing that the ion enhanced oxidation phenomenon occurs through the thin gate oxides.²² It is thus important to estimate the damage to the silicon underneath when thin silicon oxide is exposed to the $\text{HBr}/\text{O}_2/\text{Ar}$ plasma, as it is the case in a gate etch process.

The process step investigated here is an overetch process dedicated to gate patterning. The overetch time is usually set as a percentage of the etching process time and is usually set according to difference in etch rate between isolated polysilicon gates and the highest aspect ratio gates. In the following, we choose a $\text{HBr}/\text{O}_2/\text{Ar}$ process time corresponding to 50% of the time required to etch a 60 nm thick polysilicon gate (i.e., the time required to etch 30 nm of polysilicon).

When a thin oxide film (2.5 nm) is exposed to the $\text{HBr}/\text{O}_2/\text{Ar}$ plasma in cw mode, the SiO_2 thickness increases during plasma exposure, as shown in Fig. 2. Since we know from experiments conducted on thicker oxides that no etching proceeds, we can conclude that this increase in SiO_2 thickness is fully attributed to an oxidation phenomenon of silicon through the thin, as deposited, 2.5 nm thick oxide. The difference in SiO_2 thickness before and after plasma exposure is defined as the damage thickness (Δ thickness). Figure 2 shows that the damage thickness (Δ thickness) under the gate oxide has reached about 4 nm after 30 s exposure to the $\text{HBr}/\text{O}_2/\text{Ar}$ plasma in cw.

This phenomenon can be explained by the reoxidation of the silicon underneath through the thin gate oxide.¹¹ This tends to increase the oxide thickness, leading to Si recess after subsequent wet clean steps.

To better understand this phenomenon, angle resolved XPS (ARXPS) analyses are performed on thin silicon oxide wafers before and after exposure to the $\text{HBr}/\text{O}_2/\text{Ar}$ plasma in cw mode for 30 s. Figure 3 shows the Si $2p$ core level photoelectron spectrum measured at 23.75° (near normal angle) on the thin gate oxide prior to exposure to the

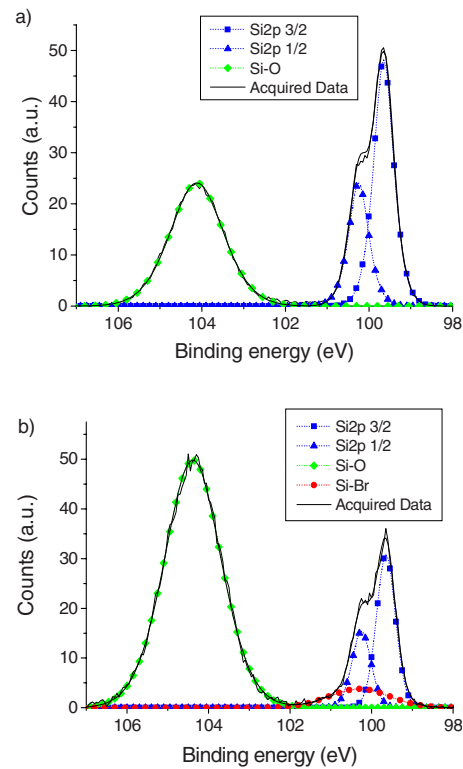


FIG. 3. (Color online) Si $2p$ core level spectra of thin (2.5 nm) SiO_2 layer measured by XPS at 23.75° (a) before and (b) after exposure to $\text{HBr}/\text{O}_2/\text{Ar}$ plasma in cw mode.

$\text{HBr}/\text{O}_2/\text{Ar}$ plasma [Fig. 3(a)] and after exposure [Fig. 3(b)]. Figure 3(a) shows that the Si $2p$ region contains two major peaks: SiO_2 at 104.1 eV and Si from the underlying substrate at 99.6 eV (for the 3/2 spin orbit doublet). In Fig. 3(b), the Si spectrum after exposure to the plasma contains three contributions. The contribution at 104.5 eV corresponds to an oxygen-rich SiO_xBr_y . The contribution at 99.6 eV corresponds to the bulk silicon. The small contribution at 100.5 eV is attributed to silicon bonded to bromine at the interface.^{23,25} The presence of the SiBr_x environment clearly shows that some bromine from the plasma diffuses or gets implanted through the thin SiO_2 to the SiO_2/Si interface in cw mode. When the bromine reaches the interface, it reacts with the silicon of the substrate forming Si–Br bonds.

Furthermore, after etching, the integrated intensity of the Si–O peak increases while the bulk Si peak intensity decreases, confirming an increase in SiO_2 thickness.

A Br $3d$ peak corresponding to 6.5 at. % of the analyzed surface (at 23.75° take-off angle) can be observed at ≈ 71 eV (Fig. 4). The Br $3d$ spectrum contains three contributions. Two main emissions at 71.1 and 70.4 eV are observed, with a third small signal at 69.4 eV (for the 5/2 spin orbit doublets). The 69.4 eV peak is attributed to photoelectrons emitted by Br atoms bonded to Si.²⁴ The higher energy emission at 71.1 eV can be ascribed to Br incorporated into the SiO_2 layer. The third Br $3d$ peak, at 70.4 eV, is ascribed to Br bonded to Si and SiO_2 at the interface.

This spectrum shows that some bromine is also incorporated into the SiO_2 layer, transforming the oxide in an

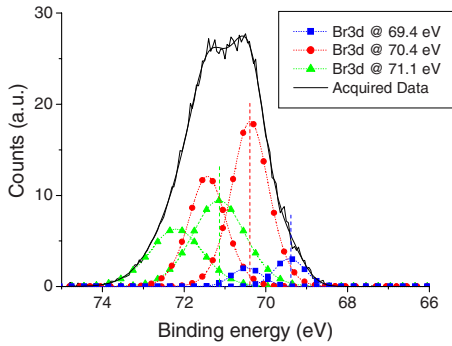


FIG. 4. (Color online) Br $3d$ core level spectrum of thin (2.5 nm) SiO_2 layer measured by XPS at 23.75° after exposure to $\text{HBr}/\text{O}_2/\text{Ar}$ plasma in cw mode.

oxygen-rich SiO_xBr_y layer. As a consequence, the silicon surface after exposure to the $\text{HBr}/\text{O}_2/\text{Ar}$ plasma in cw mode is covered with an oxygen-rich SiO_xBr_y layer, with a SiBr_x layer at the interface with the silicon wafer. It has to be reminded that hydrogen cannot be detected by XPS and might be present in the SiO_xBr_y and in the SiBr_x layers.

Although depth profile reconstruction from ARXPS measurements should be interpreted qualitatively, Fig. 5(a) also suggests the preferential accumulation of bromine at the $\text{SiO}_x\text{Br}_y/\text{Si}$ interface. More precisely, if we examine the de-

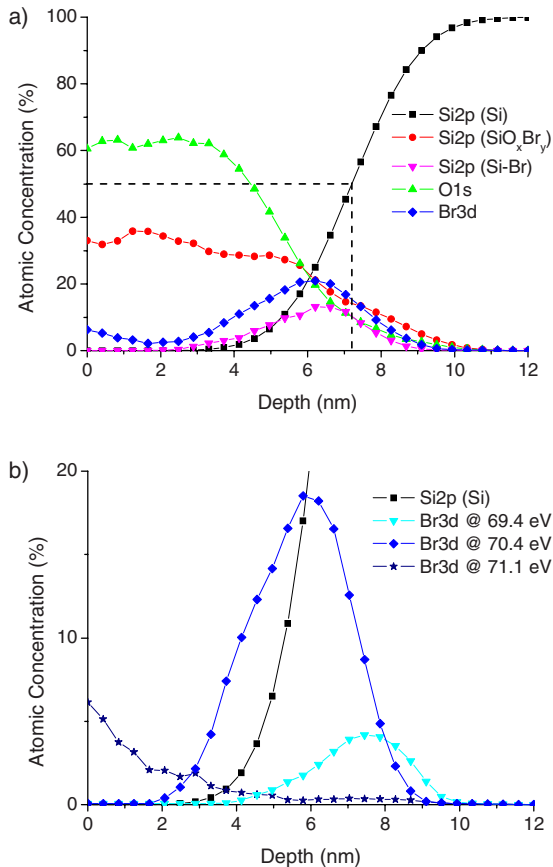


FIG. 5. (Color online) Atomic concentration depth profile of SiO_2 layer exposed to $\text{HBr}/\text{O}_2/\text{Ar}$ plasma in cw mode: (a) global depth profile and (b) decomposition of Br profile.

TABLE I. Damaged thickness after plasma exposure (cw and pulsing synchronous mode) with time compensation to match poly-Si etched thickness.

	1 kHz pulse frequency				20% duty cycle		
	cw	50%	20%	10%	5 kHz	1 kHz	200 Hz
Etch time (s)	30	56	105	300	140	105	105
Δ thickness (nm)	4	2.1	1.0	1.2	0.8	1.0	1.1

composition of Br in the SiO_2 layer [Fig. 5(b)], we show a good correlation with the attribution of Br $3d$ peaks (Br incorporated into the SiO_2 layer, accumulation at the interface SiO_2/Si , and Br atoms bonded to Si).

It can be noticed that the overlayer thickness estimated using the profile reconstruction from ARXPS (thickness for which the bulk signal represents 50% of the composition) is close to 7 nm (in good agreement with the ellipsometric measurement of 6.5 nm).

C. Diminution of Si recess

Using synchronized pulsed plasmas, the silicon etch rate is lower than in cw mode. To reflect this change, the wafer coated with thin SiO_2 is exposed to pulsed plasma conditions using etch rate compensation, meaning that the time is targeted to etch a constant polysilicon thickness (50% of overetch for 60 nm thick polysilicon gate). Table I presents the overetch time for each condition investigated together with the corresponding Δ thickness. As we observed under cw plasma exposure, the SiO_2 thickness increases when the wafer is exposed to $\text{HBr}/\text{O}_2/\text{Ar}$ plasmas in pulsed conditions. However, the damaged layer thickness reported in Table I and plotted in Fig. 6 is strongly reduced from 4 nm in cw mode down to 0.8 nm at 20% duty cycle and 5 kHz.

Those data clearly show that synchronously pulsing the $\text{HBr}/\text{O}_2/\text{Ar}$ plasma strongly limits the reoxidation of the silicon substrate through the thin SiO_2 gate oxide exposed to

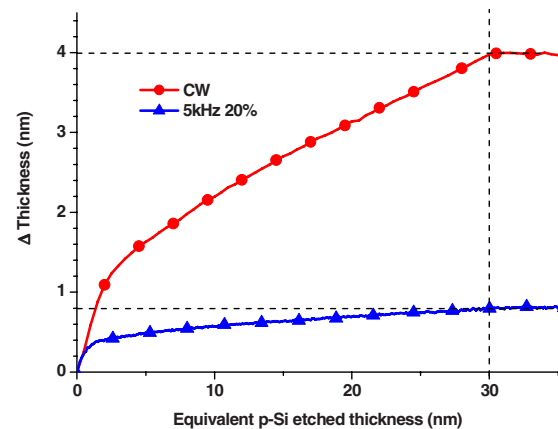


FIG. 6. (Color online) Damaged thickness measured by kinetic *in situ* ellipsometry as a function of equivalent poly-Si etched thickness in cw mode and synchronous pulsing mode with 5 kHz and 20% of duty cycle.

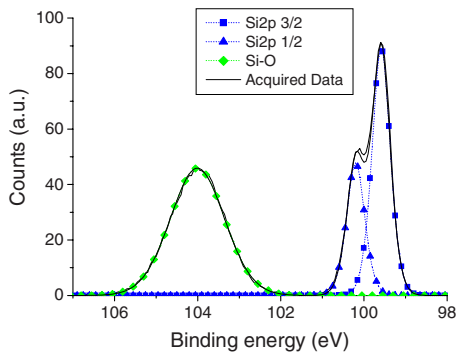


FIG. 7. (Color online) Si $2p$ core level spectrum of thin (2.5 nm) SiO_2 layer measured by XPS at 23.75° after exposure to $\text{HBr}/\text{O}_2/\text{Ar}$ plasma pulsed at 5 kHz and 20%.

the plasma. As a consequence, the silicon recess after subsequent steps will be strongly minimized. High pulsing frequencies (>1 kHz) and low duty cycles ($<50\%$) present the most promising results.

To understand this fundamental difference between cw and pulsed plasma etch processes, ARXPS analyses are performed on thin silicon oxide wafers after exposure to the $\text{HBr}/\text{O}_2/\text{Ar}$ plasma in synchronized pulsed plasma mode using the best conditions (i.e., 5 kHz/20%). For this process a Δ thickness of ≈ 0.8 nm is measured while the cw mode leads to ≈ 4 nm of Δ thickness. Figure 7 shows the Si $2p$ core level photoelectron spectrum measured at 23.75° (near normal angle) on the thin gate oxide exposed to the $\text{HBr}/\text{O}_2/\text{Ar}$ plasma in pulsed conditions. In contrast to the cw process, the Si spectrum after pulsed plasma exposure contains only two contributions: Si–O (≈ 104 eV) from an oxide layer and Si–Si (≈ 99.6 eV for the $3/2$ spin orbit doublet) from the bulk Si. There is no significant Si–Br peak (≈ 100.5 eV) detected in those conditions. The absence of the SiBr_x environment clearly shows that the diffusion or implantation of the bromine from the plasma through the thin SiO_2 to the silicon substrate interface is strongly limited when using the pulsed plasma mode. As a consequence, almost no bromine can reach the interface and react with the silicon substrate forming Si–Br bonds. The Br $3d$ region

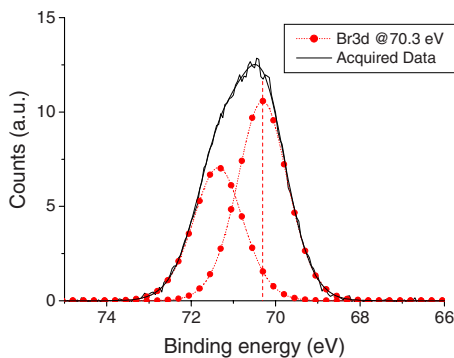


FIG. 8. (Color online) Br $3d$ core level spectrum of thin (2.5 nm) SiO_2 layer measured by XPS at 23.75° after exposure to $\text{HBr}/\text{O}_2/\text{Ar}$ plasma pulsed at 5 kHz and 20%.

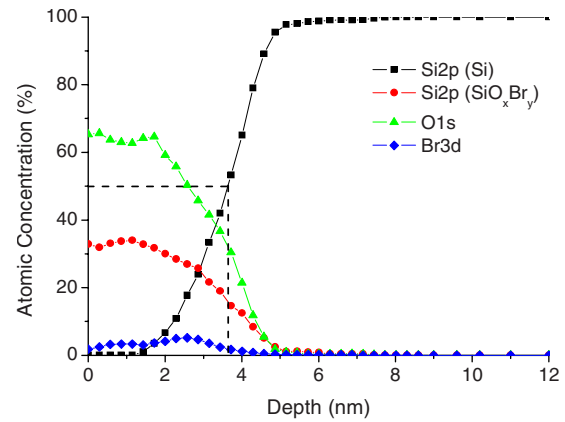


FIG. 9. (Color online) Atomic concentration depth profile of SiO_2 layer exposed to $\text{HBr}/\text{O}_2/\text{Ar}$ plasma pulsed at 5 kHz and 20%.

(Fig. 8) contains only one contribution at ≈ 70.3 eV (for the $5/2$ spin orbit doublet). This peak corresponds to only 2.4 at. % (6.5 in cw mode) of the analyzed surface. This contribution shows that much less bromine is incorporated in the SiO_2 layer, leading to a more oxygen-rich SiO_xBr_y layer than in cw mode. Therefore, the silicon surface after exposure to the pulsed $\text{HBr}/\text{O}_2/\text{Ar}$ plasma is covered with an oxygen-rich SiO_xBr_y layer, with no significant SiBr_x interface layer. This interpretation is supported by the concentration depth profile presented in Fig. 9 and calculated from ARXPS data after exposure to the $\text{HBr}/\text{O}_2/\text{Ar}$ in pulsed conditions. In this case, the overlayer thickness estimated from the profile reconstruction is close to 3.5 nm (in good agreement with the ellipsometric measurement of 3.3 nm).

IV. DISCUSSION

The data presented in the previous sections have shown several effects:

1. The polysilicon etch rate scales with the duty cycle, which tends to indicate that the etching occurs during the plasma on time only with a constant rate and is not slowed down by the off time period.
2. An infinite selectivity between poly-Si and SiO_2 is obtained. On thin layers, this high selectivity is accompanied with an oxidation phenomenon of the bulk silicon through the thin oxide.¹¹
3. In cw, a thick oxidation of the silicon bulk is generated upon exposure of $\text{HBr}/\text{O}_2/\text{Ar}$ plasmas, while it is strongly reduced with $\text{HBr}/\text{O}_2/\text{Ar}$ synchronous pulsed plasmas.
4. In cw, bromine is incorporated into the overlayer (6.5%) and reaches the interface between Si and SiO_2 , with the formation of a SiBr_x layer.
5. In pulsed plasma conditions, much less bromine is incorporated (2.4% of the top surface), and no SiBr_x bonds are observed at the silicon interface.

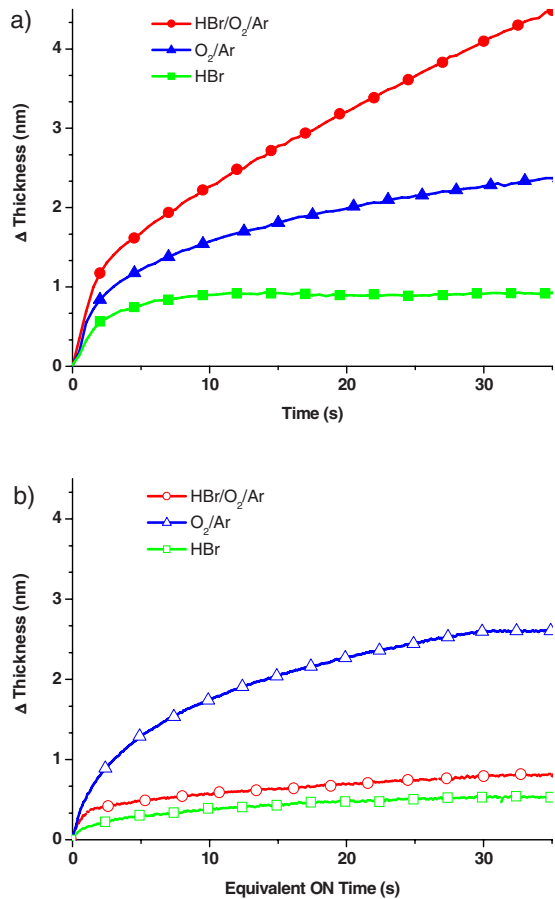


FIG. 10. (Color online) Damaged thickness measured by kinetic *in situ* ellipsometry as a function of plasma exposure time in (a) cw mode and (b) synchronous pulsing mode with 5 kHz and 20% of duty cycle for HBr/O₂/Ar, O₂/Ar, and HBr plasma.

A. Oxidation mechanism through the thin gate oxide

The thin gate oxide growth during the gate patterning overetch step has already been studied in the literature.^{2,10,11,13–15,25}

Morimoto proposed that Si etch by-products get redeposited on the wafer surface and are responsible for an oxide deposition on the wafer.²⁶ Those by-products can come from wafer silicon etching or from the etching of the SiO_xBr_y coating formed on the chamber walls' surfaces during the gate main etch step.¹⁴ In our experimental conditions, no silicon is exposed to the plasma, and the overetch step is performed in clean reactor wall conditions (SF₆/O₂ plasma before the process to recover Al₂O₃/AlF_x clean chamber wall conditions).^{27,28} The only source of silicon is the SiO₂ wafer exposed to the plasma. Since thin SiO₂ is not etched in our process conditions, no redeposition of etch by-products on the SiO₂ surface is expected, and the increase in SiO₂ layer thickness cannot be explained by a deposition phenomenon.

Donnelly *et al.* proposed that O and O⁻ diffusion through the gate oxide as well as oxygen ion implantation is responsible for the oxidation.¹³ Vallier and co-workers reported the

role of hydrogen, which generates an amorphization of the silicon substrate under the thin oxide and can play a role in the oxidation phenomenon.^{2,10} This effect was also confirmed by Ohchi *et al.*, who simulated the penetration of hydrogen ions through the thin gate oxide by molecular dynamics.¹⁵ Vitale and Smith proposed a Deal–Grove-based model using an ion-induced depth-dependent reaction rate constant.¹¹ They also showed that negative oxygen ions are unlikely to play a significant role in silicon oxidation through the thin gate oxide.

To our knowledge, there is no clear understanding of the effect of bromine on the silicon oxidation through the thin gate oxide during the overetch step. Donnelly and Layadi showed on thicker oxides (~6 nm) that bromine is incorporated on the top portion (~2.5 nm) of the oxide,²⁹ which is consistent with the results of Koshino *et al.* that the SiO_xBr_y layer is on the upper surface of a 5 nm thick SiO₂.³⁰

Our experiments performed on thinner oxide (2.5 nm) also show the incorporation of bromine on the upper surface of the SiO₂ film. This bromine uptake is clear in cw plasmas (see Fig. 5), where there is a linear decrease of the Br concentration into the top 2 nm of the surface based on ARXPS results. Using synchronized pulsed plasma conditions, the Br uptake is too low to determine precisely the profile concentration evolution on the top surface. This trend is very similar to Donnelly's data (see Fig. 5 of Ref. 27). Additionally, to the bromine uptake on the first 2 nm of the SiO₂ film, our experimental data also reveal the presence of a significant SiBr_x layer at the interface SiO₂/Si substrate using cw plasma conditions. The presence of this SiBr_x interface layer in our experimental conditions is explained by a thinner SiO₂ layer than in Donnelly's conditions, which enables either the bromine diffusion or direct implantation through the thin SiO₂ layer down to the interface between Si and SiO₂. The presence of the SiBr_x interface layer is directly correlated with the silicon oxidation through the gate oxide, since a 4 nm thick oxidation is measured in cw mode plasma, for which the SiBr_x layer is observable, whereas only 0.8 nm of Si is oxidized through the gate oxide in pulsed plasma conditions, for which no significant SiBr_x interface is observed.

To highlight the impact of HBr on the silicon oxidation through the thin gate oxide during the gate overetch process, a silicon wafer coated with a thin SiO₂ film (2.5 nm) has been exposed to an O₂/Ar plasma (5/150 SCCM) in cw mode and monitored by kinetic ellipsometry. As shown in Fig. 10(a), the silicon oxide thickness increases up to 2 nm after 30 s of plasma exposure. Even if an increase in oxide thickness with a similar trend is observed as in HBr/O₂/Ar plasma (rapid thickness increase in the first few seconds, followed by a constant thickness increase), the final silicon oxidation is much lower in oxygen plasma than in HBr/O₂/Ar plasma, proving the role of hydrogen and/or bromine in the oxidation mechanism through the gate oxide (assuming that the plasma density is in the same order of magnitude in both cases). Moreover, it should be noticed that contrary to HBr/O₂/Ar plasma, using O₂/Ar plasma in syn-

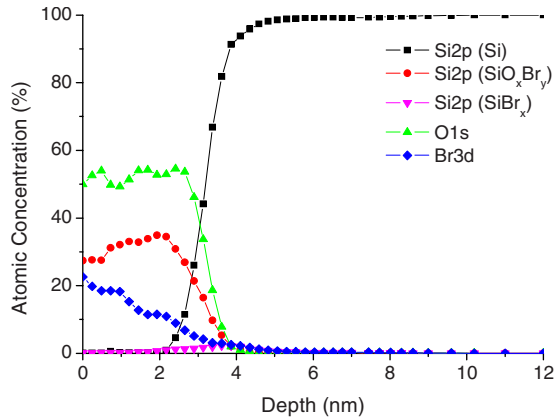


FIG. 11. (Color online) Atomic concentration depth profile of SiO_2 layer exposed to HBr plasma in cw mode.

chronous pulsing mode [Fig. 10(b)] leads to similar silicon oxidation as in cw mode plasma. This trend will be discussed later.

To better determine the role of HBr, a silicon wafer coated with a thin SiO_2 film (2.5 nm) has been exposed to HBr plasma only in cw mode and monitored by kinetic ellipsometry [Fig. 10(a)]. In these conditions, a rapid growth of the gate oxide is measured within the first 10 s (0.9 nm) and the oxide thickness does not change even after 10 s of plasma exposure. In synchronous pulsing mode [Fig. 10(b)], the rapid growth of the gate oxide is minimized to 0.5 nm. XPS analysis in cw mode (not shown here) reveals a Br 3d peak corresponding to 18 at. % of the analyzed surface at 76.25° take-off angle and 10 at. % at 23.75° . The peak for bromine may be decomposed into two peaks at 70.9 and 69.4 eV, which are assigned to Br incorporated into the SiO_2 layer and to Br atoms bonded to Si, respectively. In synchronous pulsing mode, only the 70.9 eV peak is present and corresponds to 8.6 at. % at 76.25° take-off angle and 4.3 at. % at 23.75° .

The depth profile reconstruction presented in Fig. 11 and calculated from ARXPS data after exposure to the HBr plasma in cw mode indicates that Br is more concentrated near the surface and decays to the interface SiO_2/Si .

These experiments demonstrate that the impact of synchronized pulsed plasma on the silicon oxidation is very dependent on the overetch plasma chemistry used.

Finally, a silicon wafer coated with a thin SiO_2 film (2.5 nm) has been exposed to the $\text{HBr}/\text{O}_2/\text{Ar}$ process for 65 s, followed by O_2/Ar plasma in the same operating conditions, without switching off the plasma. Kinetic ellipsometry in Fig. 12 clearly shows a higher oxidation rate during the O_2/Ar exposure after a first exposure to the $\text{HBr}/\text{O}_2/\text{Ar}$ plasma than during the $\text{HBr}/\text{O}_2/\text{Ar}$ step.

Those complementary analyses demonstrate the impact of HBr on the silicon oxidation through the gate oxide. This impact can be explained by the damage to the silicon substrate induced by the hydrogen ions, as demonstrated by Vallier *et al.*¹⁰ and by the impact of bromine incorporation down to the interface and the formation of a SiBr_x interface layer between SiO_2 and Si. This SiBr_x layer may react with oxygen

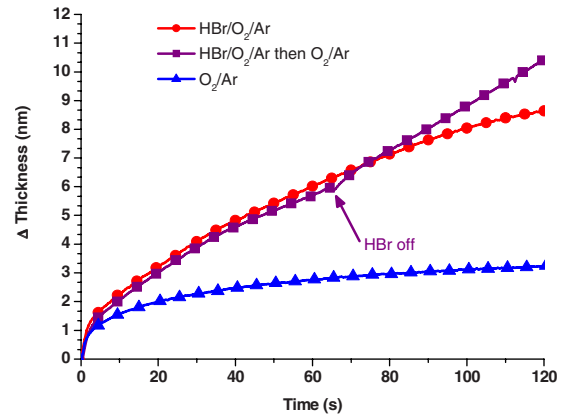


FIG. 12. (Color online) Damaged thickness measured by kinetic *in situ* ellipsometry as a function of plasma exposure time in cw mode during a $\text{HBr}/\text{O}_2/\text{Ar}$ or a O_2/Ar plasma and a $\text{HBr}/\text{O}_2/\text{Ar}$ plasma followed by O_2/Ar plasma.

atoms, which substitute for Br atoms on Si–Br bonds,³¹ favoring the oxidation of silicon at the interface between SiO_2 and Si. Indeed, it is known that most of the bromine incorporated in SiO_2 films exposed to HBr-based plasma desorbs through hydrolysis when the wafer is exposed to moist ambient.²⁴ The high water concentration in $\text{HBr}/\text{O}_2/\text{Ar}$ plasma^{32,33} as well as O radicals from the plasma²⁴ are susceptible to lead to the same oxidation mechanism of the SiBr_x layer through the thin oxide. *Ex situ* XPS analyses (not presented here) of the thin oxide exposed to the cw $\text{HBr}/\text{O}_2/\text{Ar}$ process confirm that less than 1 at. % of bromine remains on the wafer after exposure to the atmosphere. This suppression goes along with a slight variation (<0.8 nm) in thickness of the oxide layer by kinetic ellipsometry. This confirms that the Si–Br interface layer promotes the oxidation of the silicon through the thin oxide during the plasma process or when the wafer is exposed to the moist ambient.

Furthermore, since bromine is a large size atom, a reasonable assumption is that bromine is implanted through the silicon dioxide rather than diffuses through it. It may create significant damage in the SiO_2 layer. This suggests that bromine implantation through the SiO_2 layer may generate a path in the oxide layer facilitating the oxygen and water diffusion down to the SiO_2/Si interface.

In summary, we can say that silicon oxidation through the thin gate oxide is due to a synergetic effect of HBr and O_2 in the plasma. Ions create a diffusion path in the thin oxide, and more particularly H^+ . This leads to a partially amorphized bulk silicon underneath the thin gate oxide. Plasma species can diffuse and/or implant through the thin gate oxide and react with this partially amorphized silicon and more especially bromine, which reacts with silicon and forms a SiBr_x interface layer between the oxide and the bulk silicon. This SiBr_x layer enhances the oxidation by oxygen radicals and water molecules from the plasma and from the atmosphere during air exposure.

B. Impact of synchronized plasma pulsing on oxidation minimization

Our experimental data have shown that synchronous plasma pulsing during the HBr/O₂/Ar overetch process can minimize the plasma induced silicon oxidation through the thin gate oxide. In this case, no SiBr_x interface layer is observed between the SiO₂ and the bulk silicon, and very little bromine is incorporated into the oxide layer.

Based on the oxidation mechanism described above, there are several ways to limit the plasma oxidation through the thin gate oxide:

1. limiting the ion induced diffusion paths in the thin gate oxide
2. limiting the damage to the silicon crystal caused by H⁺ ions
3. limiting the plasma species diffusion and/or implantation
4. limiting the reaction of bromine with silicon at the interface

The first two points are directly related to ion energy, since the penetration depth of ions scales with the energy. By pulsing the plasma, the average ion energy has been reported to be significantly reduced.^{34–36} However, recent time resolved analysis of the ion energy distribution function in synchronous pulsed plasma indicates that the ions' energy during the on time of the plasma is not impacted by pulsing the plasma, that is to say, the instantaneous ion energy during the on time of the pulse is identical to the ions' energy in cw mode (not shown here). During the overetch process, the total on time of the plasma is very close in cw mode and in pulsed plasma, since the etch rate scales with the duty cycle. As a consequence, the dose and energy of the energetic ions (in the on time of the plasma) are very close in pulsed plasma conditions and in cw mode.

On the contrary, the neutrals and ionic compositions are strongly dependent on the pulsing operating conditions. In our conditions, we expect the ratio Br/Br₂ and O/O₂ to depend strongly on the duty cycle since they are controlled by the ratio of the dissociation rate by electron impact divided by the recombination rate of atoms on the reactor walls.^{37–40} While recombination on the surface takes place during the entire plasma period, electron impact dissociation is limited to the on period when energetic electrons are present. Hence, when the duty cycle is reduced, the ratio of atomic to molecular density of bromine and oxygen should decrease. As a consequence, less atomic species are expected to be present in synchronized pulsed plasma conditions than in cw plasmas. This trend has been confirmed by ion mass spectrometry (not shown here). According to the molecular ion implantation theory,⁴¹ the net ion energy is given by Em/M , where E is the energy of the molecular ion, m is the mass of the atom, and M is the total mass of the molecule. As a consequence, in synchronized pulsed plasmas with polyatomic ions, the net energy of the energetic atoms reaching the surface is much less than the energy of the atoms issued from monoatomic ions reaching the surface in cw mode. For example, the net energy of hydrogen atoms reaching the sur-

face as a H₂O⁺ molecular ion with a given energy is only 1/18 (less than 6%) of the energy of a H⁺ atomic ion reaching the surface with the same given energy. As a consequence, the penetration depth and damage to the silicon caused by ions from less dissociated/more recombined plasmas are expected to be strongly limited, compared to the penetration depth and damage to the silicon caused by monoatomic ions with the same energy from a highly dissociated plasma. Thus, the ion induced diffusion paths in the thin gate oxide and the damage to the silicon crystal caused by H⁺ ions are strongly limited in HBr/O₂/Ar pulsed plasma conditions.

This phenomenon is expected to play an important role in the minimization of the plasma induced oxidation through the thin gate oxide by pulsing the HBr/O₂/Ar gate overetch plasma.

The second two points (limiting the plasma species diffusion and/or implantation and limiting the reaction of bromine with silicon at the interface) are also affected by decreasing the plasma dissociation. Indeed, neutrals in the plasma depend on the plasma dissociation. For more dissociated plasmas (cw), smaller and more reactive species (e.g., O or Br radicals rather than O₂ or Br₂) are available. Due to their smaller size, they are more prone to diffuse through the thin gate oxide than molecules issued from recombination (e.g., Br₂). Furthermore, Br radicals are more susceptible to react with silicon to create the SiBr_x interface than less reactive Br₂ molecules. As a consequence, less dissociated plasmas are expected to lead to less species diffusion and less reactions at the silicon interface, which should limit the silicon oxidation through the thin gate oxide. As explained earlier, pulsed plasmas are known to be much less dissociated than cw plasmas, which should limit the plasma induced oxidation of silicon through the gate.

This phenomenon is also expected to play an important role in the minimization of the plasma induced oxidation through the thin gate oxide by pulsing the HBr/O₂/Ar gate overetch plasma. However, the fact that Ar/O₂ synchronized pulsed plasmas lead to similar silicon oxidation than Ar/O₂ plasma in cw mode (Fig. 10) suggests that modifying the O/O₂ dissociation ratio by plasma pulsing has no significant impact on the oxidation mechanisms and that the reaction is not limited by the atomic oxygen concentration.

Besides, a mechanism of reconstruction of the silicon oxide during the off time of the plasma is also possible. Ion induced damage during the on time could be repaired by diffusion of oxygen and substitution of Br by O during the off time. This may block the diffusion paths and contribute to restrict the diffusion of species toward interface

In summary, we propose that the reduction of silicon oxidation through the thin gate oxide by synchronously pulsing the plasma is attributed to a decrease of the plasma dissociation. Molecular ions are less prone to create plasma induced damage into the thin gate oxide and to disturb the silicon crystal. Molecular neutrals are larger and less reactive than atomic radicals and, as a consequence, they cannot diffuse through the thin gate oxide and react with the silicon sub-

strate as much as atomic species. Plasma dissociation is decreased by synchronously pulsing the plasma, and less dissociated plasmas are obtained at low duty cycles, which explains that pulsed plasma with small duty cycles lead to less oxidation of the bulk silicon through the thin gate oxide.

V. CONCLUSION

Silicon loss from the active region of the transistor is inevitable with conventional plasma etching of the polysilicon gate and has a significant effect on transistor performance. It originates from the removal during wet cleans of the plasma induced oxidized layer below the thin gate oxide.

The plasma induced oxidation through the thin gate oxide is attributed to the creation of a diffusion path by energetic ions, the amorphization of the silicon crystal underneath the thin oxide by energetic protons, and the diffusion and/or implantation of plasma species through the thin oxide, particularly Br, which reacts with silicon and creates a SiBr_x interface layer promoting the oxidation by oxygen and water.

To minimize this Si recess, we have investigated the possibility of pulsing HBr/O₂/Ar plasmas for gate etch applications. Using synchronous pulsed plasmas, we have shown that the damaged layer thickness can be reduced from 4 nm in cw mode down to 0.8 nm at high pulsing frequency (5 kHz) and low duty cycle (20%). This decrease is attributed to a decrease of plasma dissociation by pulsing the plasma. Less dissociated plasmas have a larger ratio of molecules over atomic species, which leads to less ion induced damage and less species diffusion through the thin gate oxide. Those results demonstrate the interest of synchronous plasma pulsing for improving plasma etch processes.

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