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Abstract: The design of static power converters makes intervene an important number of variables as well as several different kinds of constraints.
The goal of this work consists in introducing the EMI constraint at the time of the power electronic circuit's design while leading an accurate analysis of the conducted sources of perturbations. The developed models aim to improve the realism of the power components simulation in the goal to optimize the design while dealing with EMI constraints.

Index terms: VHDL-AMS models, EMI constraint, Power components simulations.

NOMENCLATURE

- Ads: Body region area [m^2].
- ε_{si} : Silicon permittivity [F/m].
- $V_{Td:}$ Gate-drain overlaps depletion threshold voltage [V].
- Wdsj: Drain-source depletion width [m].
- Cgdj: Gate-drain overlaps depletion capacitance [F].
- Coxd: Gate-drain overlap oxide capacitance [F].
- Coxs: Exceeding oxide capacity [F].
- Cm: Source metallization capacity [F].
- Ibss: Steady-state base current [A].
- Icss: Steady-state collector current [A].
- Iccer : Collector-emitter redistribution current [A].
- Iceb: Emitter-base capacitor current [A].
- W: Quasi-neutral base width [m].
- q: Electronic charge [C].
- A: Device active area [m^2].
- μ_{eff}: Effective mobility [$m^2.V^{-1}.s^{-1}$].
- n_{eff} : Effective base doping concentration [m^{-3}].
- Ip_{ij}: Positive charge current between the ij nodes [A].
- Vij: The potential between the ij nodes [V].

I. INTRODUCTION

The consideration of the aspects linked to the EMI when simulating the power electronic system requires the modeling of the whole system in its real environment. Indeed, modeling must take into account on one hand the internal coupling between the different elements of the system (parasitic elements of the components, wirings and links impedances) and on the other hand, the coupling between the system and its vicinity (conducted and radiated coupling modes).

However, a particular effort must be provided to propose models for the semiconductor components enabling an accurate simulation of the switchings since they represents the main sources of high di/dt and dv/dt leading to perturbations in the converters. The used models must be valid in a large frequency range, in order to get a realistic spectral representation of the currents and voltages.

Actually, this survey aims to introduce the EMC constraint at the circuit conception time. In fact, a sensitivity study on the design parameters would permit to identify those acting directly on the radiated and conduced emissions in order to intervene at the virtual prototyping stage to insure that the EMC aspect is respected.

In this work, we propose a first version of the dynamic IGBT model in VHDL-AMS. The IGBT referenced IRGPC40UD is chosen to establish the model. It

integrates an N-channel IGBT chip as well as a fast recovery anti-parallel diode. The complete model will be implemented in a DC-DC converter circuit and used subsequently to lead a parameters sensitivity analysis of the model by observing the evolution of the conduced EMI at the LISN (Line Impedance Stabilization Network).

II. LUMPED-CHARGE DIODE MODEL IN VHDL-AMS

The lumped-charge LC modeling technique represents a systematic approach for the development of power semiconductor models of which we find several applications in the literature [12][13]. We referred for this work to the Laurizen-Ma diode model [14]. This model, based on a physical approach, is developed to replace the SPICE standard model in order to have a better representation of the inverse recovery effect.

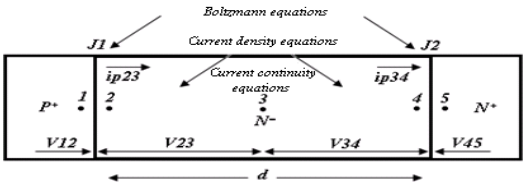

Figure 1: The LC nodes distribution in a 1-D P+N-N+ diode structure [14]

Thanks to this technique, the basic semiconductor equations are simplified while using this node arrangement (Figure 1). These relations are transformed in lumped-charge equations for every region. With regard to the VHDL-AMS diode model, we leaned on the described models in [15] used on SABER simulator.

The test circuit presented in figure 2 is used to analyze the diode model. According to the literature [18], the method consists in analyzing the inverse transient characteristic of the diode from a null forward current.

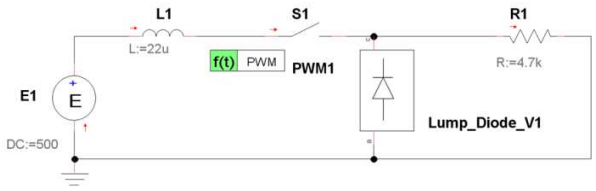

Figure 2: Simulation circuit of the inverse recovery from a null initial current

In spite of resistance R1 influences on the value of the maximal inverse voltage VRM (Figure 3), it doesn't affect its variation. On the other hand, the current slope (Figure 4) depends essentially of the applied inverse tension and of the inductance L1 permitting to impose the current gradient.

In the absence of initial current, the diode behaves like a non-linear capacitance. The internal diode capacitance discharges through the resistance and the inductance of the circuit generates an oscillation.

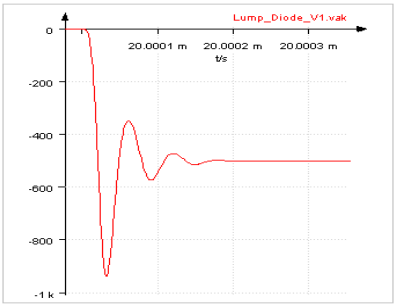

Figure 3: The voltage behavior at the reverse recovery instance

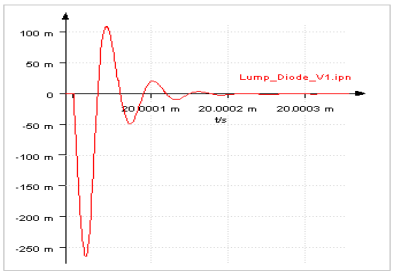

Figure 4: The inverse current behavior

III. IGBT MODELING

In spite of the recent efforts toward an IGBT behavioral modeling to avoid the physical models complexity, the understanding of the internal mechanisms proves to be even indispensable to really define the model relevance. In fact, the Hefner model is classified among the first models that takes into account the important physical modeling effects. It is the basis of several behavioral models, notably those elaborated for Spice [1][2].

This first complete model with charge control [3] shows excellent results in literature. These results were the subject of the simulations described in document [4]. To describe the injection operation done at the level of the large PNP transistor base, the theory of ambipolar diffusion [5] is used instead of conventional quasi-static approach to describe the transient behavior and the transportation of electrons and holes [6]. For these IGBT modeling works, we lean upon the Hefner model [6] and on the VHDL-AMS modeling works in literature [7].

III.1.ELECTRICAL MODEL OF THE IGBT IN VHDL-AMS

The IGBT and the VDMOSFET structures are quite identical; the main difference is that the IGBT substratum is of P+ type. In fact, these two components have the same grid structure, the source contact (for the IGBT is called cathode or emitter) is done as much on the N+ area as on the P zone. This zone has two doping levels (high doped at the volume level and low doped at the canal level) in order to guarantee a reasonable threshold voltage and a low resistivity to avoid the booting of the parasitic bipolar N+PN-[8].

Nevertheless, the physical functioning of the IGBT is closer to the bipolar transistor functioning then the VDMOSFET. Indeed, the presence of the P+ substratum permits the injection of minority carriers (holes) in the N- layer, this generates a modulation of its conductivity and induced to the reduction of its conduction resistance.

III.2.VDMOSFET CHARACTERISTICS

Figure (5) shows the VDMOSFET capacitive elements. The Cgd capacitance is equal to the oxide capacitance Coxd at the level of the grid-drain overlap for $Vds \leq Vgs - V_{Td}$, for except that for $Vds \geq Vgs - V_{Td}$, the silicon that is below the grid becomes depletive and the Cgd capacitance will be constituted by a serial recombination of the Coxd capacitance and the depletion capacitance Cgdj at the level of the grid-drain overlap.

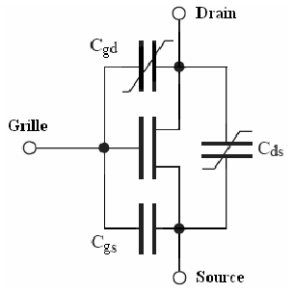

Figure 5: VDMOSFET capacitive elements

The sum of the oxide capacitance Coxs at the level of the grid-source overlap and the source metallization capacitance Cm forms the grid-source capacitance Cgs. The depletion capacitance of the drain-source junction Cds is given by:

$$Cds = \frac{Ads \times \varepsilon_{si}}{Wdsj} \quad (1)$$

III.3.THE BIPOLAR TRANSISTOR CHARACTERISTICS

Contrary to the conventional bipolar transistor, the base length is not anymore too small in relation to the diffusion length of its minority carriers. Thus, the transistor is separated to a collector/anode-base junction, a base-emitter/cathode junction and a resistive base Rb [3]. This resistance is imposed like a critical element that must essentially takes into account the current lines focusing mechanism and the base conductivity modulation [9]. It is expressed by the following equation:

$$Rb = \frac{W}{q \times A \times \mu_{eff} \times n_{eff}} \quad (2)$$

The Ic current crossing the collector/anode-base junction corresponds to the sum of two currents. The recombination capacity Ccer is an important element that describes the recombination effect when IGBT current is cut off.

Indeed, the decrease rate of the tail current correspond to the evacuation by recombination of the majority carriers stocked in the N- base [10][11]. Contrary to the Iccer current that browses this capacitance, the representation of the stationary current Icss doesn't depend on the variations of the base-emitter/cathode potential.

On the other hand, the base-emitter/cathode junction is represented as a current source Ibss set in parallel with the Iceb current. These currents symbolize the evacuation of the transistor charge.

The equivalent diagram used for the IGBT modeling in VHDL-AMS is detailed on figure 6.

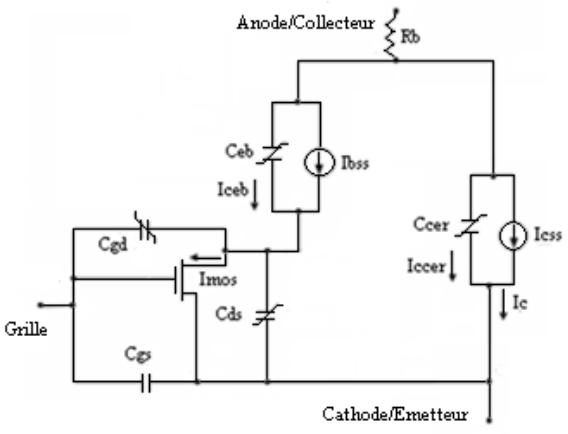

Figure 6: Equivalent circuit model of the IGBT

IV. SIMULATION CIRCUIT TOPOLOGY: BUCK CONVERTER

The IRG4PC40UD diode has the features of a power diode (600V,15A) and it is designed for bridge configuration. The major advantage of this diode is its speed and its weak losses. The IGBT and the diode modeling can be achieved in an independent way since they represent two detached components in the same package [16] and it allows us to use the already defined models of the IGBT and the diode.

The parameters identification proceeds of two main stages [7]:

- The extraction of the initial parameters: it is based, on one hand, on the manufacturer technical files (Datasheet) and the analytic equations and on the other hand on static or dynamic measurements.

- The adjustment of the parameters by an optimization approach permitting to minimize the differences between the experimentations and simulations.

At the first phase of work, we use the manufacturer's technical files as a basis [16][17] to define the model parameters.

The different simulations of this model are achieved on the Portunus® software. In order to evaluate the dynamic behavior of the model, we used a DC-DC converter circuit presented in figure 7. The switching cell is constituted of an IRG4PC40UD IGBT model (commanded by the control supply E1 (grid tension included between 0V and 15V for switching frequency of 40 KHz), a freewheeling diode model identical to that used in the IRG4PC40UD. The circuit also integrates a 500V supply E2, a grid resistance Rg of 100 Ω, a load that is constituted by a resistance Rch of 100 Ω and an inductance Lch of 1mH as well as the circuit parasitic elements. These values have been estimated on a real prototype.

A LISN circuit has been inserted between the supply and the converter in order to calculate the conduced EMI generated by the circuit in both common and differential modes.

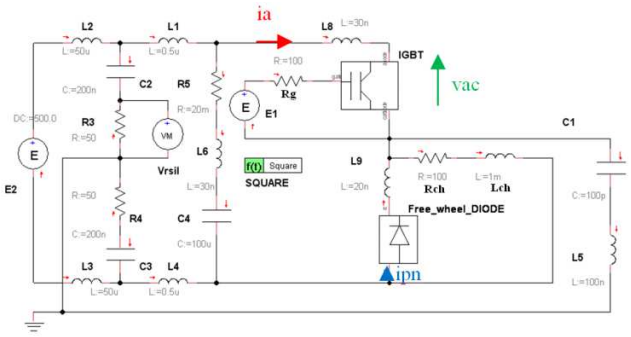

Figure 7: Switching circuit

V. SEMICONDUCTORS SWITCHING AND CONDUCTED EMI SIMULATION

The IGBT switching off (Figure 8) follows the same process that of the MOS. The current decreases suddenly since the MOS opens up and the major part of the current is cut. When the Vac voltage reaches the supply voltages, the free wheel diode in unblocked. On the other hand, a tail current persists until the complete recombination. This current is due to the excess in carriers that are not evacuated from the base of the PNP transistor.

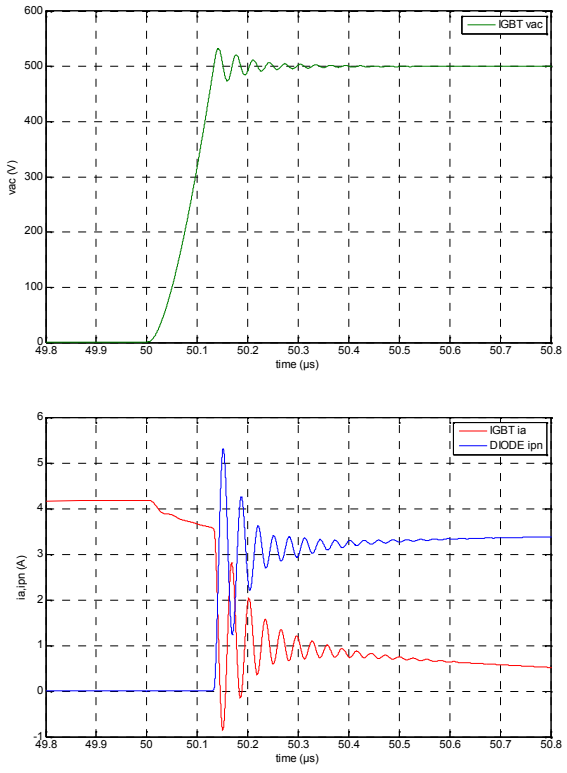

Figure 8: IGBT switching off and free wheel phase

The IGBT switching on (Figure 9) is practically identical to a MOS. Actually, when the grid voltage reaches the threshold voltage, the current increases in the IGBT. We notice that the increase of the IGBT current is made with the same slope that in the free wheel diode that continues to conduct as far as reaching the maximal current IRM.

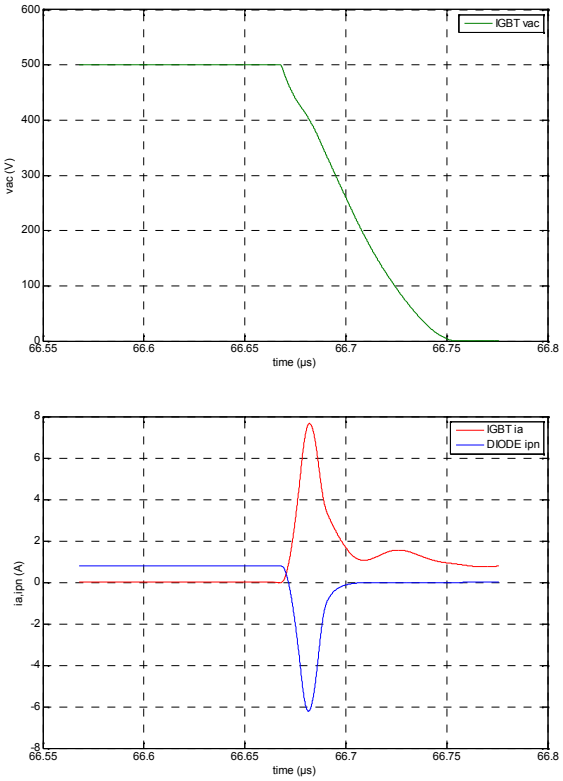

Figure 9: IGBT switching on and the inverse recovery phase

After this temporal simulation, conduced EMI versus time are extracted from the LISN. A simple Fast Fourier Transformation (FFT) calculation of these voltages allows us to deduce the EMI spectrum. Figure 10 shows the spectrum of the Vrsil voltage extracted from the LISN in which we can observe that the peaks are mainly due to the ringings caused by the switching of the non-linear components (The IGBT and the diode).

The simulation has been achieved for two different values of the load current and for two values of the grid resistance Rg. The influence of both parameters is clearly situated over 5 MHz. The dominant role of Rg can be observed.

This survey allow us to show the considerable influence of semiconductors on electromagnetic interferences generated by the switching and in another step to study the influence of model parameters and their accuracy to allow EMC analysis.

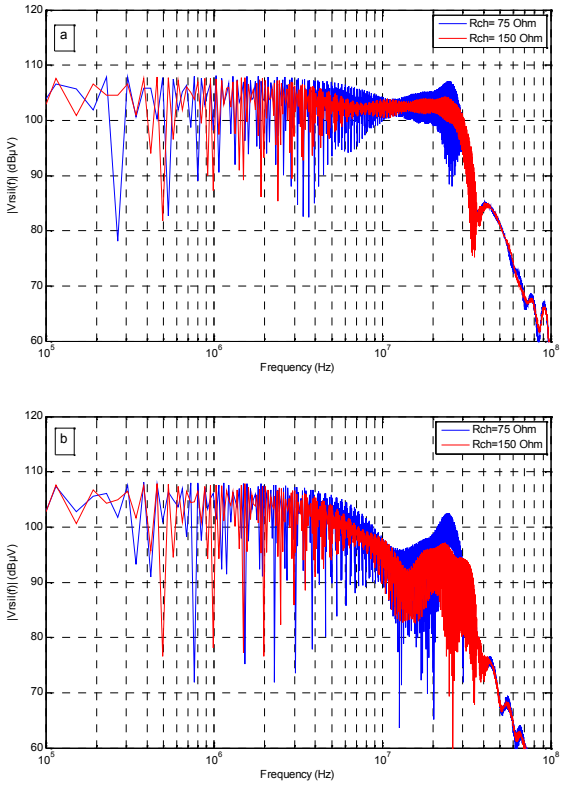

Figure 10: Vrsil spectral representation Lch=100µH (a)Rg=30Ω, (b)Rg=100Ω

VI. CONCLUSION AND PERSPECTIVES

The EMI analysis of the power electronics at the conception stage and at the time of the virtual prototyping requires the use of accurate models for the semiconductor components. These models require an important number of parameters whose exact knowledge often requires experimental measurements and optimization procedures.

The behavior in changing and steady state varies considerably according to the type of used semiconductor switch. As a fact, the circuit simulation type seems to be an indispensable stage facing a general characterization by means of measurements as the field cartography. This method allows defining the elements that mainly contribute to the resonances but requires exact models for the calculation of the electromagnetic perturbations.

Once the correct modeling is achieved, studying the distribution of the cables and the components in the chopper block is essential to evaluate the influence of the parasitic elements on the efficiency of the supplementary circuit (of filtering, of commutation help…) in order to lead a complete EMC analysis.

At this phase, we studied a VHDL-AMS primitive model of the IGBT on the Portunus® software. This work is the result of a deepened survey of the physics and the internal structure of the semiconductors. On the other hand, the implementation of the models in a chopper circuit allows us to simulate the conduced EMI generated by the circuit. Further study will combines these two aspects in order to find more precise relations between the physical models parameter and the conduced EMI. The validations of the proposed model in relation to experimental measurements are necessary at this stage. This first phase of modeling must be applied also to passive devices and to connectors that contribute inevitably to the electromagnetic signature of power devices.

VII. ACKNOWLEDGMENTS

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