A 2GHz 65nm CMOS digitally-tuned BAW oscillator

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Abstract— **The design of a 2GHz reference frequency oscillator in a 65nm CMOS process using a Bulk Acoustic Wave resonator is presented. The oscillator implements digital frequency control using a switched capacitor bank in parallel to the resonator. The tuning range is up to 4MHz with a minimum step of 1.6kHz. The oscillator core is designed to reach low phase noise (-128dBc/Hz at 100kHz offset) at low power consumption (0.9mW) using a differential topology. It is followed by a low noise divider for output at 500MHz with a phase noise of -140dBc/Hz at 100kHz offset.**

I. INTRODUCTION

Wireless communication systems require reference frequency oscillators for synchronization purpose. Conventional frequency references are commonly based on crystal oscillators. They have a high spectral purity but operate at low frequency (26MHz). In addition, a crystal is a rather expensive and is a bulky component that is difficult to integrate in the same package as the RF transceiver. An alternative to crystals can be to use Bulk Acoustic Wave (BAW) resonators. Thanks to their high quality factor and their high resonant frequency in the GHz range, RF oscillators with spectral purity equivalent to crystal oscillators can be achieved [1]. An advantage of BAW resonators is their small size, which, in the future, enables their integration into a single package together with the transceiver and into a single chip radio. In addition to spectral purity, frequency stability is another important concern when considering a reference frequency application. Frequency stability is to a large extent determined by the properties of the resonator. Therefore this question is not directly addressed in this paper where the focus is on the design of the oscillator. However, it is important that the oscillator design provides means for tuning the frequency to the desired value with a high degree of precision and over a frequency range that enables correction of the largest frequency errors.

In this paper, we report a digitally frequency-controlled BAW-based oscillator at 2GHz designed in an advanced 65nm CMOS process. The oscillator has a tuning range of 4MHz with a minimum step of 1.6kHz or 0.8ppm. The targeted application is a reference oscillator. The paper is organized as follows. In section II, a theoretical analysis of the BAW oscillator is presented that illustrates the main design challenges. In section III, the architectures of the oscillator and of the tuning bank are described. Finally, simulation results and comparisons to earlier works are reported in section IV.

II. BAW OSCILLATOR ANALYSIS

A. Solid Mounted Resonator (SMR)

A BAW resonator consists basically of a piezoelectric layer enclosed between two electrodes. By application of a RF signal on the electrodes, an acoustic wave is excited within the piezoelectric layer. Resonance occurs at a frequency determined by the thickness of the layer. In order to achieve a high quality factor, the wave is confined within the piezoelectric layer by reflectors. In thin film bulk acoustic resonator (FBAR) technology, the reflector is simply air. In solid mounted resonator (SMR) technology, a Bragg reflector is used at the bottom side of the piezoelectric layer (Fig.1). The main application of FBAR and SMR technologies today is the fabrication of RF filters [2].
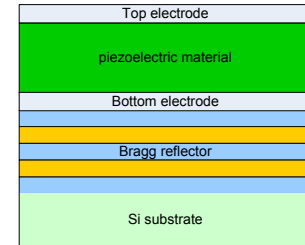

Fig. 1. Solid mounted resonator schematic cross section

In the present work, a SMR is used. An appropriate resonator model for simulation purpose is the modified Butterworth-Van Dyke equivalent circuit presented in Fig.2 [3][4]. The parameters of this model are R_m, C_m and L_m, respectively the acoustic resistor, capacitor and inductor, C_e the capacitor between the two electrodes and R_e the resistance of the electrodes. From the circuit model, we define other important parameters of the resonator as follows:

- The motional frequency:

$$f_m = 1/\left(2\pi\sqrt{L_m C_m}\right), \qquad (1)$$

- The motional quality factor:

$$Q_m = 1/\left(2\pi f_m R_m C_m\right), \qquad (2)$$

- The coupling factor which models the electro-acoustic interaction:

$$k = \sqrt{C_m/C_e}. \tag{3}$$

B. Oscillator modeling

The oscillator is decomposed into two parts for the purpose of the analysis: the active part and the resonator (Fig.2). The active part is modeled by its equivalent admittance, consisting of a negative conductance G_{osc} for compensation of resistive loss into the resonator, and of a capacitance C_{osc}. The variable capacitance C_t modeling the capacitor bank is included into the resonator part.
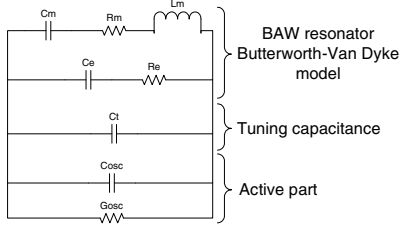

Fig. 2. Oscillator simplified model

If we denote $Y_{resonator} = G_{resonator} + j \cdot B_{resonator}$ the admittance of the resonator, and $Y_{osc} = G_{osc} + j \cdot B_{osc}$ that of the active circuit, the oscillation frequency f_{osc} is defined by:

$$B_{osc}(f_{osc}) + B_{resonator}(f_{osc}) = 0 \tag{4}$$

and the Barkhausen oscillation startup conditions at the oscillation frequency are:

$$G_{osc}(f_{osc}) + G_{resonator}(f_{osc}) < 0. \tag{5}$$

For analysis purpose, let us now define the following additional parameters:

- the effective coupling factor:

$$k' = \sqrt{C_m/(C_e + C_t + Cosc)} = \sqrt{C_m/C_p}, \tag{6}$$

- the parallel resonant frequency of the system, which is the potential oscillation frequency:

$$f'_p = f_m \times \sqrt{(C_p + C_m)/C_p} \approx f_m \times \sqrt{1 + k'^2}, \tag{7}$$

- the conductance of the oscillator at the oscillation frequency f'_p:

$$G_m = \frac{1}{R_m + R_m Q_m^2 k'^4/(1 + k'^2)}. \tag{8}$$

C. Frequency tuning

Compared to crystals used in reference frequency applications (for instance the CX-3225SB), BAW resonators have a poor frequency accuracy. The consequence is that a relatively wide tuning range is required to correct for frequency errors. From a study of the frequency dispersion of the BAW resonator, we concluded that a tuning range of about ± 1000ppm was necessary. As noticeable from equations (6) and (7),

frequency tuning by variation of capacitance C_t has the effect of changing the effective coupling factor k'. This is illustrated by Fig.3 that shows the normalized oscillation frequency as a function of k'. When increasing capacitance C_t, both the coupling factor k' and the oscillation frequency decrease. The frequency range is bounded by two limits. First, the effective coupling factor cannot be higher than the physical coupling factor of the BAW resonator, which is determined by the process. This sets the upper limit of the tuning range. The lower limit is related to equation (8), which indicates that the oscillator conductance increases rapidly when k' decreases, i.e. when frequency decreases. At a certain point, the impedance becomes so low that startup conditions are not met anymore.
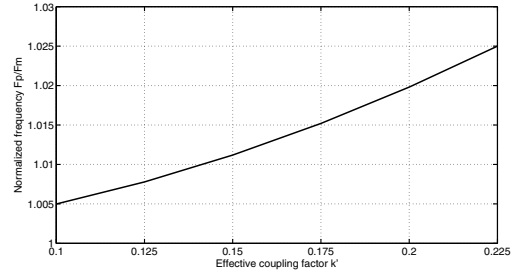

Fig. 3. Normalized frequency versus effective coupling factor

III. OSCILLATOR DESIGN

A. Topology considerations

The oscillator is designed for a resonator with a parallel resonant frequency of 2GHz, a quality factor Q_m=1000 and a coupling factor k=1.7. We selected the so-called cross-coupled NMOS differential topology in order to obtain high negative conductance and differential outputs [5]. The BAW resonator is placed between drains of the NMOS pair. Each branch of the active NMOS pair is supplied independently by a current source. So as to minimize frequency pushing and achieve high frequency stability with temperature, the supply current is stabilized relatively to supply voltage and temperature variations. In order to assess the minimum output power required for oscillator startup, we implemented a current source programmable by steps of 250μA from 250μA to 2mA. When varying the supply current, resistors at the bottom of the differential pair are switched to keep the DC common output voltage constant over the current range (Fig.4). At DC the BAW resonator and the current source show high load impedance to the cross-coupled NMOS pair. In order to prevent a latch effect in the cross-coupled pair, positive feedback in the cross-coupled pair is suppressed at low frequencies by a high-pass filter [6][7].

Current communication systems do not yet use frequency references at 2GHz. In order to measure the oscillator performances in operational conditions, we included a divider by four and a buffer. The divider has a classical D-flip-flop architecture [5]. A buffer amplifier was added following the divider for measurement purpose of the output signal into a

50Ω impedance system. Both the frequency divider and the buffer are supplied by a low drop out voltage regulator (LDO).
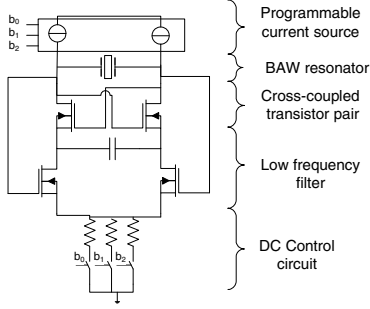

Fig. 4.   Oscillator core

B. Frequency tuning

The need for frequency tuning was discussed in section II-C. A solution to implement this tuning is to realize a capacitor bank. Let us consider the bank specifications we need. The frequency uncertainty depends on four main factors:

- the initial BAW resonator error,
- the frequency drift with temperature variation,
- the frequency drift with voltage variation,
- the frequency drift with aging.

A tuning range of ± 1024ppm is needed to correct these four drifts according to our calculations. The frequency step of the capacitor bank is limited by the technology. This leads us to the selection of 0.8ppm minimum frequency accuracy. To reach this small step, we decided to implement a specific fringe capacitance available in advanced CMOS technology. This takes advantage of the parasitic capacitance between two metal fingers. The main principle and model are given on Fig.5. The switched capacitance has two states:

- in the off state,

$$C_{AB}^{off} = (C_0 + C_2)/2, \qquad (9)$$

- in the on state,

$$C_{AB}^{on} = \left(C_2 + \frac{C_0 \cdot (2 \cdot C_6 + C_1)}{C_0 + 2 \cdot C_6 + C_1}\right)/2. \qquad (10)$$

In the off state, a parasitic capacitance still remains which limits the tuning range. We have to find a trade-off between the step capacitance, $\Delta C_p = \Delta C_t = C_{AB}^{on} - C_{AB}^{off}$, and the parasitic capacitance C_{AB}^{off}. These two parameters induce the frequency step of the bank given by (7). With this in mind, we choose $C_{AB}^{on} = 1.2 \cdot C_{AB}^{off}$, corresponding to a parasitic capacitor of 310aF and a step capacitance of 64aF for a 0.8ppm accuracy. Two capacitor banks are implemented to minimize the global parasitic capacitance. The first one, called coarse bank, is dedicated to the correction of the initial error due to the BAW resonator caused by process variations. Nominally, this bank enables to correct frequency errors up
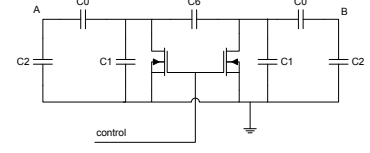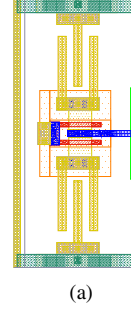
to ± 1024ppm. The second one, called fine bank, gives a nominal tuning range capability of ± 102.4ppm. It has to cope with frequency variations that can occur while the frequency reference is running. To avoid any frequency dead zone, an overlap between the two banks is introduced as presented in Fig.6. Since the frequency step of the coarse bank should be low enough to fulfill this requirement, we choose a nominal step of 64ppm. In order to lower the differential non linearity (DNL) and the integral non linearity (INL) of the two banks, a thermometric code is implemented.
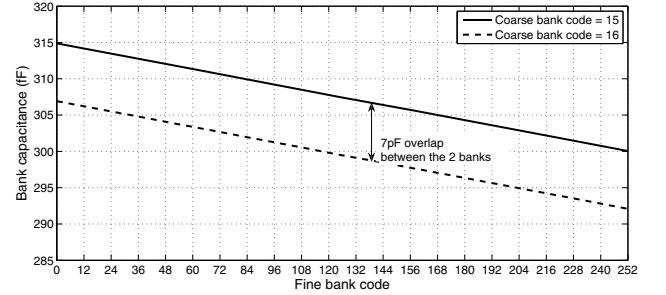

Fig. 6.   Overlap between the fine and the coarse banks for coarse bank codes 15 and 16

Fig. 5.   Fringe capacitance layout and electrical model including parasitics (C_1, C_2, C_6)

TABLE I

SUMMARY OF THE CAPACITOR BANKS PERFORMANCES

	Frequency		ΔC_t
Coarse bank tuning range	± 1024 ppm	± 2 MHz	± 128 fF
Coarse bank tuning step	64 ppm	132 kHz	8 fF
Fine bank tuning range	± 102.4 ppm	± 200 kHz	± 8.16 fF
Fine bank tuning step	0.8 ppm	1.6 kHz	64 aF

C. The circuit

The complete circuit includes the oscillator core (see Fig.4), a programmable current source, two capacitor banks with their decoder and a dedicated LDO, a divider by four and a pre-buffer with a dedicated LDO, a 500MHz 50Ω matched output
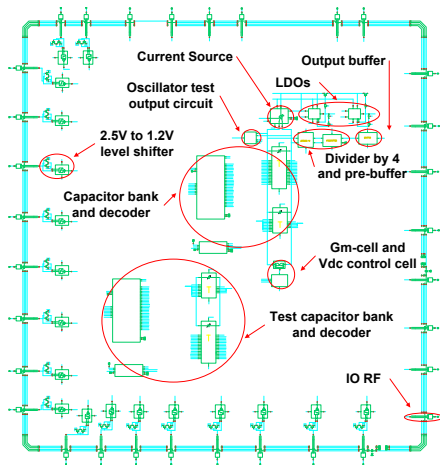
Fig. 7.   Topcell schematic of the circuit

buffer and, finally, a 2GHz test output. The global circuit arrangement is presented in Fig. 7.

IV. SIMULATION RESULTS

All the blocks were individually specified and simulated. The simulations have been carried out in process corners, over voltage and temperature ranges, and took into account layout parasites. This section presents the results of the circuit. The oscillator start-up conditions (4) and (5) were checked using AC analyses. The simulation results show that the ratio between the negative conductance created by the active circuit and the BAW resonator conductance is always higher than 2 which ensure the oscillation startup. A BAW and a crystal oscillator can be compared with regard to their phase noise. A 26MHz crystal oscillator phase noise is specified to be better than -135dBc/Hz at 10kHz offset from the carrier for cellular systems. To take into account the working frequency difference between the two oscillators a correction factor has to be applied. In our case, the circuit output signal frequency is 500MHz. The correction factor is $20 \times \log(500/26) = 26dB$. Therefore, the equivalent phase noise required of the crystal oscillator would be $L\left(f_m\right) = -135 + 26 = -109 dBc/Hz @ 500 MHz$. The simulated phase

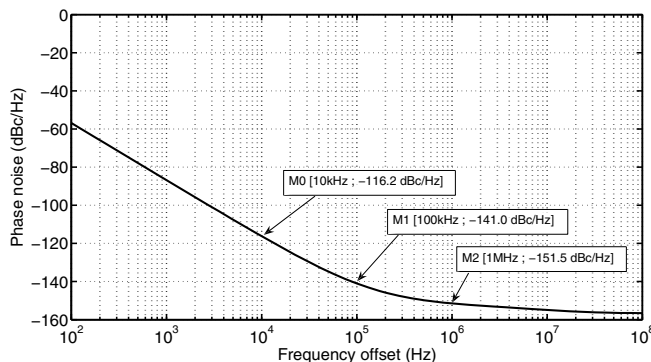Fig. 8.   Phase noise at 500MHz

noise of the BAW oscillator at 10kHz offset is -116dBc/Hz which is better than the -109dBc/Hz required, see Fig. 8.

The comparison with recent work given in Table II shows the relevance of our work.

TABLE II

BAW OSCILLATORS COMPARISON

Paper	type	Fosc (GHz)	Power (mW)	Phase noise at 2GHz (dBc/Hz)	Techno
[8]	Pierce (single)	1.9	0.3	-112@10kHz	BiCMOS
[1]	Butler (single)	2	4	-120@100kHz	BiCMOS
[9]	Colpitts (single)	2	6.8	-118@100kHz	SiGe BiCMOS
[6]	diff.	2.1	0.6	-122@100kHz	CMOS 0.13μm
This work	diff.	2	0.9	-128@100kHz	CMOS 65nm

V. CONCLUSION

We implemented a new digitally-tuned BAW based frequency reference in a 65nm CMOS process. A high spectral purity (-128dBc/Hz before the divider and -141dBc/Hz after at 100kHz from the carrier frequency) has been shown. Low power consumption (0.9mW) has been reached. We designed a digitally controlled capacitor bank enabling a 4MHz frequency tuning range with a 1.6kHz step using small fringe capacitors. The 200Hz step (0.1ppm) required for GSM/3G applications can be achieved with the bank control. As discussed above, these new oscillator key features bring possibilities to substitute it to crystal oscillators. This will be confirmed after full characterization of the circuit under manufacturing.

ACKNOWLEDGMENTS

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