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# Formation of Submicrometer Pore Arrays by Electrochemical Etching of Silicon and Nanoimprint Lithography

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This work describes the formation of submicrometer pore arrays using nanoimprint lithography and photoelectrochemical etching of n-type silicon in a hydrofluoric acid electrolyte. This work highlights more specifically the link between silicon resistivity and pore geometry. A properly chosen silicon resistivity is shown to ensure a stable pore growth and to limit damages in pore walls due to electrical breakdown and photogenerated carrier diffusion. Well ordered pore arrays with a depth up to 20  $\mu\text{m}$  and a period of 1  $\mu\text{m}$ , 750 nm, and 500 nm have been fabricated using silicon wafers with resistivities of 0.76, 0.35, and 0.15  $\Omega\text{ cm}$ , respectively.

Electrochemical etching (EE) of n-type silicon has only been thoroughly studied since the 1990s as a deep etching technique.<sup>1</sup> This process enables the formation of high aspect ratio microstructures (pores, trenches, pillars, tubes, etc.).<sup>2-4</sup> This etching is cost effective and allows one to obtain better surface roughness compared to deep reactive ion etching<sup>5</sup> as there is no scalloping effect. The aspect ratio can reach 200, and the width of the structure can be easily modulated in the growth direction.<sup>6</sup>

This technique has, however, mostly been studied for the fabrication of pore arrays in the micrometer range.<sup>7-9</sup> The current development of silicon nanodevices sometimes requires integrating pore arrays with higher densities. For instance, 500 nm pore arrays are necessary to confine light within the wavelength ranges applicable to telecommunications.<sup>10</sup> These arrays possess high interfacial surface area and are also very desirable in the fields of micro/nanofluidic membrane fabrication<sup>11,12</sup> and in the development of supercapacities in microelectronics.<sup>13</sup>

Current research is mainly focused on the fabrication of structures with nontubular pore geometry by the modulation of etching parameters during anodization.<sup>6</sup> To our knowledge, only few papers have showed successful fabrication of pore arrays with periods of  $<1\ \mu\text{m}$ ,<sup>10,14</sup> and the smallest period of the submicrometer structure up to date is 500 nm. However, the details of the etching conditions are not clear.<sup>10</sup> The lack of data concerning electrochemical etching in the submicrometer range may be accounted for, first and foremost, by the difficulty of access to nanolithography technology. Indeed, UV photolithography is mainly used in academic laboratories because high resolution techniques require expensive (e.g., deep UV steppers) or time consuming equipments (e.g., E-beam lithography). A second restriction is related to the difficulty of etching pores with diameters  $<1\ \mu\text{m}$ . Indeed, Lehmann has experimentally observed that the pore diameter is linked to the resistivity used.<sup>15</sup> So, the formation of submicrometer pores typically requires the use of a  $<1\ \Omega\text{ cm}$  resistivity. This has the effect of favoring electrical breakdown phenomena in the walls and hence to degrade their quality. Indeed, electrical breakdown phenomena lead to the formation of transversal pores in the  $\langle 100 \rangle$  direction.<sup>1</sup> Thus, the formation of submicrometer pores requires choosing the silicon resistivity with great care in order to enable the formation of homogeneous pore arrays while limiting damage due to electrical breakdown.

In this paper, we show that the electrochemical etching of silicon is perfectly adapted to the formation of 1  $\mu\text{m}$ , 750 nm, and 500 nm pore arrays corresponding, respectively, to densities of 1, 2, and 4 pores/ $\mu\text{m}^2$ . Such patterns are obtained using nanoimprint lithography (NIL). This technique shows great promise for nanopatterning due to its high resolution, high throughput, and low cost.<sup>16</sup> It con-

sists of duplication of a patterned silicon mold in a thermoplastic polymer film heated above its glass transition temperature. Thermal NIL has been used to obtain homogeneous nanostructures on 100 mm wafers.

## Experimental

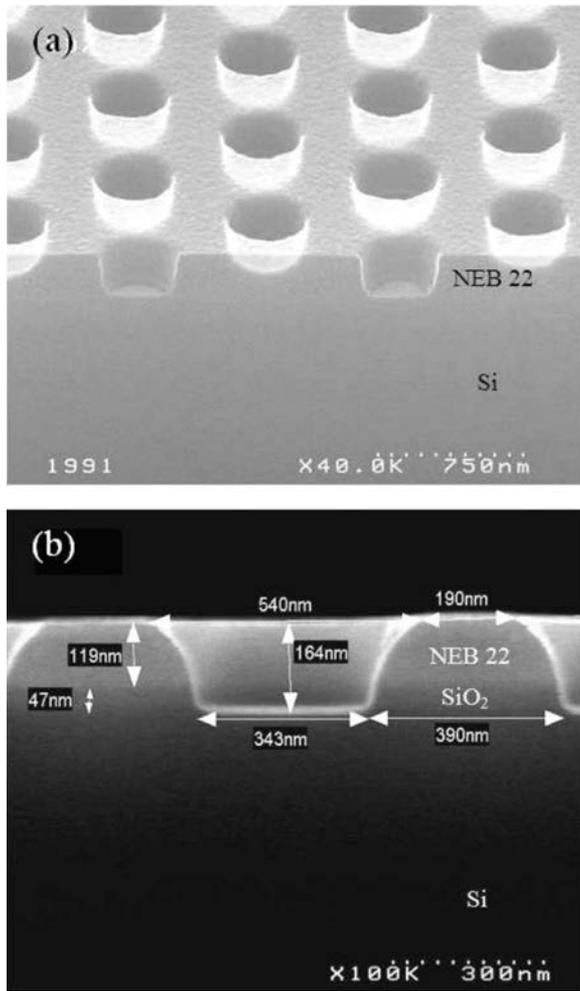
Experiments were performed on moderately doped n-type silicon (0.07, 0.15, 0.35, and 0.76  $\Omega\text{ cm}$ ),  $\langle 100 \rangle$  oriented, double side polished, and 525  $\mu\text{m}$  thick Si wafers. A  $\sim 50\text{ nm}$  thick silicon dioxide layer was then deposited on the front side using pulsed plasma enhanced chemical vapor deposition. Nanoimprint lithography was then used to define patterns on the 100 mm Si wafers.<sup>16</sup> First molds were fabricated by deep UV lithography and plasma etching. They were covered with an antisticking layer. They were imprinted in a NEB22 polymer film spin coated on the 100 mm Si substrates using a EVG520HE (EV Group, Austria) equipment, which led to uniform imprints on large surfaces (Fig. 1a). The printing parameters were 130°C, 20 bars during 4 min.

Three types of masks (A, B, and C) were processed, with pitches of 1  $\mu\text{m}$ , 750 nm, and 500 nm and pore openings of 400 nm, 375 nm, and 250 nm, respectively. A was a square lattice, while B and C were hexagonal lattices.  $\text{CF}_4$  plasma etching was then used to transfer patterns from NEB22 to silicon dioxide (Fig. 1b). After resist removal by  $\text{O}_2$  plasma, inverted pyramids were formed by KOH etching prior to EE.<sup>17</sup> EE was performed in a homemade PC controlled standard electrochemical cell, as described in Fig. 2. The cell was made of Teflon and had a volume of 400  $\text{cm}^3$ . The front side of the silicon sample was in contact with the electrolyte and had a circular shape with an area of 2  $\text{cm}^2$ . The electrolyte was prepared by adding buffered HF (BHF: Merck-Ammonium fluoride etchant AF 87.5–12.5) to a 3:1 mixture of deionized water and ethanol. Typical BHF concentrations used were in the range of 5–7.5 wt %. The counter electrode was a platinum grid immersed into the electrolyte. Infrared diodes (850 nm) were used at the back side to photogenerate carriers required for silicon dissolution. Applied voltage and etching current density were kept constant during the anodization time. The etching current was regulated by a feedback control of the intensity of the infrared diodes. After EE, the samples were cleaved in order to observe their cross section with an FEI Inspect F SEM microscope.

## Results and Discussion

Figure 3 shows high resolution scanning electron microscopy (SEM) images of pore arrays obtained from masks of types A, B, and C. Typical depths are about 20  $\mu\text{m}$  and the diameters are about 550, 350, and 270 nm, respectively. The etching conditions expressed in terms of resistivity/applied voltage/current density/BHF concentration are, respectively, 0.76  $\Omega\text{ cm}/3\text{ V}/4\text{ mA cm}^{-2}/5\text{ wt \% [BHF]}$ , 0.35  $\Omega\text{ cm}/3\text{ V}/4.5\text{ mA cm}^{-2}/5\text{ wt \% [BHF]}$ , 0.15  $\Omega\text{ cm}/$

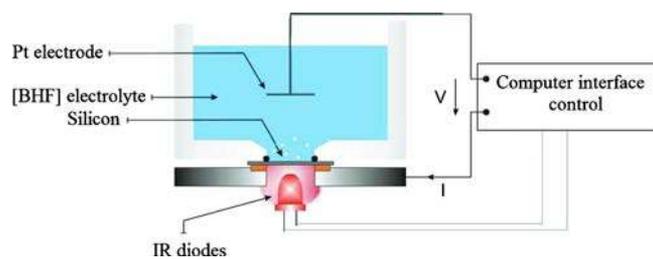
<sup>z</sup> E-mail: guillaume.laffite@univ-lyon1.fr



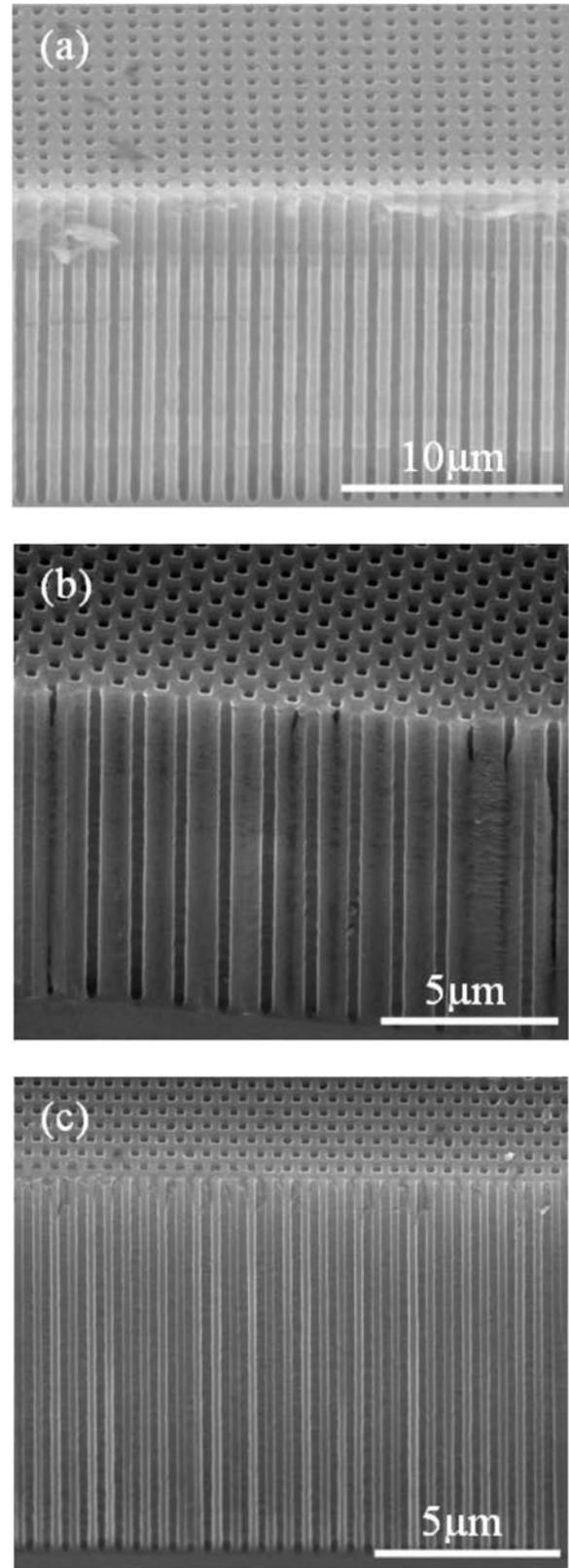
**Figure 1.** SEM views of pore opening (a) in NEB22 polymer film after imprint and (b) in silicon dioxide after  $\text{CF}_4$  plasma etching.

$4 \text{ V} / 7 \text{ mA cm}^{-2} / 5 \text{ wt \% [BHF]}$ . For each sample, the etching time is 2000 s. So, a typical etch rate is about  $0.5 \mu\text{m min}^{-1}$ .

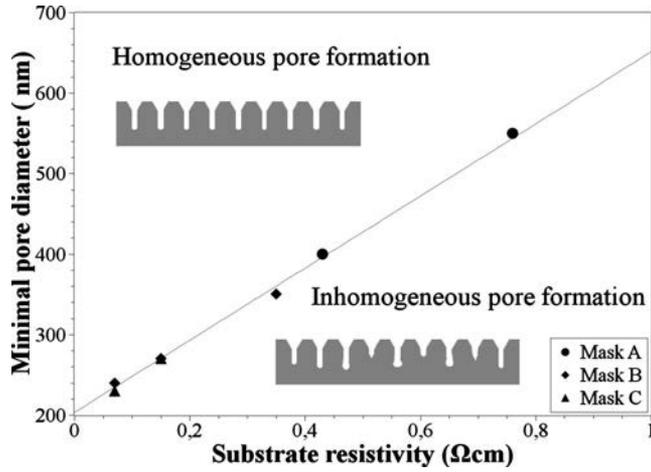
In the photon-assisted electrochemical etching process, the etching current density  $J$  is controlled by the back side illumination. The formation of homogeneous pore arrays requires high enough current densities to reach electropolishing at the pore tip.<sup>18</sup> This condition may be written as  $J_{\text{tip}} = J_{\text{ps}}$ , where  $J_{\text{tip}}$  stands for the current density at the pore tip and  $J_{\text{ps}}$  is the electropolishing current density. Within this etching regime, the pore etch rate is controlled by the steady state condition as described by Lehmann<sup>18</sup> and the pore diameter  $d$  is a function of the etching current density  $J$ . The relationship between  $d$  and  $J$  is



**Figure 2.** (Color online) Schematic diagram of the photoelectrochemical etching setup used in this study.



**Figure 3.** Cross-section SEM views of  $20 \mu\text{m}$  deep submicrometer structures formed by electrochemical etching: The pore diameter, period, and resistivities are (a)  $550 \text{ nm}$ ,  $1 \mu\text{m}$ ,  $0.76 \Omega \text{ cm}$ ; (b)  $350 \text{ nm}$ ,  $750 \text{ nm}$ ,  $0.35 \Omega \text{ cm}$ ; (c)  $270 \text{ nm}$ ,  $500 \text{ nm}$ ,  $0.15 \Omega \text{ cm}$ , respectively.



**Figure 4.** Dependence of the minimal pore diameter  $d_m$  on silicon resistivity for different masks. A reduction of diameter below  $d_m$  leads to unstable regime characterized by dying of pores. In the upper area (homogeneous pore formation), the pore formation is controlled by the steady state condition where the pore diameter is a function of current density according to Eq. 2.

$$\frac{J}{J_{ps}} \approx \text{etched area ratio} \quad [1]$$

In the case of circular pore arrays, this equation leads to

$$\frac{J}{J_{ps}} \approx \text{pore density} \times \frac{\pi d^2}{4} \quad [2]$$

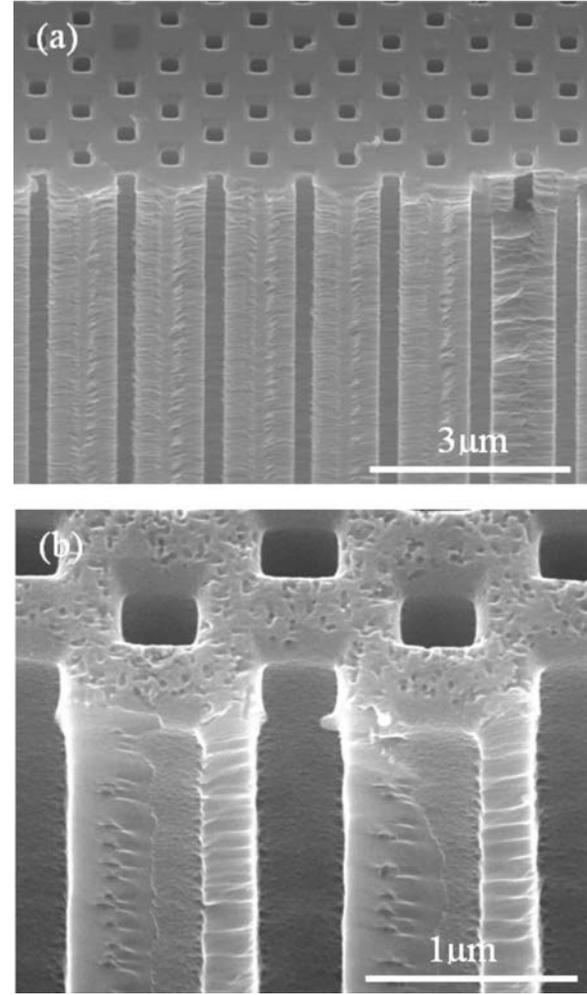
So, an increase of the etching current leads to an increase of the pore surface proportional to  $J$  and therefore an increase of the pore diameter proportional to the square root of  $J$ . However, experiments show that there is a critical current density  $J_m$  below which the steady state condition is no longer maintained and leads to dying; i.e., some pores are no longer etched. It is therefore possible to define a minimal pore diameter  $d_m$  which can be formed. Figure 4 shows  $d_m$  as a function of silicon resistivity. To make things clear, this figure means that for a given resistivity it is only possible to form homogeneous pore arrays with diameters greater than  $d_m$ . As shown in Fig. 4,  $d_m$  increases almost linearly with the resistivity for all three masks A, B, and C. We may deduce an empirical relation allowing determination of the diameter  $d_m$  according to the silicon resistivity  $\rho$

$$d_m \approx 450\rho + 200 \quad [3]$$

From our results, it cannot be concluded that the lattice periodicity or pattern morphology has an effect on the diameter  $d_m$ . Note, however, that the diameter  $d_m$  varies significantly with the electrolyte composition and more specifically with the use of HF or BHF. This phenomenon, which is not fully understood, will be the subject of future studies. The validity of Fig. 4 and Eq. 3 is therefore limited to the conditions described in the Experimental section.

Note that according to Fig. 4, it appears to be experimentally difficult to obtain  $<200$  nm diameter pores in this etching regime. The formation of  $<200$  nm diameter pores requires resorting to an etching process controlled by electrical breakdown.<sup>11</sup> The major drawbacks to this etching technique are the high amount of defects in the walls and the difficulty to control the pore diameters and depths.

We have also verified that it is possible, just as in the micrometer range, to form pores with diameters greater than  $d_m$  by increasing the etching current above  $J_m$  (homogeneous pore formation area presented in Fig. 4). As an example, from mask B using a  $0.15 \Omega \text{ cm}$  resistivity, we have etched about 270 nm diameter pores



**Figure 5.** Dependence of pore formation on etching current density ( $0.15 \Omega \text{ cm}$ , mask B): (a) etching at  $3 \text{ V}/4 \text{ mA cm}^{-2}/7.5 \text{ wt \%}$  [BHF]; (b) etching at  $3 \text{ V}/8 \text{ mA cm}^{-2}/7.5 \text{ wt \%}$  [BHF].

(Fig. 5a) at  $3 \text{ V}/4 \text{ mA cm}^{-2}/7.5 \text{ wt \%}$  [BHF] and about 395 nm diameter pores (Fig. 5b) at  $3 \text{ V}/8 \text{ mA cm}^{-2}/7.5 \text{ wt \%}$  [BHF]. As in the micrometer range, an increase of the etching current density  $J$  indeed leads to an increase of the pores diameter that is typically proportional to the square root of this density, according to Eq. 2.

In the previous section, our results showed the dependence of the minimal diameter  $d_m$  on the silicon resistivity. As a consequence, the minimal diameter  $d_m$  will define the maximal resistivity of silicon that can be used. For instance, if the goal is the formation of 300 nm diameter pores, Fig. 4 suggests that a resistivity less than  $0.2 \Omega \text{ cm}$  should be used.

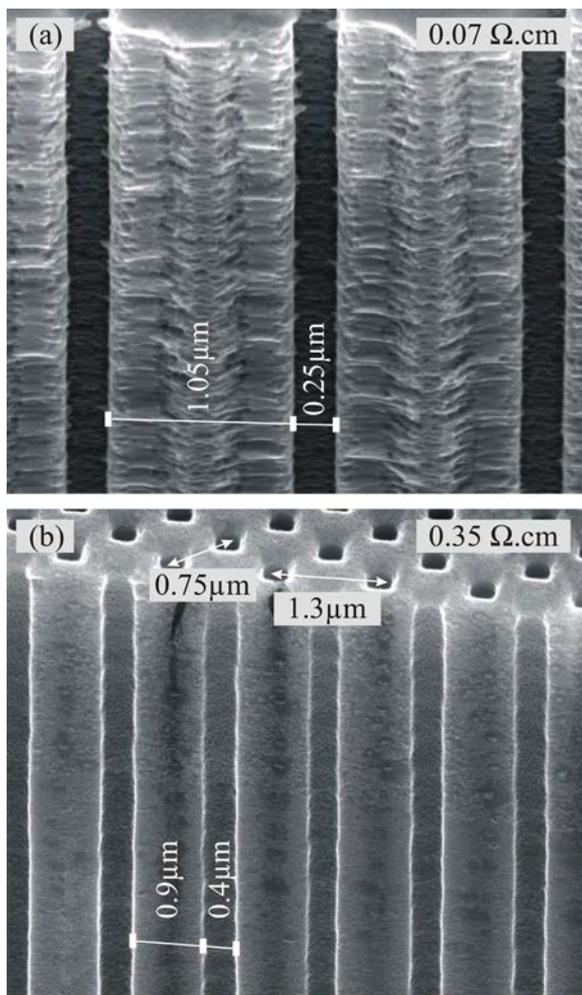
Nevertheless, a resistivity that is too low may lead to some damages in the walls. These defects might be linked to nonoverlapping of space charge region (SCR) or electrical breakdown.<sup>19</sup> The SCR overlapping condition enables pore wall passivation during etching.<sup>20</sup> In the case of a square lattice this condition requires

$$w > \frac{p-d}{2} \quad [4]$$

where  $w$  is the SCR width,  $p$  is the period of the lattice, and  $d$  is the pore diameter.

In the case of a hexagonal lattice, this relation becomes

$$w > \frac{\sqrt{3}}{3}p - \frac{d}{2} \quad [5]$$



**Figure 6.** (Color online) Cross-section SEM views of pores formed starting from mask B and showing the effect of the SCR overlapping condition on damages in the walls: (a) resistivity  $0.07 \Omega \text{ cm}$ , SCR overlapping condition not fulfilled according to Eq. 5; (b) resistivity  $0.35 \Omega \text{ cm}$ , SCR overlapping condition fulfilled.

Figure 6a shows the damages in the walls (transversal pores) for mask B (hexagonal lattice) when this condition is not fulfilled. In that case a resistivity of  $0.07 \Omega \text{ cm}$  is used, leading to an SCR width  $w$  of about  $100 \text{ nm}$ ,<sup>4</sup> while the period and pore diameter are  $0.75$  and  $0.25 \mu\text{m}$ , respectively. As another example, the use of a  $0.35 \Omega \text{ cm}$  resistivity with the same mask (Fig. 6b) allows one to considerably reduce damage while complying with the SCR overlapping condition. Indeed, the SCR width is about  $300 \text{ nm}$ ,<sup>4</sup> while the period and pore diameter are  $0.75$  and  $0.4 \mu\text{m}$ , respectively.

It is clear that the SCR overlapping condition can be fulfilled in the submicrometer range, like adjusting the silicon resistivity in the micrometer range. However, electrical breakdown is a critical issue during the formation of submicrometer pore arrays because of the use of low resistivity silicon wafers ( $< 1 \Omega \text{ cm}$ ). The etching current density  $J$  can be written as

$$J = J_{\text{photo}} + J_{\text{b}} \quad [6]$$

where  $J_{\text{photo}}$  corresponds to the photocurrent created by the IR diode and  $J_{\text{b}}$  is the breakdown current.  $J_{\text{b}}$  increases when the resistivity decreases. It is negligible for resistivities typically  $> 1 \Omega \text{ cm}$  and predominant for resistivities  $< 20 \text{ m} \Omega \text{ cm}$ .  $J_{\text{b}}$  being responsible for damages in the walls, we found experimentally that it is quite problematic to work with resistivities lower than  $50 \text{ m} \Omega \text{ cm}$ . Moreover,  $J_{\text{b}}$  also increases when the pore diameter decreases due to the high

electrical fields in the SCR.<sup>20</sup> Thus, the formation of the damages (transverse nanopores) in the walls during the pore formation induces an increase of  $J_{\text{b}}$ . As a consequence, working with a constant etching current density  $J$  and a high density of damages in the walls lead to a decrease of  $J_{\text{photo}}$  according to Eq. 6.

So, silicon resistivity is an essential parameter and must be chosen correctly depending on the pore geometry to be formed. On the one hand, this resistivity has to be as high as possible to limit the damages in the walls. On the other hand, it must be low enough to enable the formation of pores with the desired diameter (as shown in Fig. 4).

All the more, the major difficulty and the major requirement are to have low resistivity dispersion in a silicon wafer batch. For example, the dispersion given by the manufacturer could be comprised between  $0.1$  and  $1 \Omega \text{ cm}$ . Thus, some wafers from the batch will be suitable for the formation of  $250 \text{ nm}$  diameter pores and others for the formation of  $800 \text{ nm}$  pores. It is thus crucial to classify the wafers according to the resistivity with a precision of one or two significant digits.

The voltage effect is quite difficult to characterize because it has an influence on both the electric field of the SCR (and as a consequence on the focus of the electric field lines at the tip of the pores) as well as on the chemical reaction of the silicon dissolution. This reaction is not characterized well enough to do simulations on the electrochemical etching and so to accurately understand the voltage effect. Still, this voltage must be high enough to satisfy the  $J_{\text{tip}} = J_{\text{ps}}$  at the pore tip. Experimentally, we can observe that this condition is satisfied using  $3\text{--}4 \text{ V}$ . Working above  $3\text{--}4 \text{ V}$  increases damage by electrical breakdown in the walls, mostly in the  $\langle 100 \rangle$  direction.

The BHF concentration has a key role in the electropolishing current density  $J_{\text{ps}}$ . An increase of this concentration leads to an increase of  $J_{\text{ps}}$  and therefore an increase of the pore's etch rate.<sup>21</sup> However, because the correct formation of the pores requires the  $J_{\text{tip}} = J_{\text{ps}}$  condition, it is necessary to photogenerate a sufficient number of carriers with the infrared diode. In this study, we use a  $1.5 \text{ W}$  infrared diode emitting at  $850 \text{ nm}$ . The BHF concentrations presented are adapted to this infrared diode. The use of a more powerful diode would allow an increase of the BHF concentration and therefore an increase of the etch rate.

## Conclusion

We have showed that n-type silicon electrochemical etching, such as described by Lehmann, is perfectly adapted to the formation of deep submicrometer pores. The use of the nanoimprint lithography technique has enabled us to form pore arrays with periods of  $1 \mu\text{m}$ ,  $750 \text{ nm}$ , and  $500 \text{ nm}$ . In this range of periods, the silicon resistivity is a critical parameter. It has to be adjusted accurately (with a two decimal precision) depending on the desired period and pore diameter. We show here that  $< 0.15 \Omega \text{ cm}$  resistivities enable the formation of pores with a  $< 270 \text{ nm}$  diameter.

This shows the realistic possibility of forming pore arrays with a period down to  $300 \text{ nm}$ . We are currently working on the etching of pores with periods of  $450$  and  $400 \text{ nm}$  by holographic lithography techniques. We are also working on another etching regime (with lower voltage and etching current) in which the etch rate is no longer bound by  $J_{\text{ps}}$  and which enables us to work with higher resistivities and to obtain smaller diameter pores while limiting electrical breakdown phenomena.

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