Experimental validation of the exponential localized states distribution in the variable range hopping mechanism in disordered silicon films

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Carriers transport in low temperature ($\leq$600 °C) polycrystalline silicon thin film transistor channel region is studied for devices biased from weak to strong inversion. Analysis is supported by the theory of the 3D variable range hopping model due to hopping between localized electronic states near the Fermi level. The corresponding density of states is determined following an exponential (tail states) distribution associated with the statistical shift of the Fermi level. © *2011 American Institute of Physics*. [doi:10.1063/1.3625944]

Electrical properties in amorphous, or poly-, micro-, and nano-crystalline silicon materials are strongly controlled by trapping effect at defects located within the bulk of the layer. Many studies reported on carriers transport in such disordered silicon thin film layers in relation with spatial structural defects distribution. For amorphous or micro- or nano-crystalline silicon, embedding quasi uniformly distributed high defect density, it is widely admitted that most convenient transport mechanism describing electrical properties is carriers hopping between localized states close to the conduction band edge (E_C), first proposed by Mott.[1] For 100 nm thicker polycrystalline layers, made of large size (>100 nm) monocrystalline grains with a columnar structure, it is usually admitted that defects are mainly located at the grain boundaries. In this case, according to Seto's theory,[2] carrier transport is strongly affected by intergranular barriers induced by the carriers trapping effect at defects located at these grain boundaries.

Two main causes of bulk defects are usually invoked: dangling bonds and strained bonds corresponding to deep and shallow level trap states into the band gap, respectively. Two types of distributions are considered: Gaussian distribution with a maximum around the midgap and exponential band tailing corresponding to dangling bonds and strained bonds type defects, respectively.[2,3] Methods based on capacitance, resistivity, conductance activation energy, and low frequency noise measurements exist to determine these distributions.[4–7] The corresponding energy distribution of the states (DOS) is representative of the crystal quality of the material, thus of the fabrication parameters, and many studies have been devoted to the determination of the DOS used as diagnostic tool.

In this paper, carriers transport in low temperature ($\leq$600 °C) processed polycrystalline silicon thin film transistors (TFTs) is analyzed in function of temperature and gate voltage. Polycrystalline silicon channel region is considered quite similar to disordered silicon material embedding quasi spatially uniform distribution of gap states. Analysis of the field effect conductance allows the determination of the exponential localized tail states distribution related to variable range hopping (VRH) process of carriers.

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Devices are fabricated on glass substrate. A thick atmospheric pressure chemical vapour deposition (APCVD) SiO_2 layer is first deposited to prevent a possible contamination from the substrate because of thermal annealing during the fabrication process. TFTs are elaborated with one 200 nm thick polycrystalline silicon layer: the upper part (100 nm thick) is heavily *in situ* N-type doped (source and drain regions) and the bottom part is non-intentionally doped with a residual doping $\sim 2 \times 10^{16}$ cm^{-3} and is dedicated to the active layer. Polycrystalline silicon layer is deposited by low pressure-CVD (LPCVD) technique in an amorphous state and is crystallized by a solid phase crystallization (SPC) thermal annealing in vacuum at 600 °C. The gate insulator is made of a 60 nm thick SiO_2 layer deposited by APCVD technique at 420 °C and annealed in nitrogen ambient for densification. Electrodes are made of thermally evaporated aluminium. Finally, the devices are annealed into forming gas at 390 °C to ensure good electrical contacts.

Dark current-temperature measurements, in the range 200 K to 530 K, are carried out with samples placed in a cryostat in vacuum (10^{-4} Pa) using a Keithley 617 electrometer. All tested N-channel TFTs are biased in the linear mode ($V_{DS} = 300$ mV) and operating from weak to strong inversion ($-4\ V \leq V_{GS} \leq 4\ V$).

For low-temperature ($\leq$600 °C) polycrystalline silicon TFTs, the structure of the channel region, located close to the gate insulator/active layer interface, is significantly different from crystalline silicon metal oxide semiconductor field effect transistor (MOSFET) because of both deposited SiO_2 gate insulator and polycrystalline silicon active layer qualities. The structural defects are located close to the interface due to the non-respect of stochiometry of the silicon oxide, the surface roughness,…, and also within the active layer with significant intra-grains defects density (in addition to those located at the grain boundaries) for such low temperature crystallized polycrystalline silicon layer. Thus, it is reasonable to consider spatial structural defects uniformly distributed along the active layer. The corresponding trap states are distributed over a large bandgap energy range and large values amplitude. In this way, it is realistic to consider structural quality of both polycrystalline silicon active layer and interface region quite similar to (amorphous-type or) highly disordered silicon material. Therefore, because

carriers transport mainly takes place in channel region for TFT biased from weak to strong inversion, the most convenient model describing electrical properties in such highly disordered N-channel region is carriers hopping between localized states close to the conduction band edge (E_C).[1] In this case, carriers transport mechanism is thermally activated.[8] The activation energy was deduced from the slope of the linear decrease of the conductance in an Arrhenius representation. The corresponding measured activation energy (E_A) decreases with the gate voltage (Fig. 1(a)). Values are consistent with previous modeling of the channel conductance in hydrogenated amorphous silicon TFTs.[9] The decrease of E_A is related to the increase of the carriers number in the channel, and thus also to the statistical shift of the Fermi level into the upper part of the bandgap energy.

For polycrystalline silicon TFTs biased from weak to strong inversion, carriers transport takes place in a region which depth conduction pathway varies with the applied gate bias magnitude. For the device biased in the subthreshold region, close to the flatband voltage condition $V_{FB} = -3$ V (estimated at the minimum of the drain current of the transfer characteristics of the TFTs $I_{DS} = f(V_{GS})$, see in Ref. 7), carriers flow through the almost active layer thickness. For devices biased above the threshold (strong inversion), conduction occurs in few nanometers thick channel region. In this case, considering such modulation of the channel conduction pathway, the 3D VRH model to describe carriers transport is rather more appropriate than the 2D model used for hydrogenated amorphous silicon TFTs.[10] The field effect enhanced channel conductance ($g_{DS} = I_{DS}/V_{DS}$) temperature dependence displayed in the Figure 1(b) shows that channel conductance follows the 3D VRH mechanism described by Mott's law:[1]

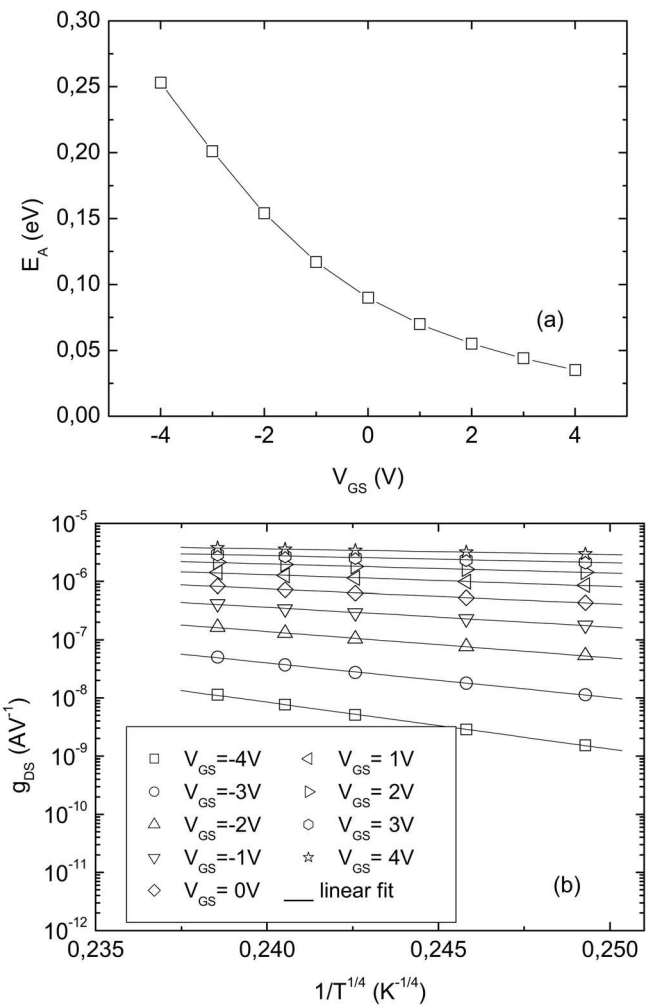

FIG. 1. Polycrystalline silicon TFTs are biased from weak to strong inversion ($-4\ V \le V_{GS} \le 4\ V$). (a) Plots of the measured channel conductance activation energy as a function of the gate voltage. (b) Polycrystalline silicon TFTs channel conductance as a function of $T^{1/4}$.

$$g_{DS} = g_{DS0} \exp\left[-\left(\frac{T_0}{T}\right)^{1/4}\right], \tag{1}$$

where g_{DS0} and T_0 are both dependent on the gate voltage, and[11–15]

$$T_0 = \frac{\gamma^3 c^4}{kN(E_F)}, \tag{2}$$

with k the Boltzmann constant and $N(E_F)$ the density of localized states near the Fermi level (E_F) calculated by adjusting the parameter electronic wave decay length γ^{-1} for localized states ($0.3\ nm \le \gamma^{-1} \le 3\ nm$), and c a constant in the range of 2.06 to 4.2 depending on the $N(E_F)$ feature.[9] In this model, hopping refers to carriers tunneling transitions from occupied to unoccupied localized states, the state energy difference being bridged by emission of absorption of one or several phonons. The hopping between states that are close in energy (even if they are wider spaced) becomes preferable than that between the nearest neighbors whose energies differ substantially. In addition, according to Mott,[1] $N(E_F)$ is assumed an energy independent distribution, and a large number of previous studies on carriers transport,[11–15] in particular for amorphous, micro- or nano-crystalline silicon layers, reported average value depending on the quality of the material.

The dependence of the conductance pre-factor, g_{DS0}, (deduced from the linear fits of the plots in the Figure 1(b)), with $T_0^{1/4}$ is displayed on the Figure 2 and follows:

$$g_{DS0} = g_{DS0m} \exp\left[\left(\frac{T_0}{T_m}\right)^{1/4}\right], \tag{3}$$

with T_m, defined as characteristic temperature (≈621 K), and g_{DS0m} both independent on gate voltage. According to previous study based on numerical modeling of single-phonon hopping transport,[12] such positive correlation between these two parameters predicts an exponential (tail states) distribution of the localized electronic states $N(E_F)$ related to strained bonds type defects in the core of the disordered semiconductor. Such states distribution feature acts as a quality factor of the polycrystalline silicon active layer.

The analysis of the field effect enhanced channel conductance allows the determination of the localized states density from relation (2) for each T_0 value (measured for TFTs biased from weak to strong inversion). Calculations were carried out for $c = 4.2$ corresponding to an exponential state distribution.[12] In addition, assuming that $E_A \approx E - E_F$,

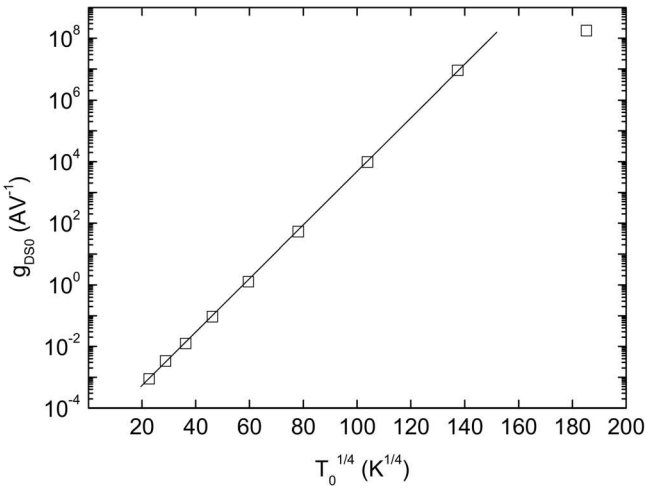

FIG. 2. Plots of the polycrystalline silicon TFTs channel conductance prefactor g_{DS0} as a function of $T_0^{1/4}$.

the dependence of $N(E_F)$ with E_A gives an insight of the corresponding exponential states distribution (for one adjusted γ^{-1} value) into the upper part of the bandgap. In this way, the localized state distributions are reported in the Figure 3 for 0.3 nm $\leq \gamma^{-1} \leq 3$ nm (grey area). Values obtained for highest γ^{-1} values are quite consistent with those measured by other experimental methods for highly disordered silicon layers.[13,16,17] This means that $\gamma^{-1} \sim 3$ nm could be an appropriate value for the studied polycrystalline silicon TFTs. In addition, the increase of $N(E_F)$ with E_F shift was also previously observed with the increasing doping level in p-doped microcrystalline silicon.[13,14]

In this case, at low activation energies (high gate voltages), it means that close to the conduction band gap edge, $N(E_F)$ related to shallow tail states distribution can be modeled as (see Fig. 3)

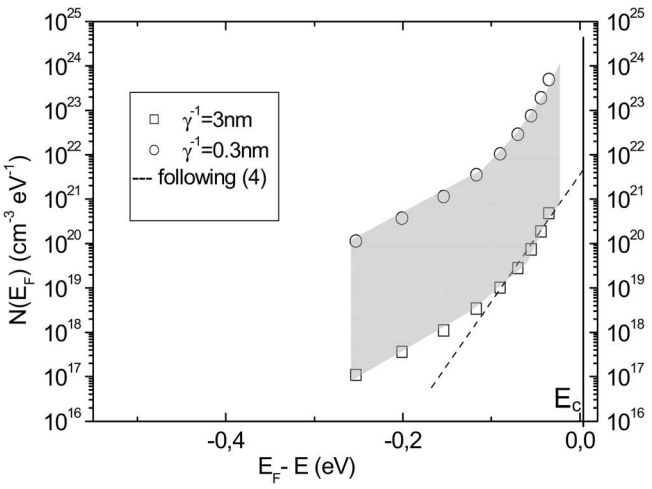

FIG. 3. Distribution of localized states as a function of the position of the Fermi level in the upper part of the bandgap calculated with c = 4.2, and for 0.3 nm $\leq \gamma^{-1} \leq 3$ nm (grey area). Dotted plots: calculated exponential distribution following (4) for $\gamma^{-1} = 3$ nm. The linear fit gives a linear regression coefficient R = 0.989, with error bar $\Delta N_0 = 1.4 \times 10^{21}$ cm^{-3} eV^{-1} and $\Delta E_0 = 1.2$ meV.

$$N(E_F) = N_0 \exp\left(-\frac{E - E_F}{E_0}\right), \quad (4)$$

with $N_0 = 4.1 \times 10^{21}$ cm^{-3} eV^{-1}, $E_0 = 15$ meV. Such distribution is consistent with theoretical calculations previously reported in the case of hydrogenated amorphous silicon.[16,18] However, at high activation energies (low gate voltages) the plots of $N(E_F)$ is not representative of the tail states distribution. In this case, due to the high defects density within the polycrystalline silicon active layer, one can consider that the Fermi level is pinned and thus a quasi constant value of $N(E_F) \sim 10^{16}$–10^{17} cm^{-3} eV^{-1} is measured. This result could be related to the energy independent $N(E_F)$ assumed in the Mott's model, usually reported in many previous experimental analysis of the 3D VRH mechanism in disordered semiconductors.[13–15,19,20] Only theoretical or numerical models proposed an exponential distribution of localized states for hopping process.[12,21] Therefore, our experimental analysis gives a method to determine the DOS to qualify disordered semiconductors and validates the model of exponential (tails) states distribution involved with the VRH model.

Analysis of electrical behavior in low temperature ($\leq$600 °C) polycrystalline silicon TFTs by the field effect method shows that carrier transport is described by 3D variable range hopping mechanism between defect states near the Fermi level. Results show that localized states exponentially distributed in the upper part of the bandgap contribute to the VRH model. This present method is proposed to quantitatively determine the corresponding distribution of the localized electronic shallow tails states to qualify polycrystalline silicon active layer and could be extendedly used for disordered semiconductors qualification.

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