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Plasma etch technologies for the development of ultra-small feature size transistor devices

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Key words: Plasma etch, reactive ion etching, inductively coupled plasma, block copolymer lithography, feature size, pattern transfer

Abstract

The advances in information and communication technologies have been largely predicated around the increases in computer processor power derived from the constant miniaturization (and consequent higher density) of individual transistors. Transistor design has been largely unchanged for many years and progress has been around scaling of the basic CMOS device. Scaling has been enabled by photolithography improvements (i.e. patterning) and secondary processing such as deposition, implantation, planarization etc. Perhaps the most important of the secondary processes is the plasma etch methodology whereby the pattern created by lithography is 'transferred' to the surface via a selective etch to remove exposed material. However, plasma etch technologies face challenges as scaling continues. Maintaining absolute fidelity in pattern transfer at sub-16 nm dimensions will require advances in plasma technology (plasma sources, chamber design, etc.) and chemistry (etch gases, flows, interactions with substrates, etc.). In this article, we illustrate some of these challenges by discussing the formation of ultra-small device structures from the directed self-assembly of block copolymers which micro-phase separate in various conditions. The polymer pattern is transferred by a double etch procedure where one block is selectively removed and the remaining block acts as a resist pattern for silicon pattern transfer. Data is presented which shows that highly regular nanowires patterns of feature size below 20 nm can be created using etch optimisation techniques and in this article we demonstrate generation of crystalline silicon nanowire arrays with feature sizes as below 8 nm. Block copolymer techniques are demonstrated to be applicable from these ultra-small feature sizes to 40 nm dimensions. Etch profiles show rounding effects because etch selectivity from in these nanoscale resists patterns is limited and the resist thickness rather low. The nanoscale nature of the topography generated also places high demands on developing.

Introduction

It is often said that Moore's law has driven progress in microelectronics for over 40 years [1]. This scaling not only enables greater device densities and computing power but also

decreases power usage and cost [2]. State of the art integrated circuitry has feature sizes of 32 nm with around 1 billion transistors on a single die (chip) [3]. However, the industry is largely product demand driven and the need to deliver higher performance - in e.g. medical diagnostics such as MRI and personalised treatment, high resolution video capture and storage, 3D video demands, improved graphics, data encryption as well as high density storage – will drive the processor industry towards 4 nm features sizes and possibly less. Scaling has been achieved by photolithography, the process by which light passing through a patterned mask is incident on a photosensitive resist film at a substrate [4]. The incident light either stabilises or destabilises the resist (negative and positive tone resists) to a solvent so that by solution the mask pattern or its inverse is created in the resist film. In the simplest form of patterning, the patterned resist is used as an etch mask whilst exposed substrate is controllably removed to transfer the pattern to the substrate. Whilst originally wet chemistries were used as etches, the advantages of plasma etching where chemically active radicals/ions were used to remove material led to its' exclusive use [5]. The advantages of inductively coupled plasma (ICP) and reactive ion etching (RIE) methodologies in terms of anisotropy (i.e. etching in vertical direction only with little or no lateral etching), large-area and high-density at relatively low pressures have led to the adaption of these sources in industry [6]. Perhaps the greatest advantage of plasma techniques in modern integrated circuit (IC) manufacture is the uniformity of the etch process which results in extremely uniform features [7].

However, in the last 10 or so years the fabrication industry has undergone and will undergo something of a revolution as both materials and device design change dramatically. Ever decreasing dimension and the role of line edge roughness on device variation [8] will necessitate the development of ever more specific, anisotropic plasma etches (for silicon, silica, gate dielectric and other materials). The introduction of new materials such as ultra-low-dielectric constant (ULKs) for interconnect isolation [9], high dielectric constant materials such as HfO_2 for the gate dielectric [10] and the introduction of new device materials such as III-Vs for electron and Ge for hole transport [11] will necessitate the development of new etches and etch techniques allowing high anisotropy and composition control in compositionally and structurally complex materials. Further, beyond feature sizes of 16 nm, fundamental changes to both the front end (device level) and back end (interconnect layers) processes will be required.

Devices are expected to move from simple planar designs to nanowire or so-called finFET (fin-field effect transistors) structures [12]. A simplistic schematic of a 3 fin device is shown in Figure 1(a). Potentially, these devices have significantly enhanced performance compared to simple planar CMOS structures but require complicated plasma etch processing to create structures with highly regular sidewalls and relatively high height to diameter aspect ratios. They would be fabricated e.g. from silicon on insulator (SOI) substrates where significant material is removed to form the nanowires. Subsequent lithography-plasma etching is then required to create source/drain and the gate, again with fine control of sidewall regularity. As described above, the active device material is likely to change from silicon or strained silicon and gates are likely to become more complex oxides and oxide mixtures. Precision end-point

control (where the etch is stopped) will be required because substrates and gates are likely to be complex, graded, multi-layer structures because of substrate-film lattice mismatch. The level of control of the plasma conditions and etch recipes will be significantly greater than current and likely to require significant methodology development. Besides their application in front end processes, plasma etching is used extensively in back end processing, particularly in the development of topography in which copper is deposited to form the interconnects and vias that connect devices. The Damascene process is a lithographic-etch combination where silica dielectric layers are etched to pattern channels and holes into which copper is plated [13]. The copper is then planarized to remove excess metal. This avoids difficult copper etching since fluorine and chlorine ions produce non-volatile products. Etch stops are used to prevent over etching and poisoning of the device layer. However, resistance-capacitive coupling and the time delay that results, has led to the use of porous silica in an effort to reduce the dielectric constant. This is problematical to etch controllably because of the thin-wall structure between pores. The development of ordered mesoporous ULKs will challenge the plasma chemistry further [9] as shown in Figure 1(b) to 1(d). Unless the etch is highly controlled, poor sidewall regularity is difficult to avoid.

It is clear that implementing plasma techniques for surface etching will be a challenge as the nature of transistor devices changes. One potential method for extending the current scales achievable by 193 nm photolithography is the double exposure technique where e.g. features are patterned into resist and a plasma exposure is used to isotropically etch these features to a smaller size [14]. A second application of resist and lithographic exposure then creates a resist pattern between the first set which are also isotropically etched to reduce feature size. A third etch is then used to transfer the resist pattern to a device layer. However, the ITRS clearly points to a number of solutions to overcoming barriers to ultra-small (<16 nm) feature size [3]. One of these involves the use of directed self-assembly where chemical interactions between moieties results in the spontaneous formation of a regular pattern at a substrate surface. These patterns then act as a resist for transfer to a device layer [3]. This form of chemical patterning will be used to illustrate some of the more interesting challenges facing plasma etch methodologies in the next few years.

Plasma processing for development of nanoelectronics

A plasma is a partially ionised gas containing, ions, radicals and neutrals. The energy to create the plasma is obtained via the coupling of an external magnetic field to the plasma gas. Industrial IC manufacture has been realised by two plasma etching techniques; reactive ion etching (RIE) and inductively coupled plasma (ICP) methods. RIE has been summarised by, e.g., Jansen et al [15]. An RIE apparatus consists of a glow discharge generated plasma where gas molecules (e.g. SF₆ for silicon etching) are dissociated and ionised to create reactive species. Substrates are placed on an r.f (radio frequency)-driven capacitively coupled electrode to generate a d.c. bias at the sample. Reactive species, such as F radicals and ions, impinge on the surface creating volatile silicon species. In most practical processes, RIE is actually a combination of the reactive species reactions that are highly species selective and ion bombardment where the reaction is a physical process caused by kinetic

energy transfer. Radical etching (or true plasma etching) is limited to neutral radicals and the plasma is normally excited by microwaves. These plasma etches are chemical in nature and can have very high selectivity and impart little damage. They are, in essence 'isotropic'. This type of selective etch is used to remove photoresist after pattern transfer.

In silicon technologies, selectivity or contrast between the removal rate for the resist and the exposed substrate allow a pattern transfer process to take place generating sharp-edged substrate features with high aspect ratios. As feature sizes decrease, the critical dimension (CD, the regularity of feature size) becomes ever more important because of the need to reproduce devices with similar characteristics [16]. Thus, one of the main challenges will be how to produce topographic features in a substrate with high fidelity and low roughness when mask materials may not be of ideal composition or thickness (see below for examples). High aspect ratio (depth/feature size) features require 'anisotropic' etches and is achieved using plasmas that generate both radicals (i.e. chemical selectivity) and ions (physical removal of substrate species) and is described by the generic term RIE. In RIE, plasma exposure develops a negative charge at the substrate from electrons produced in the plasma. This charge accelerates positive ions towards the surface in a direction normal to the surface plane. This ion bombardment occurs causing accelerated substrate removal as well as roughening the surface to create more reactive surfaces. In order to achieve higher ion bombardment rates the RIE plasmas are characterised by low plasma potentials (< 100 V) and high r.f. biases (> 500 V) compared to plasma etching where there is only low sample bias (< 10 V). Sidewalls of features are largely unaffected by the bombardment process and so the sidewalls etch at a much lower rate than the substrate base allowing high aspect ratio features to be generated with vertical sidewalls and little change in resist feature size and spacing [17]. It is important to note that RIE is a true combinatorial technique in that etch rates for RIE are higher than the total etch rate that might be achieved by ion beam and chemical etching separately [18].

Etch directionality in RIE can be achieved in two main ways. The first of these is simple ion-induced RIE where ion modification of the exposed surface leads to enhanced removal [19]. Typical examples are Cl_2 sponsored etching of Si and O_2 etching of polymers. The most common technique in the microelectronics industry is ion-inhibition RIE where the as-created sidewalls are coated with a passive film that resists etching [15]. This film can be created by use of gases that e.g. form stable non-volatile carbon halogen materials [20], trapping volatile silicon products at the trench walls by cryogenic cooling [21], using gases (e.g. C_4F_8) that form polymeric barrier layers [22] and erosion/re-deposition of mask materials such as metal halogens. Typical examples are chlorine and bromine based silicon etches, whilst $\text{SF}_6 - \text{O}_2$ based plasmas can also be used as anisotropic etches. An ever more important issue in RIE is aspect ratio dependent etching (ARDE) [23, 24]. This has been important in micromachining for some time as high aspect ratio features are required. However, as device feature size reduces, this is becoming a general problem in nanocircuitry generation. ARDE describes the loss of fidelity that occurs in small feature sizes where feature width is comparable or less than the feature depth. ARDE is a result of several issues, e.g. deflection via ion scattering of

ions towards the sidewall, diffusion effects in reactants/product reaching/leaving the base of the feature and diverging electric fields in the feature.

The inductively coupled plasma (ICP) technique can achieve much higher etch rates than RIE etching as they can operate at high plasma densities [25]. In comparison to RIE tools where the r.f. frequency is capacitively coupled to the plasma gas, in an ICP etcher power is input inductively. ICP etchers have their impedance matched to the plasma and consequently achieve high coupling efficiency between the plasma electrons and the applied field. Further, the plasma is much more controllably contained in ICP tools which further improve efficiency. ICP tools operate at low pressures (< 20 mT) which have important consequences. The general principles of plasma etching described above (such as etch chemistry, etch anisotropy, sidewall modification etc.) for RIE are maintained for ICP systems but there are proven advantages of the ICP technique. The low pressure improves diffusion of reactive species into small features enhancing the rather low etch rates achieved by RIE in very small feature sizes. It also reduces ion scattering and so improves the anisotropy of an etch. There are also distinct disadvantages of the ICP etch process. The low pressure reduces selectivity of the etch process and so results in mask damage and removal. The use of thick etch masks limits feature depth. For these reasons, combination ICP-RIE etch tools are frequently used to achieve optimum results.

The following will describe how very small feature sizes can be achieved at silicon substrates using block copolymer nanolithography. The use of block copolymers (BCPs) for generating highly regular patterns at surfaces is now well-established and has been ear-marked as a possible solution for achieving ultra-small features for silicon and related materials [26, 27]. These systems form ordered patterns by a process of microphase separation [26,27]. However, the need to achieve pattern transfer of the very small features realised by these methods via plasma etching methods is a serious challenge [28].

Experimental

Self-assembled PS-b-PMMA (polystyrene-b-polymethylmethacrylate) block copolymer patterns are used for nanolithography – pattern transfer of the substrate to silicon substrates. The concept is simple. A selective ion etch is used to selectively remove the more reactive PMMA leaving a topographic PS pattern over the silicon surface. The PS is used as mask to protect underlying silicon from a silicon ICP etch.

Plasma etching: PMMA dry etch removal was performed with an Oxford Instruments Plasmatech 100 system in RIE mode using various oxygen (O₂) and tri-fluoromethane (CHF₃) mixtures at a pressure of 10 mTorr at 10 °C. For homopolymer etching, both PS and PMMA films were loaded within the same etch sequence to ensure both films were exposed to identical processing. Two silicon pattern transfer procedures were utilised using a combination of silicon hexafluoride (SF₆) and octafluorocyclobutane (C₄F₈) in ICP mode at a pressure of 15 mTorr at 10 °C. In the first method the flow rates were 90 sccm and 40 sccm for C₄F₈ and SF₆ respectively and the etch time was 30 s at an ICP power of 400 – 600 W. In

the second method the flow rates were 80 sccm and 15 sccm for C₄F₈ and SF₆ respectively and the etch time was 12 s at an ICP power of 1200 W. A third oxygen plasma etch was used to remove residual PS after pattern transfer. This PS strip was centred on a 2000 W ICP etch at a pressure of 10 mT with an O₂ flow of 30 sccm for a time of 10 s.

The etch conditions to provide maximum selectivity to PMMA were found by studies of PS and PMMA homopolymer samples which allowed etch contrast between the blocks to be carefully optimised. The RIE etch uses a combination of oxygen and fluorine sources since the addition of oxygen dramatically increases production of fluorine ions and increasing etch anisotropy whilst enhancing selectivity to the oxygen containing PMMA block. In the ICP etch SF₆ acts as the source of ion and radical fluoride species whilst the C₄F₈ forms a polymeric layer at the sidewalls allowing high etch anisotropy and relatively deep feature sizes (i.e. high aspect ratio) to be produced.

Block copolymer polymer development: Symmetric PS-*b*-PMMA copolymers with molecular weights of approximately, 90-85, 52-52, 37-37 and 18-18 kg mol⁻¹ (the polymers are indicated as e.g. PS-*b*-PMMA 37 k – 37 k through the text) and a neutral polystyrene-*random*-polymethylacrylate (PS-*r*-PMMA) with a PS content of 58% were purchased from Polymersource of Canada. For this study, a 1.5% weight solution of PS-*b*-PMMA in toluene was deposited at 3000 rpm onto a PS-*r*-PMMA brush layer. The brush layer was deposited by spincoating and annealed for up to 12 h at 180 °C. A thin approximately 3 nm layer remains after repeated washing of the non-reacted PS-*r*-PMMA layer in toluene. The brush layer is needed to assure vertical (to the surface) arrangements of lamellar blocks of the two polymer types which would tend to form parallel layer structures without use of the brush [26]. For homopolymer films, solution concentrations of 2 wt. % polystyrene (PS) and 4 wt. % polymethylacrylate (PMMA) were used. This provided homopolymer films with final thickness values in the range of 100 to 150 nm which were used to establish preliminary etch rates. Block copolymer films were annealed at 180 °C under vacuum for around 12 h.

Film characterisation: A J.A. Woolam (M-2000U) spectroscopic ellipsometer was used to evaluate homopolymer film thicknesses before and after etching. Scanning probe microscopy measurements were performed using a DME DS-50 dual scope in tapping mode. SEM images were obtained using Hitachi S4800 cold emission microscope and FEI dualbeam strata 400 operating between 2 and 10 kV. In order to minimize charging effects, samples were coated with a thin layer of Au/Pd sputtering methods. TEM samples first received a 25 nm gold protection layer by electron beam evaporation (Temescal FC-2000) at room temperature. This can be observed in some of the images described below. The gold protects the delicate polymer films during cross-section preparation and provides image contrast because of the low atomic number of carbon which ensures that only silicon and SiO₂ are generally seen. Electron transparent cross sectional samples were prepared using FIB or via a sequence of grinding and precision polishing steps (Gatan Series, model no. 691) resulting in a region of electron transparency at the thin film/silicon interface. All FIB samples were also precision polished to obtain the highest quality images possible. Cross sectional images of the etched films were taken on a JEOL 2000 FX operating at 200 kV.

Results and Discussion

As outlined above, to estimate the etch rate of the individual PS and PMMA blocks and, more importantly, to establish the ideal conditions for achieving etch selectivity (etch contrast) between the PS and PMMA blocks, etch rates of homopolymer films were investigated in a similar manner to methods outlined elsewhere [29]. Briefly, Asakawa showed that the higher the oxygen content within the polymer backbone, the faster it's etch rate was for a specified set of parameters in a CF_4 RIE configuration [29]. Thus, as PMMA contains an ether linkage and PS is an aromatic hydrocarbon, etch contrast between the two polymers is possible. Using the homopolymer films, the RIE gas flows were adjusted to provide the highest PMMA etch rates and minimum PS etch rates. Data are provided in Table 1 which provides the gas flow rates for trifluoromethane (CHF_3) and oxygen (O_2) mixtures, homopolymer film thickness, resultant etch rates per minute and PS to PMMA selectivity for a series of RIE etches. We emphasise of course, that these values are provided as a guide for other researchers but it is noted these will generally not be transferable to other equipment as etching is reliant on plasma properties and, hence, experimental configuration etc and these values represent optimum performance for the apparatus used here. We do note that gas flow rates did have considerable effect on the etch profile of the nanostructures generated. This is in itself an unusual observation and we suggest this may be related to etch product removal rate variation which is critical in these ultra-small topographies generated. It can also be seen that the introduction of fluorine deficient CHF_3 into the O_2 RIE which is often used for polymer etching results in improved selectivity and this can be suggested to be as a result of polymerization in the etch process [30]. Careful process control through flow rate control allows etch selectivity optimization. It was found that a RIE using CHF_3/O_2 with the following flow rates of 40 sccm/5 sccm provided a PMMA etch rate of 45 nm min^{-1} but more importantly a reduced etch rate for PS of 13 nm min^{-1} over the same time window. This represented an etch selectivity of PS to PMMA of 3.5 for the PS and PMMA homopolymer films.

These etch conditions were then used to selectively etch the PMMA block a self-assembled patterned PS-*b*-PMMA film. Figure 2(a), is a topographic AFM image of a PS-*b*-PMMA (37 k - 37 k) film produced by deposition and vacuum annealing of the BCP onto a silicon substrate with a neutral PS-*r*-PMMA brush layer pre-deposited as described above. The film adopts a characteristic fingerprint pattern with the blocks oriented vertically. The feature size was measured at 21 nm. The film has an overall thickness of ~56 nm (inclusive of polymer brush) as determined by TEM. Based on the conditions identified for maximum selectivity for the homopolymer etching, the patterned PS-*b*-PMMA films were etched for different times ranging from 30 to 120 seconds and examined ex-situ at 30 second interval by TEM, AFM and SEM.

Figure 2 a-f represents a topographic AFM study of various etch times for the PMMA removal step. It can be seen that the plasma etch does not damage the pattern and the fingerprint pattern is maintained. The height difference in the pattern (between light and dark stripes) increase through the etch times from 6 to 30 nm showing that PMMA removal is

taking place. It should be noted that this height difference is not quantitative because it cannot be proven that the tip reaches the silicon substrate from which it may be blocked by the topography of the film produced by etching. However, it is close to what might be expected if the PMMA is removed with an etch selectivity of 3.5. The removal of PMMA can be confirmed by SEM. In Figure 3(a) a 70° tilt cross SEM image displays the structure of a PS-*b*-PMMA film after 120 seconds exposure to RIE. Figure 3(b) shows a higher resolution SEM image where the average size of the PS features can be estimated as about 19 – 20 nm. It was not, however, possible to ascertain from the SEM images whether a residual layer of PMMA remained or that silicon had been removed.

To obtain a more quantitative insight into the PMMA removal step, it was necessary to use cross sectional TEM to resolve the end point of the etch. The end point is the etch time that corresponds to the complete removal of PMMA but no (or only a vanishingly small amount of) silicon is removed. This is critical because as much PS must remain as possible so that the pattern can most effectively be transferred. The PS height defines the maximum feature depth that can be achieved in a plasma etch process. Figure 4(a)-(d) represents the TEM cross section at various time intervals throughout the PMMA removal etch process. It should be noted that these samples need to be very carefully prepared to ensure that the arrays of interest are propagating towards the incident beam. This was not always possible and ‘ghosting’ of the images occurs because of non-perfect alignment (see e.g. Figure 4(d)). It is clear that the silicon-polymer interface can be readily observed in these images. At 30 second etch time, the removal of PMMA can be detected by the emergence of etch pits. These become more apparent at longer etch periods. These etch pits are rounded at the base and this becomes quite pronounced at longer times. The origin of the rounding may result from the diffusion of gas species or from the nature of the electric fields gradients within complex narrow feature size trenches. These two effects can change species densities etc. across the feature base and re-deposition of polymer components at the sidewalls may occur. It might be noted that this re-deposition problem might be expected to be more pronounced in these complex fingerprint patterns than might be expected from idealised directed structures where the lines are parallel. Rounding may also be exacerbated by PS block penetration into the edges of the PMMA feature. It should be noted that the etch rates of both PS and PMMA appear to have increased during the 60 to 90 second interval suggesting that the etch rate is not linear. This is confirmed in Figure 5 which displays plots of the PS and PMMA thickness as a function of etch time. Variation in etch efficiencies with time are typical of many processes and probably result from variations in etch species resulting from plasma stabilization after being struck. After etching for 120 seconds it can be seen that the features have almost reached the silicon surface with only a residual layer of thickness 1-3 nm remaining. This probably represents the remnants of polymer brush. The final PS thickness is only some 14 nm and this is inconsistent with the etch selectivity optimised by use of the homopolymer films. An etch selectivity of 3.5 for a film of 56 nm would suggest the PS would be around 40 nm thick at the end point. Indeed, the data shown in Figure 5 and indicates that high etch selectivity is maintained only for the first 60 s of the etch. The accelerated removal of PS with time could result from plasma variations with time or from differences in homopolymer properties compared to the block copolymer. We would suggest

a simple explanation where products of the PMMA removal increase with time and these species assist PS removal. The relatively poor etch selectivity observed in these structures represents a significant challenge for etch processing to generate very small structures because thin resist layers will be required.

An important point to note that the etch anisotropy is excellent. The width of the PS features after PMMA removal is estimated at 19 nm compared to the feature size of unetched blocks of 22 nm. This is close to the value estimated by SEM (Figure 3(b)). Thus only some 1.5 nm of the etch process is removed from each side of the PS block. Considering some polymer chain inter-penetration occurs, sidewall removal is negligible in this process.

The ability to selectively etch these structures is a precursor to pattern transfer to the substrate as the PS structure will form a resist during silicon removal in an ICP etch as described in detail below. It also allows direct (secondary) electron microscopy imaging of the self-assembled polymer structures. The ability to pattern over a range of BCP molecular weights is shown in Figure 6. As can be seen, the molecular weight of the blocks determines the feature size. Analysis of the images shows that the variation in feature size is 44 nm (90 k-85 k), 32 nm (52 k – 52 k), 20 nm (37 k – 37 k) and 11 nm (18 k – 18 k). It should be noted that the PS-*b*-PMMA (18 k – 18 k) system provided almost ideal straight line patterns using normal procedures. This was found to be highly reproducible. It appears that at these small polymer chain lengths that the random coil structure of the blocks is becoming highly extended allowing more ordered arrangements of the micro-phase separated structures.

Figure 7 shows SEM and TEM images of a fully pattern transferred surface following the silicon plasma etch process and residual PS strip as described above (derived from a PS-*b*-PMMA 37 k – 37 k film). PMMA had been removed using normal etch conditions for 120 s. From the 70° tilt SEM image (Figure 7(a)) it can be readily seen that the etch process has facilitated good pattern transfer. The fidelity of the pattern transfer can be more directly observed using TEM cross-section as can be seen in Figure 7(b). Etch selectivity is high as the 14 nm PS feature remaining from the PMMA removal has resulted of a feature depth of around 32 nm. However, the silicon line features are not as regular as might be hoped. Both the base of the features and the top of the silicon lines are rounded somewhat. The rounding of the features at the base of the silicon lines produced probably reflects the rounding seen in the PMMA removed samples (Figure 4). The rounding of the silicon lines probably results from the rounded PS features seen in Figure 4 as well as only limited etch anisotropy. As discussed more extensively below, the rounding is a result of several processes. Certainly etch selectivity and anisotropy contributes as film thickness variation does. However, dimension and pattern regularity are important as they can determine product removal and re-deposition. The problems associated with using relatively soft resists such as PS at these nanometre dimensions is clear. It should be stressed that although these features have become rounded, dimension control through the silicon pattern transfer has been maintained. The features have an average base width of 19-20 nm in close agreement with the PS feature size noted above.

The same pattern transfer treatment was used to look at the various polymer molecular weights used (18 k – 18 k through to 90 k – 85 k) and the data are described in Figure 8. The feature widths at the base agree reasonably well with the SEM data presented in Figure 6 (42 nm (90 k- 85 k), 33 nm (52 k – 52 k), 19 nm (37 k – 37 k) and 11 nm (18 k – 18 k). This suggests that etch selectivity is high through the feature size regime. It is also apparent from all the TEM images that the crystallinity of the silicon is maintained and there is no indication of amorphitization following the etch processes. This is true of even the smallest features even at the narrowest points of the lines suggesting this is a well optimized process. Two further points may also be noted. For the largest feature size, rounding at the base and the silicon lines is the smallest observed. This suggests our proposed mechanism of diffusion limitations leading to product re-deposition is probably correct. The other point that is important is that rounding appears reduced for the 18 k – 18 k small features. This is again consistent with our mechanism as these straight line features should allow easier gas transport. These data suggest that as feature size is reduced in microprocessors that complex designs will become progressively harder to maintain.

This latter point is confirmed by studies of idealised PS-b-PMMA 37 k – 37 k samples that had been aligned using x-ray interference lithography where the brush is chemically pre-patterned by exposure to the x-rays [31]. SEM and cross-section TEM provide detailed analysis of these samples in Figure 9. SEM data (Figure 9(a)) clearly indicates the line structures which can now be accurately described as nanowires. The width of the wires is consistent with previous measurements at about 20 nm. TEM data (Figure 9(b) through (d)) show the uniformity of the processing. As previously, the crystallinity of the process is maintained. Figure 9(b) shows several nanowires and the first few are indicated by arrows. The dark area between them is metal used in the sample preparation. This and similar images can be used to estimate the reproducibility and regularity of the polymer structure and the processing. The width of 35 nanowires was measured from images using Gigital micrograph GATAN Software. The mean half width of the wires was 17 nm with a standard deviation of 0.56 nm. This can be considered as providing a measure of the line edge roughness (LER about half the standard deviation, 0.28 nm) and reproducibility of the process. Line edge roughness is a critical parameter in device functionality as it determines the drive voltage needed for on-off operation [32]. It is obvious from the images that the shapes are much more regular structures than for the non-aligned systems. Indeed, the top of the wires and the sidewalls show little sign of curvature. The base of substrate between features shows little sign of rounding compared to the previous data and this is consistent with reduced material re-deposition. There is a small slope to the sidewalls indicating some anisotropy but this is much reduced compared to previous. Overall, the regularity of the BCP structure has resulted in dramatic improvement of the etch process.

This work has shown that very small features can be produced in silicon using block copolymer lithography. However, the work has highlighted several issues that will result in challenging demands on the plasma etch processes used in industry. These are discussed in more detail below.

Conclusions and Outlook

The use of self-assembled patterns to generate circuitry is in its infancy and it is clear that block copolymers are showing some promise. Significant developmental work is required to generate large-scale wafer processing techniques of sufficient reliability, reproducibility and predictability if these 'bottom-up' methods are to be commercialised for integrated-circuit manufacture. However, whether resist patterns are generated by these emerging methods or other techniques such as nanoimprint lithography, x-ray lithography, e-beam techniques etc. it is obvious that plasma chemistry and apparatus must be further developed in parallel with the patterning science. This work has shown that very small feature size silicon nanowire structures can be created from conventional plasma etch methods and etches can be developed that are reasonably reproducible and reliable. However, many challenges will need to be addressed if ultra-small feature size nanolithography is to be developed to meet future requirements.

These include:-

- a) It will be necessary to designing circuitry based around on simple structures which allow rapid diffusion of etch gases to prevent re-deposition of products and ensure regularity of structure. This is consistent with industry design changes which have allowed circuitry to be generated from parallel line structures rather than using complex shapes or patterns that were seen as a limitation in self-assembly generated patterns [33].
- b) There will have to be precision end-point control of the etch processes of sensitive materials so that shape control of features is as exact as possible. Techniques such as optical interferometry will need to be extended into the nanometre range to facilitate precise measurement of not only end-point but also defect density in self-assembled patterns [34].
- c) Achieving high etch selectivities or contrasts to allow high aspect ratio features may not be possible using conventional resist materials. This will affect the shape of features particularly at sidewalls etc. The development of novel resists such as metal oxides for patterning of etch sensitive materials such as complex III-V systems is a key challenge for both plasma scientists and chemists [35, 36].
- d) In order to achieve the required etch selectivities and anisotropies, plasma conditions and apparatus will require careful attention to achieve required shape/size regularity. There will be further needs to design new etch chemistries and methods. One of the methods that has attracted some attention has been the development of isotropic etches to reduce feature roughness [37]. New plasma methodologies being developed may be key to generating nanofeatures of required regularity and techniques such as pulsed ICP methods have shown promise [38]. Authors have shown monolayer control of etch depth has been demonstrated using pulsed polymer – deposition steps via modulation of the bias power [39].
- e) The limitations of resist chemistry may require the use of hard masks – materials such as metal oxides whose rate of removal in an etch is very small. This would allow high aspect ratio features to be produced and help improve shape profiles and etch anisotropy. This can be achieved in block copolymer lithography by transferring the

pattern to an underlying oxide prior to etching the material of choice. This is illustrated in Figure 10. In step (b) a hard mask resist layer is deposited onto the substrate. (c) and (d) represent BCP development and selective block removal. (e) and (f) represent pattern transfer to the substrate and resist strip. This hard mask technique may be of particular value to unconventional materials such as Ge and III-Vs which are expected to play important roles in devices due to mobility limitations. In block copolymer lithography, pseudo hard-mask methods may be developed by use of polymer blocks that have hetero atoms included to provide high etch contrast in e.g. RIE etches [40].

It is clear that significant research and development will be required to meet the etch requirements outlined here. Whilst much of the article is focussed in silicon etching, the need to develop non-Si etches of the highest quality will be required. There will be a pressing need to develop etches for non-conventional materials of complex composition and structure which result in high pattern transfer fidelity whilst maintaining that structure and composition of the materials. It is likely in the next few years that plasma science, which has had something of a low profile in the area of microelectronics, will adopt a more significant role in delivering solutions for the nanoelectronics industry.

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Table 1: As-deposited and post etch homopolymer film thickness, etch rates nm min^{-1} , gas flow rates and PS to PMMA selectivity for 2% wt PS and 4% wt PMMA homopolymer films after 1 minute of etching. Etch 3 was used for all diblock copolymer etching. Base Pressure and temperature were set at 10 mTorr and 10 C respectively. Please note that etch rates are measured to an experimental accuracy of around 15 nm min^{-1} . These errors are based on reproducibility of three similar measurements.

RIE power (watt)	O ₂ flow rate (sccm)	CHF ₃ flow rate (sccm)	Etch Time (min)	PMMA etch depth (nm)	PS etch depth (nm)	PMMA etch rate (nm min^{-1})	PS etch rate (nm min^{-1})	PS to PMMA etch selectivity
50	50	0	0.5	150	73	300	146	2.1
60	50	0	0.5	76	54	152	108	1.4
70	70	0	0.5	65	52	130	104	1.3
70	70	0	0.5	149	70	298	140	2.1
150	5	40	1	44.0	18.0	44.0	18.0	2.4
150	25	20	0.75	137.0	56.0	182.7	74.7	2.4
100	10	40	1	54.0	26.0	54.0	26.0	2.1
100	5	40	1	45.0	13.0	45.0	13.0	3.5
100	2	40	1	13.0	5.0	13.0	5.0	2.6
60	5	40	1	21.0	13.0	21.0	13.0	1.6

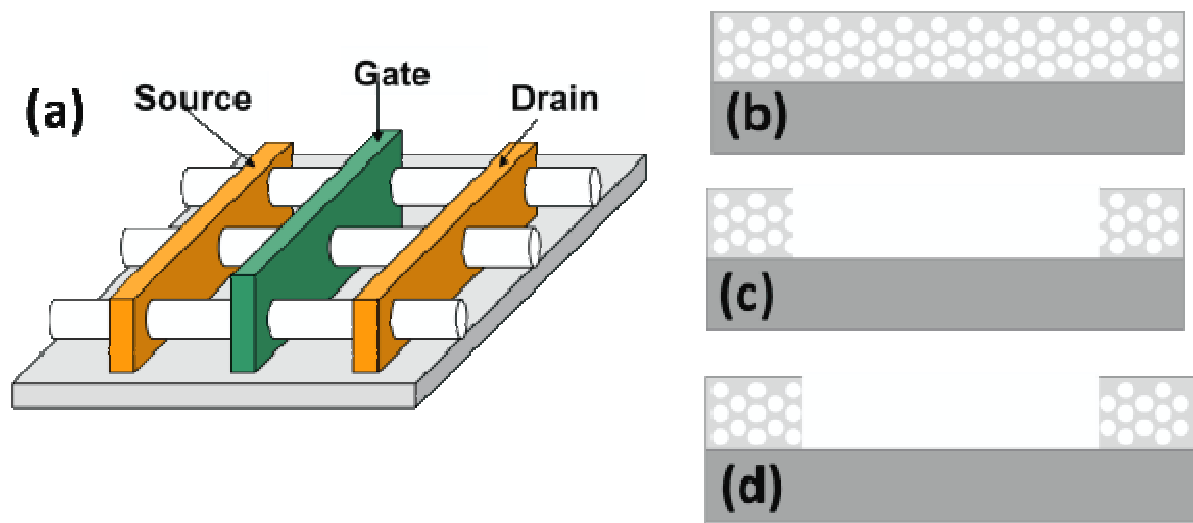


Figure 1: (a) simple schematic of a FIN-FET structure – a proposed novel device structure. (b) through (d) illustration of the challenges in etching porous materials (as illustrated in (a) where etching can leave open (c) or closed pores (d). See text for details.

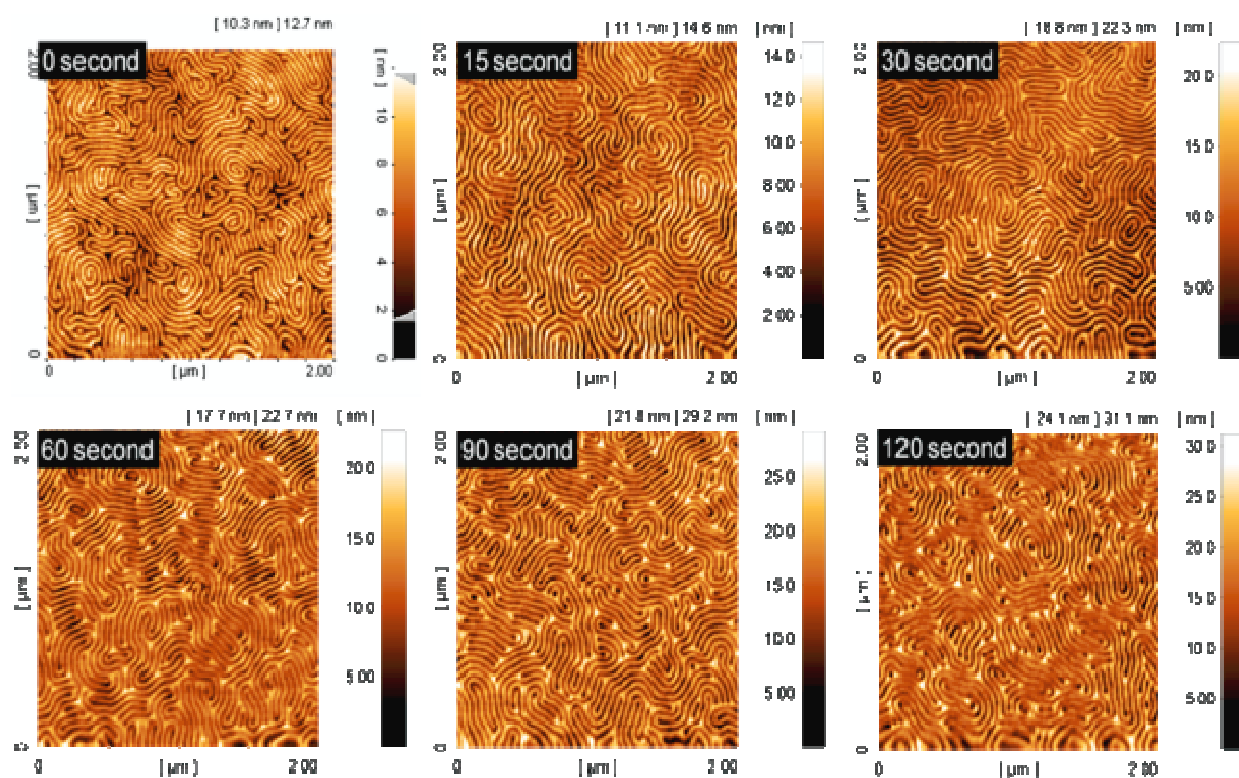


Figure 2: AFM topographic 2 x 2 micron scans for 0, 15, 30, 45 60, 90 and 120 second etch intervals of a 1.5% PS-*b*-PMMA film deposited on a neutral PS-*r*-PMMA brush layer (etch times are shown for each AFM in the figure).

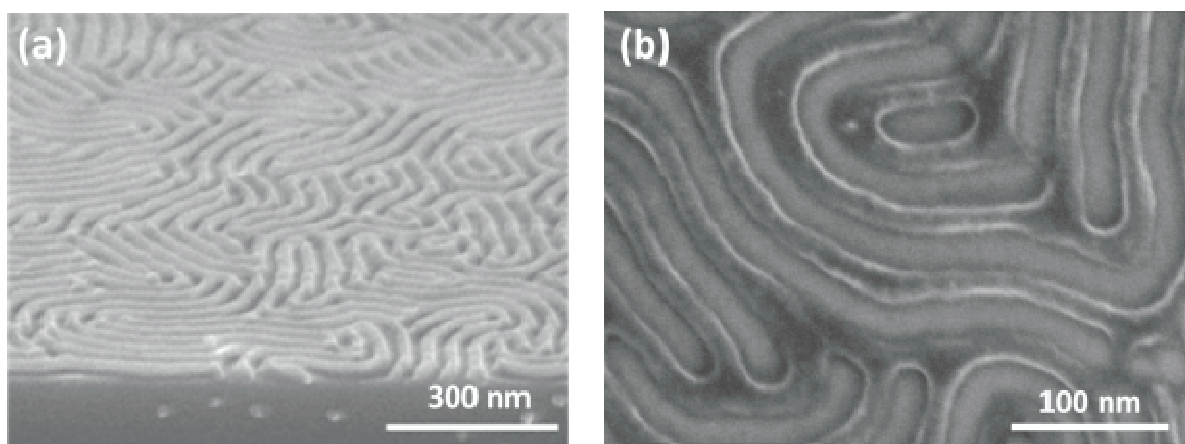


Figure 3: SEM images of PS-*b*-PMMA film after 120 s PMMA etch period. (a) tilt image indicating PS removal and (b) higher resolution top down image.

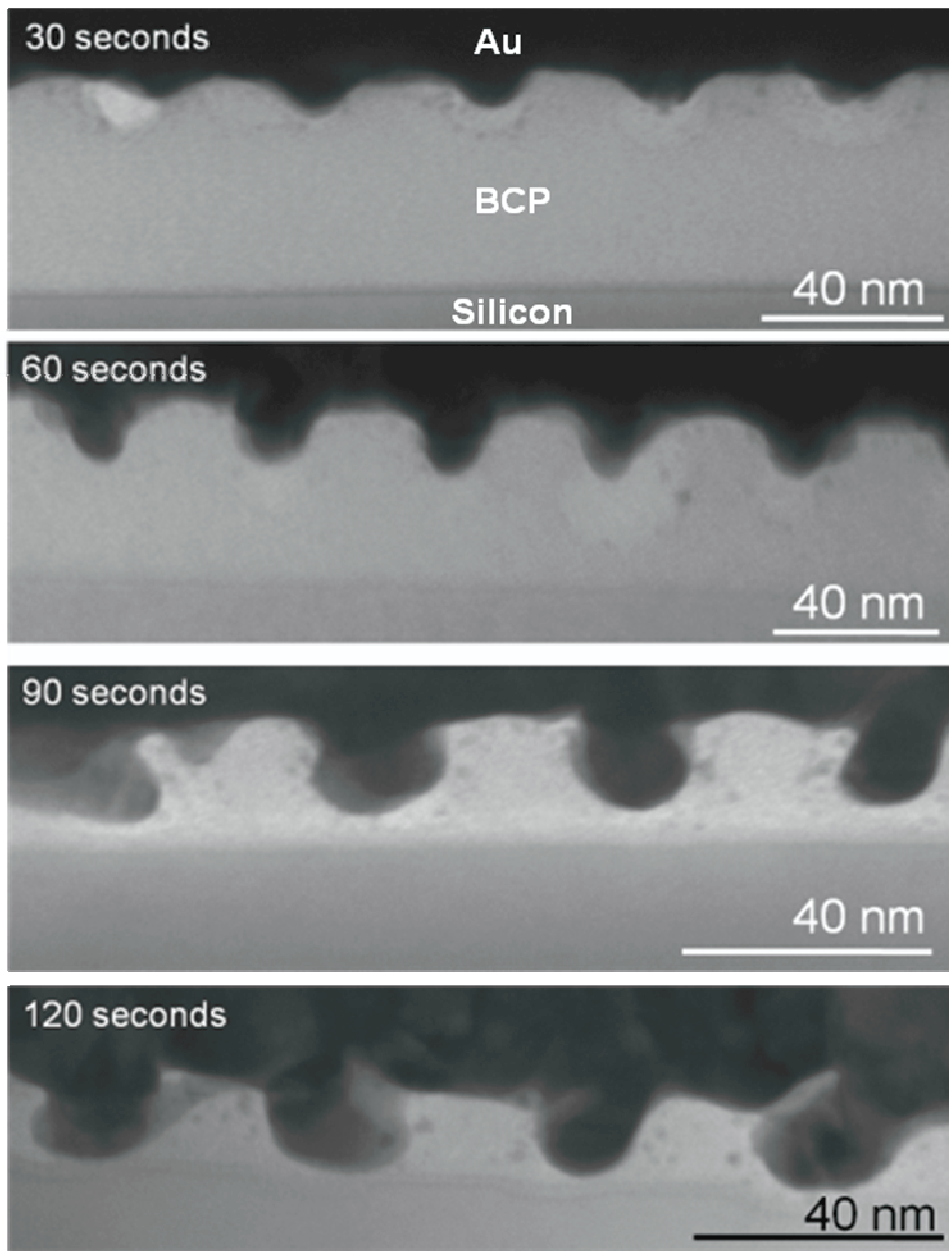


Figure 4: Progressive PMMA removal observed via TEM images of films post 40 sccm $\text{CHF}_3/5$ sccm O_2 RIE plasma etches ((a) to (d) from top to bottom respectively and times illustrated in figure). (a) and (b) the formation of etch pit after 30 and 60 seconds respectively. (c) the formation of well developed etch cavities at the 90 second interval and full removal of PMMA after 120 second (d). Gold metal capping layers ensure that polymer profile is protected from thermal and chemical processing during TEM sample thinning.

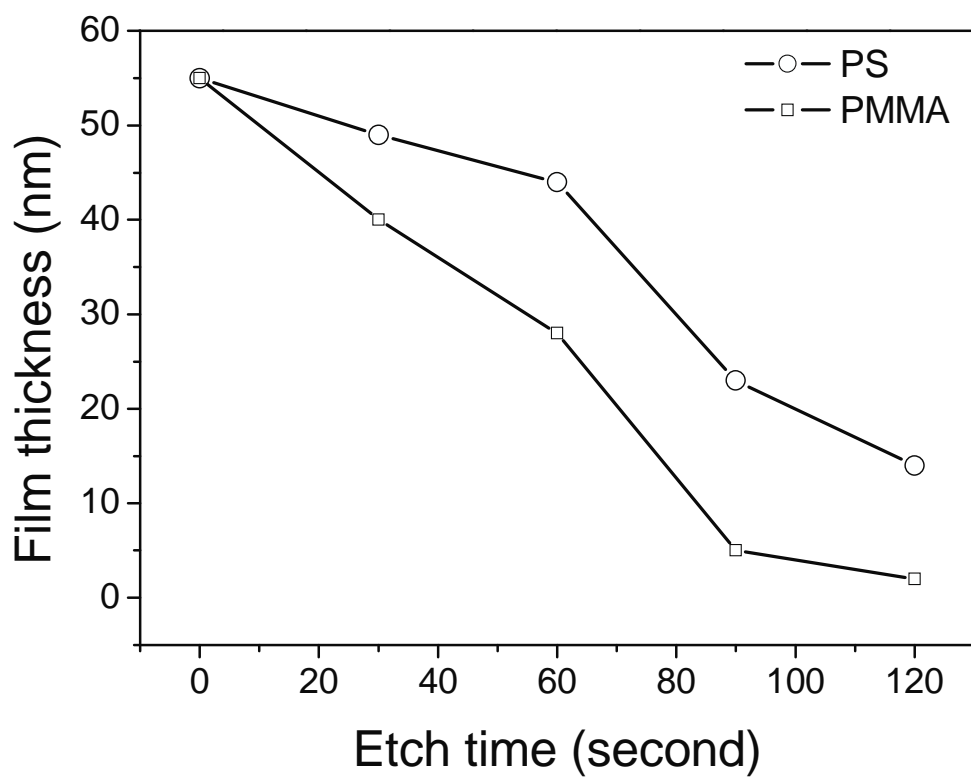


Figure 5: Plot of PS and PMMA film thickness (in a microphase separated BCP film) determined by cross sectional TEM as a function of RIE time for a CHF_3/O_2 etch (see text for details).

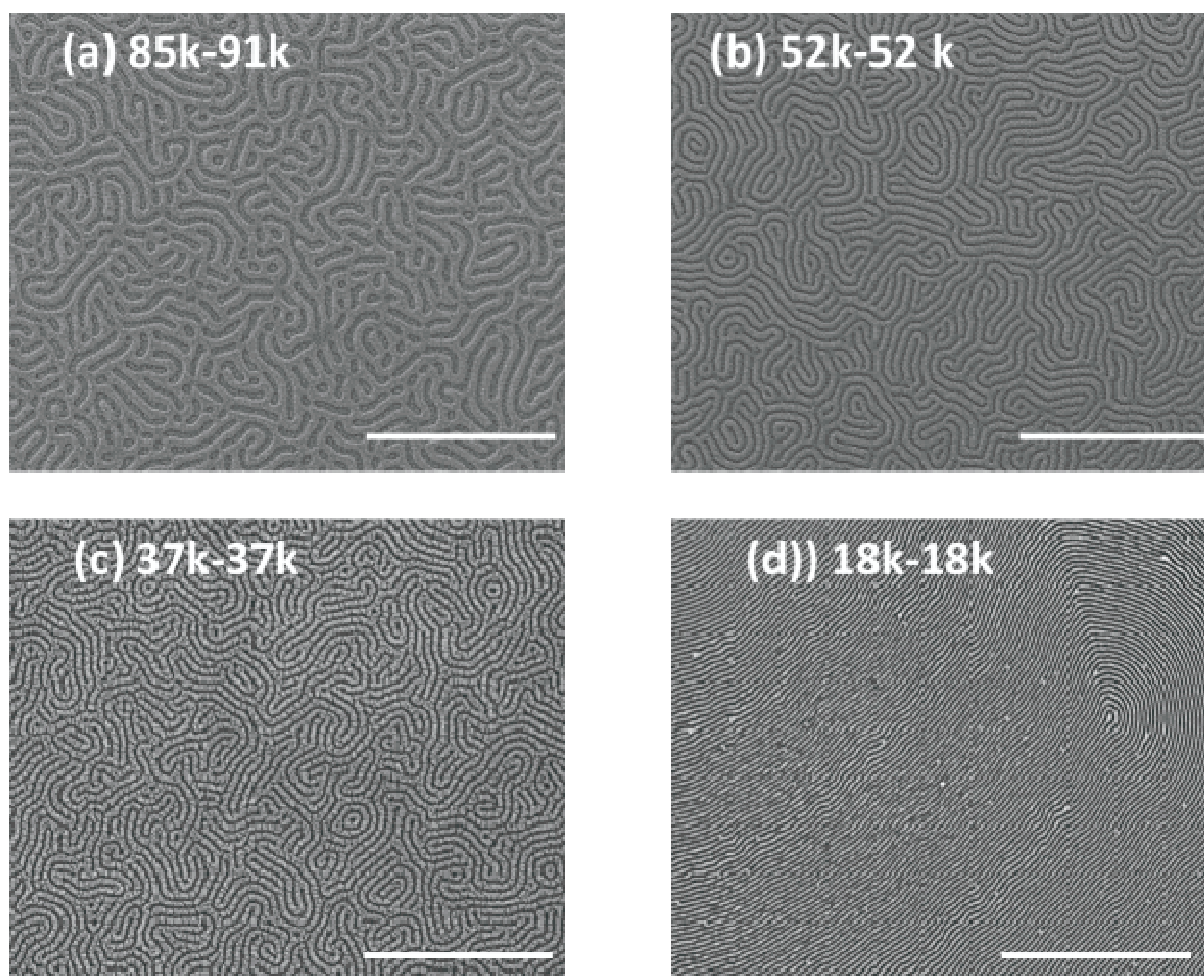


Figure 6: Top down SEM images of BCP patterns of various molecular weight PS-*b*-PMMA films on silicon substrates. Molecular weights as indicated in figures. All scale bars 1 μm .

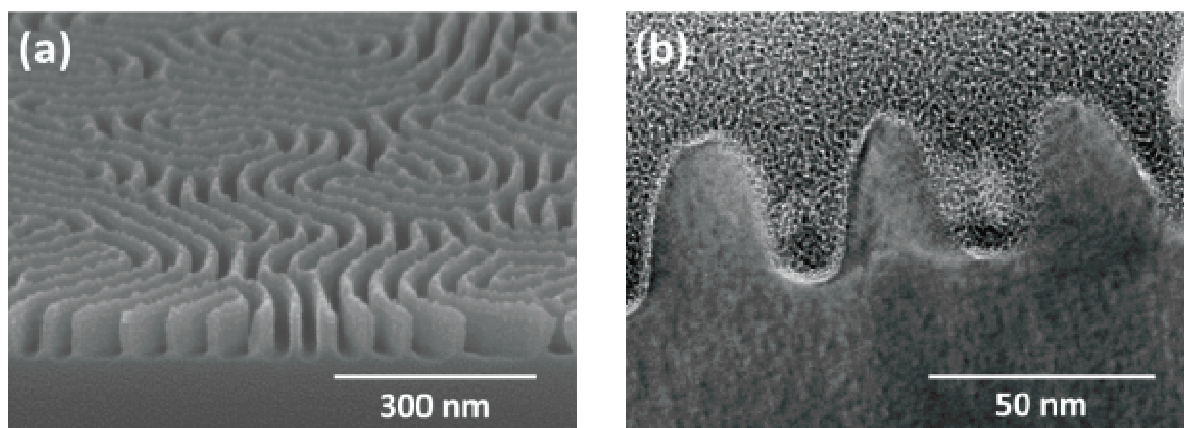


Figure 7: (a) SEM tilt image of pattern transferred polymer pattern. (b) TEM cross-section of same.

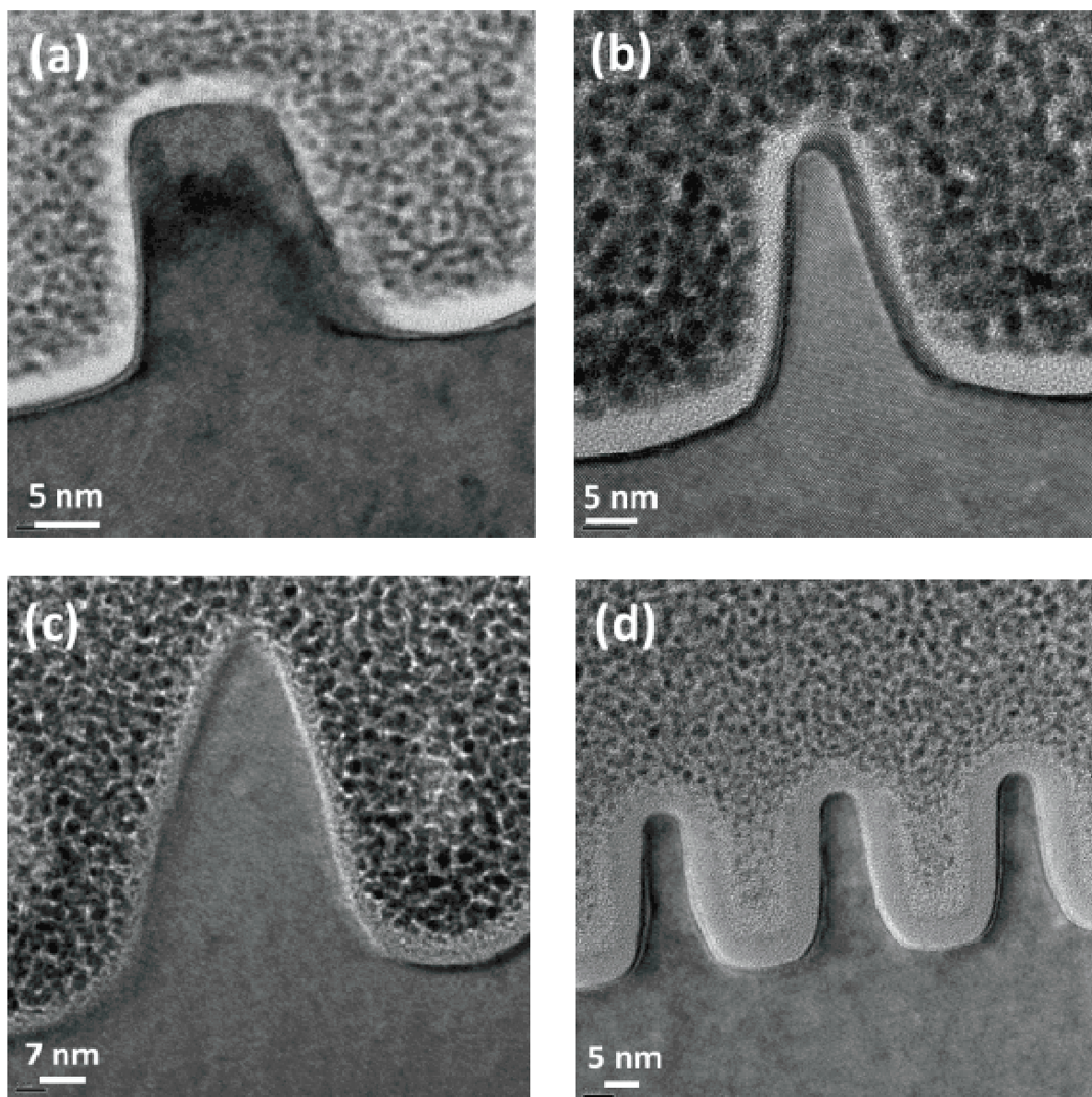


Figure 8: Cross-section TEM images of silicon lines formed via BCP pattern transfer. (a) PS-*b*-PMMA 90 k – 85 k, (b) PS-*b*-PMMA 52 k – 52 k, (c) PS-*b*-PMMA 37 k – 37 k, (d) PS-*b*-PMMA 18 k – 18 k.

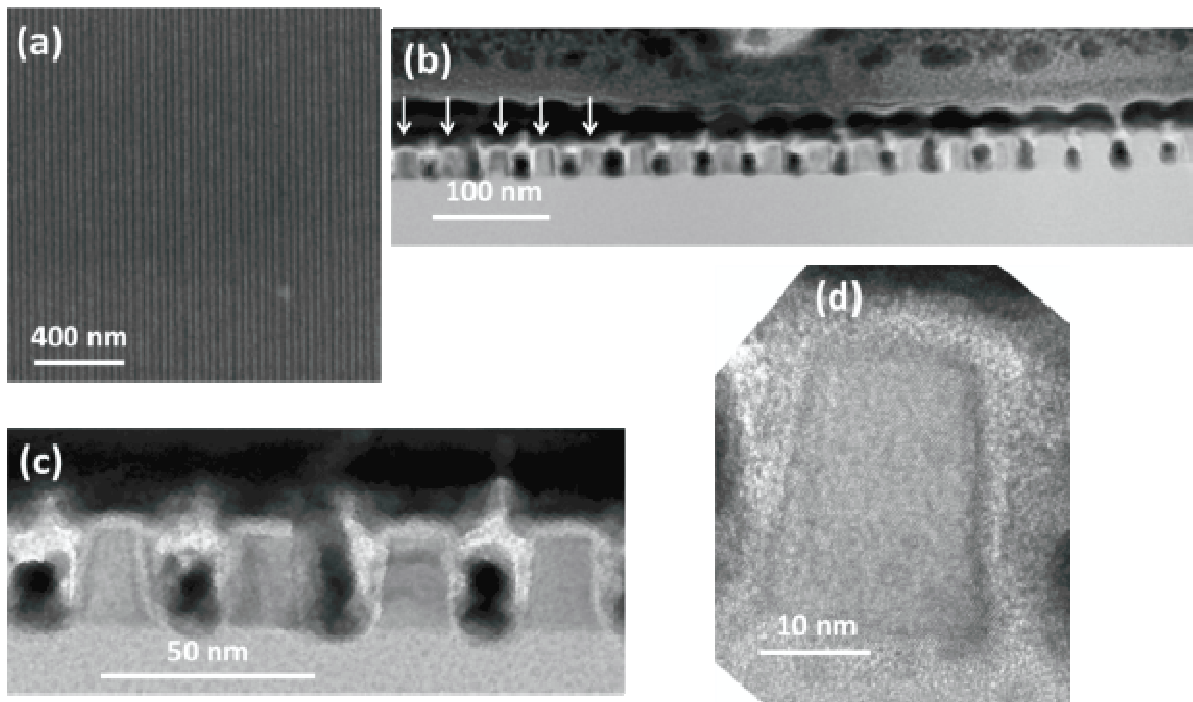


Figure 9: SEM (a) and TEM (b) to (d) of aligned PS-*b*-PMMA silicon nanowire structures developed on silicon-on-insulator substrates by plasma etching processes.

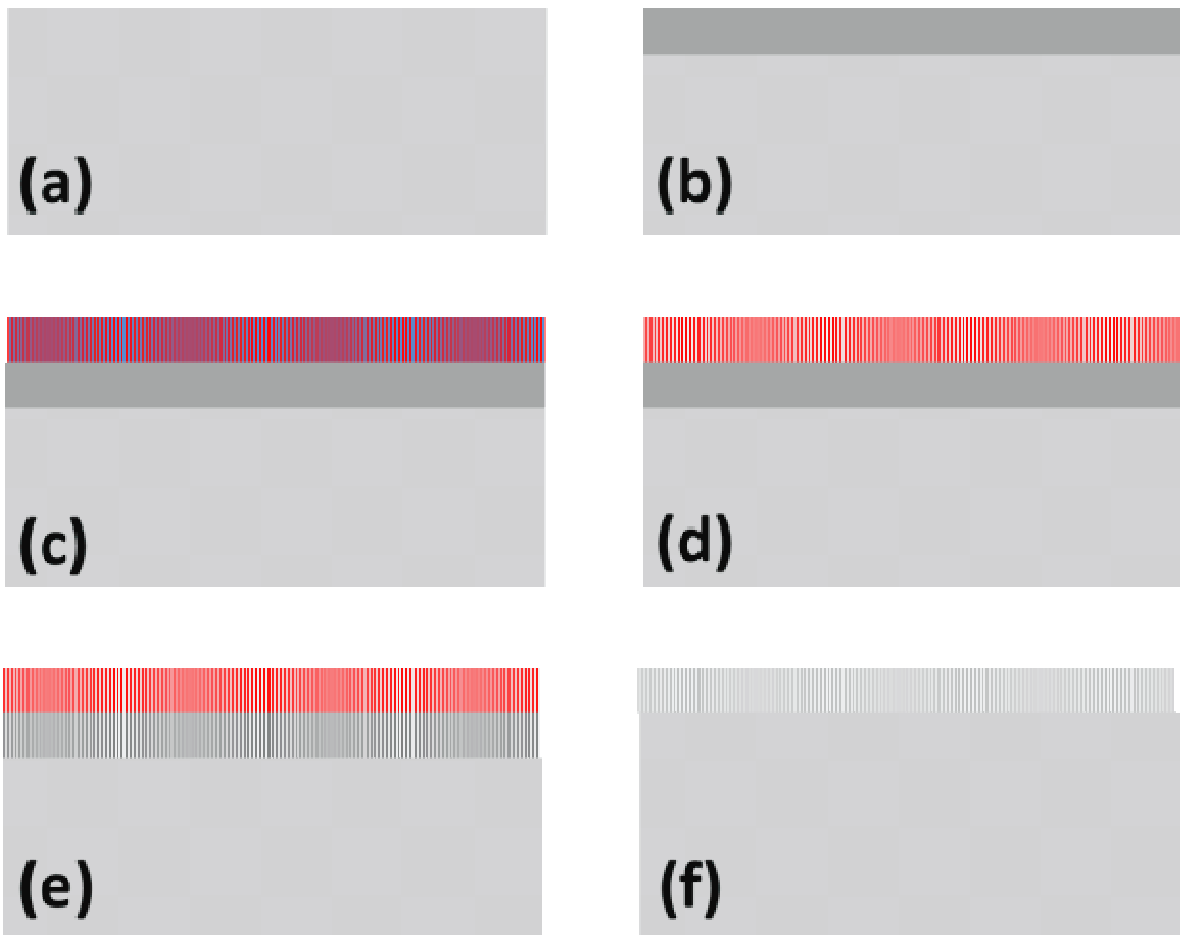


Figure 10: Schematic of how block copolymer lithography could be combined with a hard mask to generate small size features in substrates. See text for details.