



**HAL**  
open science

## First demonstration of heat dissipation improvement in CMOS technology using Silicon-On-Diamond (SOD) substrates

J.-P. Mazelier, J. Widiez, F. Andrieu, M. Lions, S. Saada, M. Hasegawa, K. Tsugawa, L. Brevard, J. Dechamp, M. Rabarot, et al.

### ► To cite this version:

J.-P. Mazelier, J. Widiez, F. Andrieu, M. Lions, S. Saada, et al.. First demonstration of heat dissipation improvement in CMOS technology using Silicon-On-Diamond (SOD) substrates. IEEE International SOI Conference, Oct 2009, Foster City, United States. 10.1109/SOI.2009.5318735 . hal-00604213

**HAL Id: hal-00604213**

**<https://hal.science/hal-00604213>**

Submitted on 29 Sep 2023

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

# First demonstration of heat dissipation improvement in CMOS technology using Silicon-On-Diamond (SOD) substrates

J.-P. Mazellier<sup>1,4</sup>, J. Widiez<sup>1</sup>, F. Andrieu<sup>1</sup>, M. Lions<sup>1,2</sup>, S. Saada<sup>2</sup>, M. Hasegawa<sup>3</sup>, K. Tsugawa<sup>3</sup>, L. Brevard<sup>1</sup>, J. Dechamp<sup>1</sup>, M. Rabarot<sup>1</sup>, V. Delaye<sup>1</sup>, S. Cristoloveanu<sup>4</sup>, L. Clavelier<sup>1</sup>, S. Deleonibus<sup>1</sup>, P. Bergonzo<sup>2</sup>, O. Faynot<sup>1</sup>

(1) CEA-LETI MINATEC, 17 rue des Martyrs, 38054 Grenoble, France. Email: françois.andrieu@cea.fr

(2) CEA- LIST, Gif-sur-Yvette, France (3) AIST NTRC, Tsukuba Central, 305-8565, Japan (5) IMEP-LAHC, Grenoble, France

## Abstract

We have fabricated Silicon-On-Diamond (SOD) substrates on which, for the first time, we integrated n and p Fully Depleted MOSFETs high-K/metal gate down to 200nm gate length. The devices show excellent electrical characteristics and a 57% improvement of the thermal resistance compared to the co-processed one on standard SOI.

Process #A consists in a silicon carburation step in a CH<sub>4</sub>-rich H<sub>2</sub> plasma, which precedes an in situ nucleation step under bias (Bias Enhanced Nucleation, BEN [6,7]) whereas process #B starts with a spin-coating of nanodiamond crystallites on Si [5]. For both techniques, the following growth step is done in CH<sub>4</sub>-poor H<sub>2</sub> plasma.

## Introduction

Due to the increasing 2D or even more 3D integration density, thermal management is considered as a major challenge for power, light devices as well as for advanced CMOS high performance technologies [1]. Indeed a high operation temperature reduces both performance and reliability. This is especially true for devices on standard Silicon-On-Insulator (SOI), which suffer from the low Thermal Conductivity (TC) of the buried SiO<sub>2</sub> (TC=1.4 compared to 148 W/mK for Si). Some theoretical studies already proposed to deal this challenge at the device level, e.g. by integrating a buried material like diamond [2,3], which exhibits a record of TC=2000 W/mK and a good electrostatic trade-off for thin films electron devices thanks to a 5.5 relative permittivity.

In this study, we detail the fabrication of SOD substrates and the electrical and thermal performances of n&pMOSFETs integrated on these wafers.

## Diamond synthesis

In this study, we compare two undoped diamond CVD techniques (referred as #A and #B), which mainly differ by the diamond seed formation and the process temperature (see details in Table 1 and [4,5]).

	Process #A	Process #B
Carburation	CH <sub>4</sub> /H <sub>2</sub> (10/90 %) 26mBar, 120sccm 950W, 720°C	None
Seeding	BEN (-307V) CH <sub>4</sub> /H <sub>2</sub> (10/90 %) 26mBar, 120sccm 950W, 750°C	Nanoseeding 5nm seeds, ultrasonication
Nucleation density	~10 <sup>11</sup> cm <sup>-2</sup>	~10 <sup>11</sup> cm <sup>-2</sup>
Growth	CH <sub>4</sub> /H <sub>2</sub> (0.6/99.4 %) 35mBar, 250sccm 1100W, 820°C	CH <sub>4</sub> /CO <sub>2</sub> /H <sub>2</sub> (5/5/90%) 0.2mBar, 100sccm 1100W, 370°C

Table 1. Main parameters of both #A and #B processes used for deposition of thin CVD diamond films in this study

## SOD substrate and MOSFET processing

We have used such films, with thickness between 200-400nm, in order to fabricate SOD substrates by using BESOI technique [2,8]. A scheme of the process is described in Figure 1. Note that top silicon layer thickness is about 70nm. We have integrated MOSFETs with a high-K/metal gate in order to characterize the performance of our processed substrates. Standard SOI substrates (Top silicon 70nm, BOX SiO<sub>2</sub> 145nm) have been co-processed for reference. A TEM cross-section view of a MOSFET device processed on SOD substrate is given in Figure 2.

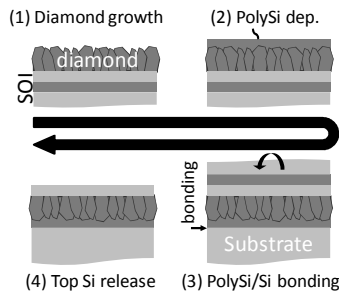


Figure 1. BESOI integration to fabricate SOD substrates. CVD Diamond is grown on high quality SOI substrate and capped with polysilicon for bonding purpose. After bonding, substrate and BOX of initial SOI are removed to release to silicon layer of SOD.

## Electrical characterization

Electron and hole mobilities in the MOSFET channel have been extracted by the Split-CV method. The mobilities are similar whatever the diamond deposition process used and are as high in SOD as in SOI (Figure 3). This is consistent with the numerous physical analyses performed on SOD substrates of either type #A or #B (not shown here): SIMS measurement show neither noticeable carbon nor hydrogen diffusion in the top silicon layer; Raman spectroscopy reveals no strain in top silicon; no degradation in crystalline top silicon film is noticeable in HRTEM pictures. We have also demonstrated functional devices down to 200nm gate

length (see the Id-Vd curve in Figure 3 and the TEM in Figure 2).

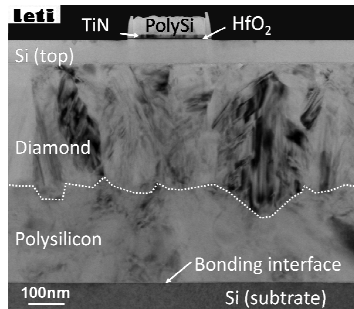


Figure 2. TEM cross-section view of a FD transistor processed on SOD (#A) substrate. The gate length is 200nm and the top silicon is 70nm thick. The gate stack is 3nm HfO<sub>2</sub> / 10nm PVD TiN / 50nm LPCVD polysilicon.

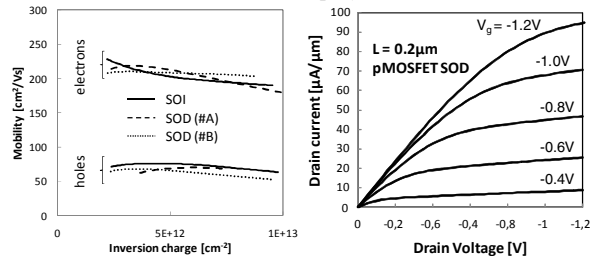


Figure 3. Left: Electrons and holes mobility in front channel measured by Split-CV method at room temperature measured at 100µm gate length. Right: I<sub>d</sub>(V<sub>d</sub>) of pMOSFET w/ 200nm gate length on SOD #B.

### Thermal performance

We have measured the out-of-plane effective Thermal Conductivity (TC) of 220nm thin CVD diamond film by the 3ω method (Figure4-left) [9]. We found TC<sub>eff</sub>=11.3W/mK (for diamond #A). This value is consistent w/ literature results but lower than the thermal performance of bulk diamond (Figure4-right). The first reason is that this value integrates the thermal resistances of the diamond/Si interfaces. The second is relative to the lower size of the diamond crystallites in the first 100nm of the deposited diamond. Grain boundaries indeed lower the TC of diamond. Nevertheless, finally, 200nm thin diamonds are about one decade better than a thermal oxide at the same thickness (1.3W/mK) (Figures 4).

We have also measured the thermal resistance (TR) of the *integrated* SOD substrates thanks to 4-contacts gate lines, used as heat source and thermometer (see insert of Figure 5). This resistance is plotted for different line widths in Figure 5. For large devices, we get the same R<sub>th</sub> whatever the substrate because the 725µm thick silicon substrate limits the thermal dissipation (quasi-1D regime). When the width is shrunk, higher R<sub>th</sub> are obtained because of a typical 2D effect. In the sub-10µm line width region, SOI impedes greatly the heat removal because of the SiO<sub>2</sub> thermal barrier. On the other hand, SOD exhibits up to 57% lower R<sub>th</sub> than SOI. These

measurements are consistent with the aforementioned characterisations of thin diamonds (Figures 4) and demonstrate that the thermal impact of the material just below the active region is crucial for smaller devices. Finally, one can see that the thermal performance is quite similar for type #A and #B. This could be interpreted by similar grain properties of the diamond layers, at least in the first 100nm close to the top Si.

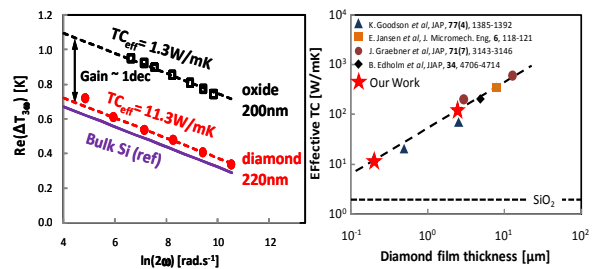


Figure 4. Left: Effective TC extraction using 3ω method. Right: Evolution of diamond TC with thickness.

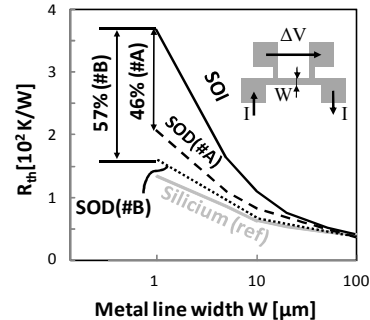


Figure 5. Thermal resistance of different substrates vs. the typical dimension of the tested structure (metal lines).

### Conclusion

We fabricated Silicon-On-Diamond substrates with different high-quality CVD diamond films. For the first time, high-K/metal gate devices have been processed on these SOD substrates. They highlight excellent electrical characteristics (carrier mobility as high as on SOI) and greatly improved thermal performances (-57% reduction of the thermal resistance, compared to standard SOI). To our knowledge, it is the first demonstration of such thermal improvement of SOI CMOS devices with alternative material BOX.

### Acknowledgement

This work was supported by the French National Research Agency (ANR) through Carnot funding.

### References

- [1] C. Chen, ISSCC'06 ; [2] B. Edholm *et al.*, SOI Conference 1997 ; [3] J. Zimmer *et al.*, CS Mantech Conf 2008 ; [4] S. Saada *et al.*, PSS(a) 2007 ; [5] K. Tsugawa *et al.*, New Diamond and Carbon Tech. 2006 ; [6] Yugo *et al.*, App. Phys. Letters, 1991 ; [7] M. Lions *et al.*, PSS(a) 2009 ; [8] J. Widiez *et al.*, SSE 2009 [9] S.-M. Lee *et al.*, JAP 1997.