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Demonstration of low leakage current and high polarization in ultrathin AlN/GaN high electron mobility transistors grown on silicon substrate

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High quality AlN/GaN heterostructures grown on silicon substrate are demonstrated. It is found that high carrier concentration can be achieved whereas circular diodes showed a low leakage current up to 200 V reverse bias. 200 nm gate length AlN/GaN transistors exhibited a drain current density of 1.3 A/mm with a pinchoff leakage current below 20 μA/mm and a record GaN-on-silicon extrinsic transconductance of 470 mS/mm. These results demonstrate the possibility to achieve a unique combination of large polarization with a barrier thickness as low as 3 nm while preserving a remarkably low device leakage current without using any gate insulator. © *2011 American Institute of Physics*. [doi:10.1063/1.3595943]

To extend GaN-based high electron mobility transistor (HEMT) frequency operation, the device dimensions need to be reduced. In particular, the gate length scaling must be linked to the reduction in the gate to channel distance in order to avoid short channel effects.[1] Additionally, high current density should be maintained while downscaling the device geometry. Unlike GaAs or InP-based devices, gate recess etching in GaN-based is difficult to control since no chemical etchant is known to have a significant etch rate on GaN-based materials. On the other hand, dry etching generally generates defect states that may induce damage, high gate leakage current, and thus reliability issues. Furthermore, decreasing the AlGaN barrier thickness below 10 nm leads to a strong degradation of the two-dimensional electron gas (2DEG) carrier concentration,[2,3] resulting in poor device performance. In this frame, AlN/GaN heterostructure is becoming of high interest because of its theoretical 2DEG density that may exceed $5\times10^{13}/\mathrm{cm}^2$ and the possibility to achieve a high current density while using an ultrathin barrier layer,[4–7] allowing a high aspect ratio (gate length on gate to channel distance). The outstanding potential for high frequency operation of ultrathin Al-rich barrier GaN devices has been already demonstrated.[8,9] However, the gate leakage current in ultrathin GaN-based barrier layers remains a serious concern and gate insulators are generally used to reduce the gate tunneling current.[10,11] Nevertheless, the use of a dielectric on top of the barrier layer as gate insulator has several drawbacks; (1) this increases the total barrier thickness resulting in transconductance and thus radio frequency performance degradation, especially for deep submicrometer gate lengths and (2) this may also induce device stability issues due to the barrier layer/dielectric interface contamination.[12] Furthermore, GaN devices could also be cost effective for large market adoption as the unique possibility to grow advanced heterostructures on large diameter Si substrates, up to 150 mm has been demonstrated.[13]

In this letter, a high quality ultrathin barrier AlN/GaN HEMT structure grown on Si substrate is demonstrated. It is shown that this unique planar 3 nm barrier thickness technology allows both a high sheet carrier density and a low leakage current, resulting in a record transconductance of GaN-on-Si III-nitride HEMTs.

The AlN/GaN heterostructures (see inset of Fig. 1) were grown by metal-organic chemical vapor deposition (MOCVD) on a highly resistive (>5000 Ω cm) 4 in. Si (111) substrate. Standard high temperature AlN nucleation layer, a single AlGaN intermediate layer and a 1 μm GaN as buffer layer[14] have been used followed by a 3.0 nm ultrathin AlN barrier layer and a 5.0 nm thick *in situ* Si_3N_4 cap layer. Thin film thicknesses have been calibrated by transmission electron microscopy. Atomic force microscopy (AFM) has been used to reveal the surface morphology of the SiN/AlN/GaN-on-Si heterostructure (Fig. 1). Excellent root-mean-square (rms) roughness of 0.25 nm and 0.35 nm are observed in a 1×1 $\mu\mathrm{m}^2$ and 5×5 $\mu\mathrm{m}^2$ area, respectively. The *in situ* SiN layer allows for handling the strain relaxation resulting from the high tensile stress of the AlN barrier layer with the GaN layer, giving rise to a high surface quality. It has to be pointed out that the use of similar growth conditions without *in situ* SiN cap layer results in surface cracks and higher rms

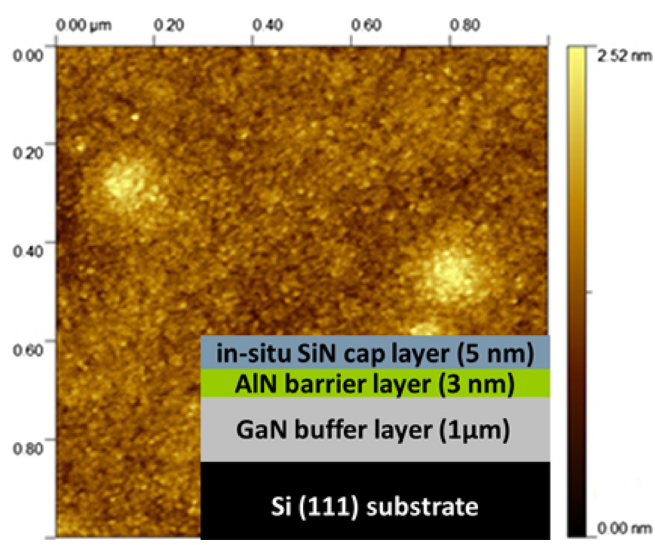

FIG. 1. (Color online) AFM top view in a 1×1 $\mu\mathrm{m}^2$ area showing the surface morphology of SiN/AlN/GaN grown on Si substrate; the schematic cross section of the structure appears in the inset.

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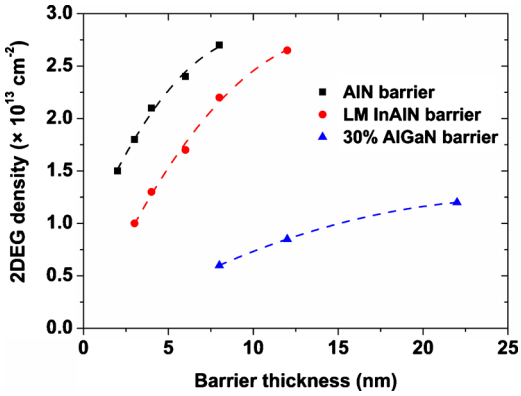

FIG. 2. (Color online) Room temperature 2DEG carrier density measured by Van Der Pauw method of SiN/AlN/GaN, lattice matched $In_{0.17}Al_{0.83}N/GaN$, and $Al_{0.3}Ga_{0.7}N/GaN$ heterostructures as a function of the barrier layer thickness.

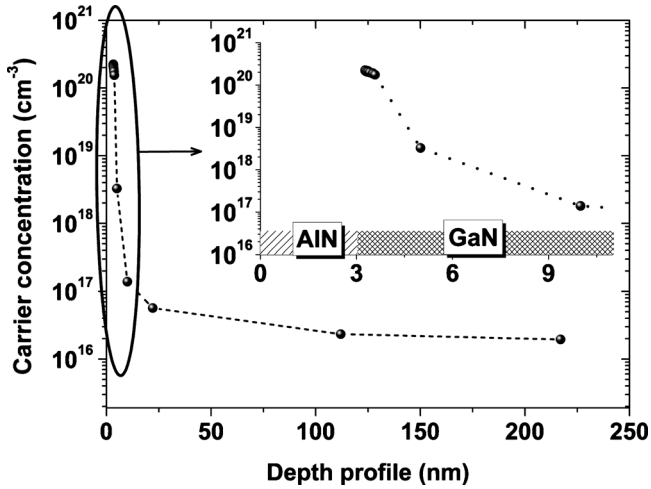

FIG. 3. Carrier density profile of AlN/GaN-on Si HEMT structure. The inset shows the first 10 nm of the carrier profile indicating a sharp carrier confinement and high polarization at the AlN/GaN interface.

roughness. Additionally, the *in situ* SiN cap layer acts as a passivation layer and thus significantly reduce the effect of the surface charges, consequently preventing the 2DEG depletion from the surface.[15]

Room temperature Van Der Pauw–Hall measurements have been performed as a function of the barrier layer thickness on various heterostructures in order to benchmark the SiN/AlN/GaN in term of 2DEG properties (Fig. 2). In all cases, the mobility ranged between 1100 and 1550 $cm^2/V\,s$ showing that a high interface quality is maintained into the heterostructure. In agreement with previously reported results,[2] the commonly used $Al_{0.3}Ga_{0.7}N/GaN$ HEMTs show a 2DEG density well below 10^{13} cm^{-2} with barrier thicknesses lower than 10 nm. As expected from their wider band gap and thus higher spontaneous polarization as compared to $Al_{0.3}Ga_{0.7}N/GaN$ HEMTs, much higher carrier concentration is found in the case of $In_{0.17}Al_{0.83}N/GaN$ HEMTs. However, it clearly appears that the widest known III-nitride AlN band gap (6.2 eV) enables to achieve superior 2DEG properties resulting in a significant carrier concentration even when using barrier thicknesses below 5 nm.

The device fabrication has been performed as follows: Ohmic contacts were formed directly on top of the 3 nm thick AlN barrier layer by etching the *in situ* Si_3N_4 layer. A Ti/Al/Ni/Au metal stack has been used, followed by an annealing at 900 °C in N_2 ambient. Device isolation was obtained by He implantation. The extracted contact resistance was 0.65 Ω mm. Gate lengths of 0.2 μm were defined by conventional e-beam lithography. The SiN underneath the gate was fully removed using a low power SF6 plasma that yields in an etching selectivity between the SiN and the AlN materials of a factor 90. This allows both to stop accurately on the 3 nm AlN barrier layer and to avoid implantation of fluorine ions, which is detrimental for the 2DEG carrier concentration. Ni/Au (40 nm/400 nm) gate metals were then deposited. The gate-source and gate-drain spacing were 0.4 μm and 1.3 μm, respectively, and the device width was 50 μm. Finally, 200 nm plasma-enhanced chemical vapor deposition Si_3N_4 has been deposited as passivation layer. 50 μm diameter Ni/Au circular diodes have been fabricated on the same mask set.

Capacitance-voltage and current-voltage measurements have been carried out on 50 μm diameter circular diodes. Figure 3 shows the typical carrier density profile of the AlN/GaN-on-Si HEMT structure. A high carrier concentration is observed at the AlN/GaN interface and a low background carrier density is seen at the bottom of the GaN buffer layer, indicating a sharp carrier confinement. The inset shows a closer view of the first 10 nm of the carrier profile, confirming the high polarization between the 3 nm AlN barrier thick and the GaN buffer layer. Figure 4 depicts the current-voltage characteristic of the same circular diode in semilogarithm and linear scale. Forward diode characteristic extraction indicates an ideality factor of 1.35 and a barrier height of 1.2 eV, in agreement with the reported barrier height of Ni on strained $Al_{0.25}Ga_{0.75}N/GaN$ HEMTs.[16] A remarkably low leakage current is observed reproducibly up to 200 V reverse bias indicating that no electron tunneling occurred through the 3 nm ultrathin barrier layer. This is attributed to the absence of defects into the AlN film resulting from the high growth quality as well as the AlN surface quality enhanced by the *in situ* grown SiN that prevents oxide and/or defects formation inducing generally parasitic conductions.

Figure 5 shows typical transfer characteristics of a 0.2 × 50 μm^2 AlN/GaN HEMT on Si at $V_{DS}=10$ V. A high maximum dc output current density exceeding 1.3 A/mm at $V_{GS}=+2$ V is obtained. The extrinsic transconductance (g_m) peaks at 470 mS/mm at $V_{GS}=-1$ V, which is beyond the

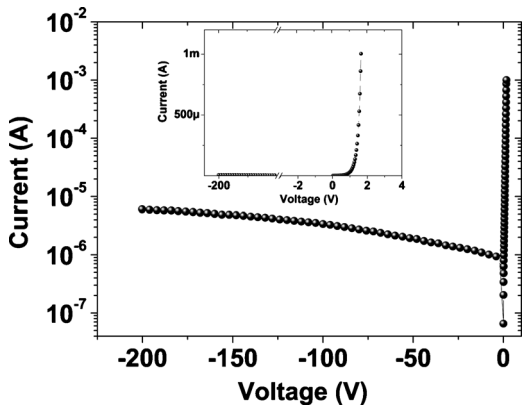

FIG. 4. 50 μm circular diode characteristic of 3 nm barrier thickness AlN/GaN-on Si HEMT structure revealing a low leakage current up to 200 V reverse bias.

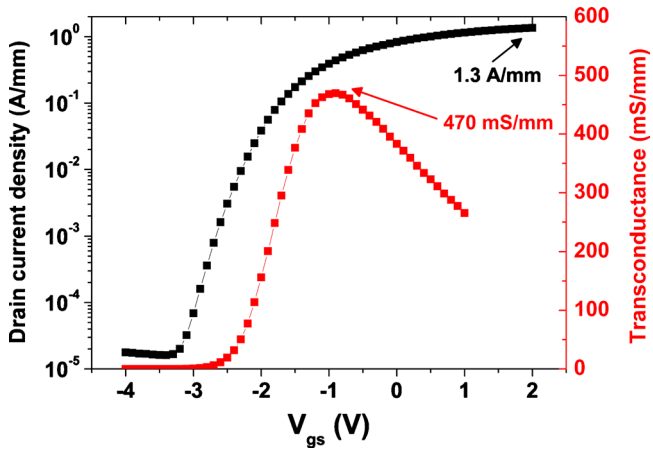

FIG. 5. (Color online) Transfer characteristics of the $0.2\times 50\ \mu m^2$ SiN/AlN/GaN HEMT on silicon substrate, demonstrating a record extrinsic transconductance of GaN-on-Si HEMTs.

highest value of any GaN-based HEMT structure grown on Si substrate. The record g_m results from the combination of a high 2DEG density and a short gate to channel distance. The low leakage current observed on circular diodes is confirmed at the transistor level with a gate and drain leakage currents of less than 20 μA/mm. Consequently, this technology allows achieving a high aspect ratio, a high current density, and a low leakage current while avoiding gate recess and gate insulator that are difficult to control and generally induce device stability issues.

We have demonstrated an innovative SiN/AlN/GaN HEMT structure grown by MOCVD on large diameter high resistive Si (111) substrate. The unique combination of a 3 nm ultrathin barrier layer and a high 2DEG density resulted in a high output current density well above 1 A/mm at V_{GS} =+2 V and the highest extrinsic transconductance ever achieved for GaN-on-Si HEMTs. Furthermore, low leakage current through the 3 nm AlN barrier layer has been observed in both circular diodes and field effect transistors without the use of any gate dielectric. These results show that this highly scalable technology should offer unprecedented frequency operation considering the high aspect ratio achievable with sub-100 nm gate lengths and the great AlN/GaN-on-Si material quality already obtained. Therefore, breakthrough millimeter wave performances can be expected in a cost-effective way using this heterostructure.

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