



**HAL**  
open science

# CMOS inverter based on Schottky source-drain MOS technology with low-temperature dopant segregation

G. Larrieu, Emmanuel Dubois

► **To cite this version:**

G. Larrieu, Emmanuel Dubois. CMOS inverter based on Schottky source-drain MOS technology with low-temperature dopant segregation. IEEE Electron Device Letters, 2011, 32 (6), pp.728-730. 10.1109/LED.2011.2131111 . hal-00603004

**HAL Id: hal-00603004**

**<https://hal.science/hal-00603004v1>**

Submitted on 16 Sep 2024

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

# CMOS Inverter Based on Schottky Source–Drain MOS Technology With Low-Temperature Dopant Segregation

Guilhem Larrieu and Emmanuel Dubois

**Abstract**—This letter demonstrates the integration of complementary dopant-segregated Schottky barrier MOSFETs into CMOS inverters. The implementation of a valence-band-edge silicide, namely, PtSi, associated to arsenic (As) and boron (B) low-temperature segregation is validated for the first time at the circuit level. Current drives for n- and p-type devices are  $I_{\text{on}} = 596/378 \mu\text{A}/\mu\text{m}$  at  $V_{\text{ds}} = |1.1 \text{ V}|$  and  $|V_{\text{gs}}| = 2 \text{ V}$  to account for the 2.4-nm gate oxide thickness. Excellent inverter voltage transfer characteristics, large voltage gain, and appreciable noise margins have been obtained down to 0.5 V of supply voltage.

**Index Terms**—CMOS inverter, dopant segregation (DS), MOSFETs, Schottky barrier (SB), silicon-on-insulator (SOI).

## I. INTRODUCTION

**T**HIN-BODY MOSFET architectures associated to upcoming technology nodes are expected to deliver a higher current drive at shallower junction depth and reduced silicide thickness. As a consequence, severe constraints are imposed to conventional implanted source/drain (S/D) in terms of dopant activation that governs the sheet and contact resistivities and in terms of lateral dopant profiling that directly impacts short channel effects. One alternative is to use silicided metallic contacts that present a very low effective Schottky barrier height (SBH) to electrons and holes for n-type and p-type MOSFETs, respectively. Considering that the equivalent SBH should not exceed 0.1 eV in order to position Schottky-barrier (SB) MOSFETs advantageously with respect to conventional technology [1], low-temperature dopant segregation (DS) at the Schottky interface has emerged as a sound technological solution. The most advantageous methodology is to combine a band-edge silicide to its appropriate dopant type. In that way, p-type MOSFETs with boron-segregated PtSi contacts have been demonstrated [2]. Conversely, a conduction band-edge silicide such as YbSi<sub>2-x</sub>, coupled to As segregation, has been proposed for the n-MOSFET counterpart [3]. However,

this last approach faces two major obstacles: 1) the integration of a second silicide material; and 2) difficulties to process rare-earth silicides due to their high affinity with oxygen and reactivity with silicon-based dielectric materials [4]. Although a material like PtSi that presents a large SBH to electrons is theoretically not attractive for n-MOS devices, its association to As segregation [5] proved to produce near 0.1 eV barrier. Following this integration strategy, 0.35- $\mu\text{m}$ -long-gate n-MOSFETs have been demonstrated [6]. Dopant-segregated Schottky S/D integration in basic complementary CMOS inverter has also been demonstrated for midgap silicides [7]–[9]. Referring to these last reports, the so-called *implantation before silicidation* scheme was used in conjunction with high-temperature activation. Under these conditions, the advantage of low-temperature processing to relax constraints associated to the integration of temperature-sensitive materials is, however, lost. Although the utility of PtSi for both n- and p-type injection has also been outlined in the literature through material studies [4], [5], [10], no report exists on its practical implementation in basic digital circuitry. Recently, Khater et al. have provided a comprehensive performance review of Schottky source/drain transistors using a single silicide [11], without elaborating, however, on basic digital circuit operation. This letter proposes the first report on complementary SB-MOSFETs integrated in CMOS inverters based on As- and B-segregated PtSi contacts integrated in the so-called *implant-through-silicide* flavor using a single segregation activation step at 600 °C. Based on this process, functional elementary inverters down to 70 nm of gate length are demonstrated. In the first step, the CMOS process integration is briefly recalled, and individual current–voltage characteristics are detailed. Essential circuit parameters such as the output logic levels, static noise margins, and voltage gain of the  $V_{\text{out}}-V_{\text{in}}$  transfer characteristic are subsequently extracted and discussed.

## II. DESIGN AND EXPERIMENT

The starting material consists of a (100)-oriented p-type doped (4–10  $\Omega \cdot \text{cm}$ ) SOI substrate that was thinned from 50 down to 16 nm by chemical etching [12]. The main process steps are summarized in Fig. 1(a) and are detailed in [13]. The process sequence begins with the definition of a MESA isolation recess by etching the SOI active layer down to the buried oxide. The gate stack is composed of a 2.4-nm thermal oxide covered by a 50-nm-thick tungsten metal gate. Slim

This work was supported by the European Commission through the METAMOS project (016677) and NANOSIL project (216171).

G. Larrieu is with LAAS, CNRS, Université de Toulouse, 31077 Toulouse, France (e-mail: guilhem.larrieu@laas.fr).

E. Dubois is with the Institut d'Electronique et de Microélectronique et de Nanotechnologie, UMR CNRS 8520, 59652 Villeneuve d'Ascq, France (e-mail: emmanuel.dubois@isen.iemn.univ-lille1.fr).

- Mesa isolation
- Gate patterning and spacer formation
- PtSi S/D silicidation
- As I/I on n window
- $\text{BF}_2^+$  I/I on p window
- DS activation RTA 600°C
- Al pads

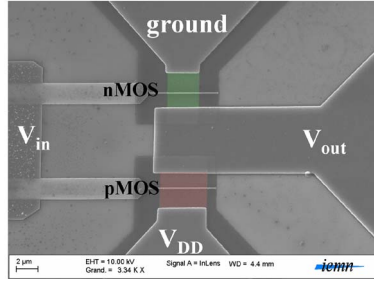


Fig. 1. (Left) Schematic process flow of SB-CMOS integration with dopant segregation at low temperature and (right) aerial SEM view of an SB-CMOS inverter with PtSi S/D contacts associated to As/B segregation for the n-MOS pull-down/p-MOS pull-up transistors.

15-nm-wide nitride spacers are subsequently integrated on each side of the gate by PECVD deposition and dry etching. A 15-nm platinum silicide layer is selectively formed on S/D regions of n-type and p-type transistors from a 7-nm Pt overlayer. At this stage, boron dopants are confined into the silicide by ion implantation ( $\text{BF}_2^+$  15 keV,  $5 \times 10^{14} \text{ cm}^{-2}$ ) to obtain p-type contacts, with the complementary n-type transistor being protected by a resist mask. The reciprocal approach is followed for the n-type transistor using arsenic implantation ( $\text{As}^+$  17 keV,  $5 \times 10^{14} \text{ cm}^{-2}$ ). A single annealing step limited to 600 °C is subsequently applied to segregate dopants at the interface between the silicide and the semiconductor [2], [5]. At this temperature, sub-0.1-eV SBH has been measured on dedicated test structures for both contact polarities. For instance, boron-segregated PtSi contacts on p-Si exhibits an SBH of 70 meV [2], [5], [10], while arsenic-segregated PtSi contacts on n-Si exhibit an SBH of 80 meV [5], [10]. Because annealing is limited to the temperature of silicidation, the deep diffusion of dopants is avoided, thus alleviating issues associated to the formation of ultrashallow junctions. Finally, 200-nm Al contact pads are structured over the source, drain, and gate terminal and sintered at 400 °C for 4 min under  $\text{N}_2\text{H}_2$  atmosphere. Fig. 1(b) presents a SEM aerial view of a DS SB-CMOS inverter. The shaded top and bottom regions correspond to the implantation windows of arsenic and boron implants, respectively. It is worth noting that a mesa recess separates the transistor common output node to prevent any dopant interdiffusion effect that could degrade the Schottky barrier height. To achieve symmetric pull-down and pull-up operation, channel widths of the n-MOS and p-MOS transistors are set to  $W_n = 3$  and  $W_p = 4.5 \mu\text{m}$ , respectively.

### III. RESULTS AND DISCUSSION

Fig. 2 shows the static  $I_{\text{ds}}-V_{\text{gs}}$  and  $I_{\text{ds}}-V_{\text{ds}}$  characteristics of typical 70 nm long gate transistor. From a qualitative standpoint, no sublinear inflexion is observed on the  $I_{\text{ds}}-V_{\text{ds}}$  curves indicating that the SB heights for both transistor types are sufficiently low to not limit carrier injection at the source junction [13]–[15]. The current drive for n- and p-type devices is  $I_{\text{on}} = 596/378 \mu\text{A}/\mu\text{m}$  at  $V_{\text{DD}} = 1.1$  V with  $|V_{\text{gs}}| = 2$  V to account for the 2.4-nm gate oxide thickness. The subthreshold slope value at low  $V_{\text{ds}}$  is close for both transistor polarities, namely, 106 and 88 mV/dec for n- and p-type transistors, respectively.

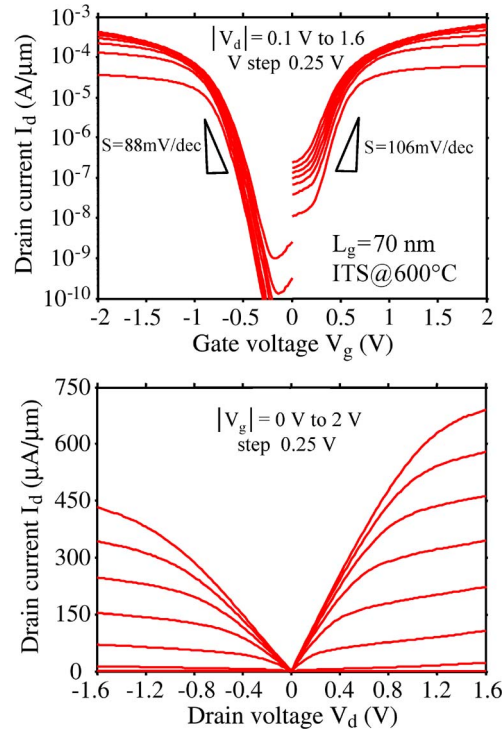


Fig. 2. Static  $I_{\text{ds}}-V_{\text{gs}}$  and  $I_{\text{ds}}-V_{\text{ds}}$  characteristics of 70 nm long gate complementary SB-MOSFETs with PtSi S/D and dopant segregation to modulate the SBH at the silicide/Si interface.

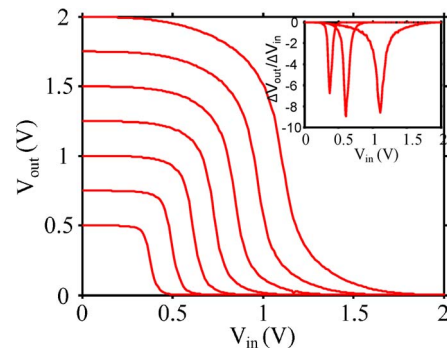


Fig. 3. VTC of an SB-CMOS inverter at different  $V_{\text{DD}}$  ranging from 0.5 to 2 V by step of 0.25 V. The gate length of complementary transistors is 70 nm, while their width ratio is selected to account for the difference current drive:  $W_{\text{n-MOS}} = 3 \mu\text{m}$  and  $W_{\text{p-MOS}} = 4.5 \mu\text{m}$ . The voltage gain ( $\Delta V_{\text{out}}/\Delta V_{\text{in}}$ ) is given in the inset for three different  $V_{\text{DD}}$  (0.5, 1, and 2 V).

Fig. 3 shows the voltage transfer characteristics (VTC) for an inverter featuring 70-nm-long transistors. Several  $V_{\text{DD}}$  values are considered ranging from 0.5 to 2 V by step of 0.25 V. For each supply voltage condition, well-behaved VTC is obtained with a low-to-high output dynamic that reach the rail-to-rail supply voltage range. This indicates that subthreshold leakage currents of both transistors are sufficiently low to not degrade high and low logic states. The inset of Fig. 3 shows the voltage gain variations along the VTC for several  $V_{\text{DD}}$ . A sharply peaked distribution reveals a narrow transition zone that amounts to 210 mV for  $V_{\text{DD}} = 1$  V. The peak position at  $\sim 0.6$  V is slightly shifted off  $V_{\text{DD}}/2$  due to an uncompensated asymmetry between n- and p-MOS saturation currents. This

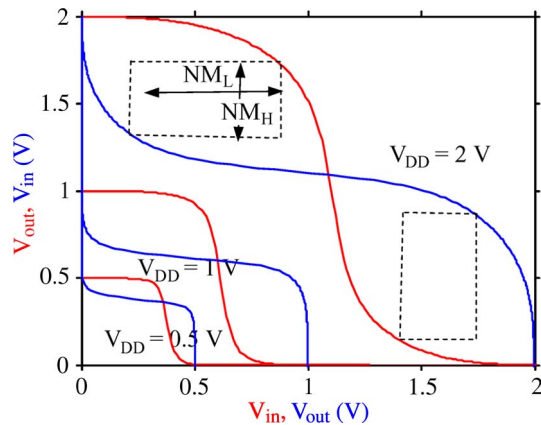


Fig. 4. Transfer static characteristics of 70 nm long gate channel SB-MOSFET inverter at three different  $V_{DD}$  (0.5, 1, and 2 V) by plotting  $V_{in}$  and  $V_{out}$  interchangeably to evaluate noise margins ( $NM_L$  and  $NM_H$ ) according to the MPC.

asymmetry partially originates from unequal DIBL factors for both transistor polarities of DIBL (177 and 126 mV/V for n- and p-MOSFETs, respectively). Although the device width ratio ( $W_p/W_n$ ) was tuned to obtain balanced saturation currents at  $|V_{gs}| = 2$  V to compensate for the thick gate oxide, the direct measurement of the VTC makes this correction unpractical. To refine the analysis, the static noise margins have been evaluated using the maximum product criterion (MPC) [16] that maximizes the area of the rectangles that can be embedded within the VTC loops of cross-coupled inverters. Excellent noise margins are deduced from the graphical illustration in Fig. 4, e.g.,  $NM_L = 0.47$  V and  $NM_H = 0.21$  V for 1 V of supply voltage.

#### IV. CONCLUSION

The integration of CMOS inverters based on complementary segregated PtSi Schottky S/D extensions and using a single low-temperature activation step at 600 °C has been demonstrated for the first time. Excellent dc VTC, large voltage gain, and appreciable noise margins have been obtained down to 0.5 V of supply voltage. One single silicide coupled to a low-temperature S/D module offers an effective, viable, and low-cost manufacturing approach for future technology nodes of complementary MOSFETs. This approach is also particularly well suited to the integration of temperature-sensitive materials and for monolithic device stacking in three dimensions that must comply with severe thermal budget reduction to guarantee silicide stability.

#### REFERENCES

- [1] D. Connelly, C. Faulkner, and D. E. Grupp, "Performance advantage of metal source/drain in ultra-thin-body silicon-on-insulator and dual-gate CMOS," *IEEE Trans. Electron Devices*, vol. 50, no. 5, pp. 1340–1345, May 2003.
- [2] G. Larrieu, E. Dubois, R. Valentin, N. Breil, F. Danneville, G. Dambrine, J. P. Raskin, and J. C. Pesant, "Low temperature implementation of dopant-segregated band-edge metallic S/D junctions in thin-body SOI p-MOSFETs," in *IEDM Tech. Dig.*, Dec. 2007, pp. 147–150.
- [3] G. Larrieu, D. A. Yarekha, E. Dubois, N. Breil, and O. Faynot, "Arsenic-segregated rare earth silicide junctions: Reduction of Schottky barrier and integration in metallic n-MOSFETs on SOI," *IEEE Electron Device Lett.*, vol. 30, no. 12, pp. 1266–1268, Dec. 2009.
- [4] G. Larrieu, D. A. Yarekha, E. Dubois, D. Deresmes, N. Breil, N. Reckinger, X. Tang, and A. Halimaoui, "Issues associated to rare earth silicide integration in ultra thin FD SOI Schottky barrier nMOSFETs," *ECS Trans.*, vol. 19, no. 4, pp. 201–207, Apr. 2009.
- [5] Z. Zhang, Z. Qiu, R. Liu, M. Ostling, and S.-L. Zhang, "Schottky-barrier height tuning by means of ion implantation into preformed silicide films followed by drive-in anneal," *IEEE Electron Device Lett.*, vol. 28, no. 7, pp. 565–568, Jul. 2007.
- [6] Z. Zhang, Z. Qiu, P.-E. Hellstrom, G. Malm, J. Olsson, J. Lu, M. Ostling, and S.-L. Zhang, "SB-MOSFETs in UTB-SOI featuring PtSi source/drain with dopant segregation," *IEEE Electron Device Lett.*, vol. 29, no. 1, pp. 125–127, Jan. 2008.
- [7] T. Kinoshita, R. Hasumi, M. Hamaguchi, K. Miyashita, T. Komoda, A. Kinoshita, J. Koga, K. Adachi, Y. Toyoshima, T. Nakayama, S. Yamada, and F. Matsuoka, "Ultra low voltage operations in bulk CMOS logic circuits with dopant segregated Schottky source/drain transistors," in *IEDM Tech. Dig.*, Dec. 2006, pp. 1–4.
- [8] A. Kinoshita, C. Tanaka, K. Uchida, and J. Koga, "High-performance 50-nm-gate-length Schottky-source/drain MOSFETs with dopant-segregation junctions," in *VLSI Symp. Tech. Dig.*, 2005, pp. 158–159.
- [9] L. K. Bera, Y. F. Lim, S. J. Tan, W. Y. Loh, B. Ramana Murthy, N. Singh, T. Yang Rong, H. S. Nguyen, R. Kumar, G. Q. Lo, N. Balasubramanian, and D. L. Kwong, "Dopant-segregated Ni-silicide Schottky-source/drain CMOS on strained-Si/SiGe multiple quantum-well channel on bulk-Si," in *Proc. 36th ESSDERC Conf.*, Sep. 2006, pp. 290–293.
- [10] N. Breil, A. Halimaoui, E. Dubois, E. Lampin, L. Godet, G. Papisoulitis, G. Larrieu, and T. Skotnicki, "Investigation on the platinum silicide Schottky barrier height modulation using a dopant segregation approach," in *Proc. Mater. Res. Soc. Symp.*, Mar. 2008, vol. 1070, pp. 85–90.
- [11] M. Khater, Z. Zhang, J. Cai, C. Lavoie, C. D'Emic, Q. Yang, B. Yang, M. Guillorn, D. Klaus, J. Ott, Y. Zhu, Y. Zhang, C. Choi, M. Frank, K.-L. Lee, V. Narayanan, D.-G. Park, Q. Ouyang, and W. Haensch, "High- $K$ /metal-gate fully depleted SOI CMOS with single-silicide Schottky source/drain with sub-30-nm gate length," *IEEE Electron Device Lett.*, vol. 31, no. 4, pp. 275–277, Apr. 2010.
- [12] X. Tang, N. Reckinger, G. Larrieu, E. Dubois, D. Flandre, J. P. Raskin, B. Nysten, A. M. Jonas, and V. Bayot, "Characterization of ultrathin SOI film and application to short channel MOSFETs," *Nanotechnology*, vol. 19, no. 16, pp. 165 703–165 710, Apr. 2008.
- [13] G. Larrieu and E. Dubois, "Integration of PtSi-based Schottky-barrier p-MOSFETs with a midgap tungsten gate," *IEEE Trans. Electron Devices*, vol. 52, no. 12, pp. 2720–2726, Dec. 2005.
- [14] E. Dubois and G. Larrieu, "Measurement of low Schottky barrier heights applied to S/D metal-oxide-semiconductor field effect transistors," *J. Appl. Phys.*, vol. 96, no. 1, pp. 729–737, Jul. 2004.
- [15] E. Dubois, G. Larrieu, N. Breil, R. Valentin, F. Danneville, D. Yarekha, G. Dambrine, A. Halimaoui, A. Pouydebasque, and T. Skotnicki, "Recent advances in metallic source/drain MOSFETs," in *Proc. IWJT*, May 2008, pp. 139–144.
- [16] J. R. Hauser, "Noise margin criteria for digital logic circuits," *IEEE Trans. Educ.*, vol. 36, no. 4, pp. 363–368, Nov. 1993.