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ENVIRONMENTAL CONDITIONS INFLUENCE ON EMBEDDED CAPACITORS - COMPARISON WITH DISCRETE CAPACITORS

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Abstract

The technology evolution of capacitors from a precedent paper in 1993 [1] in which we studied a ceramic capacitor reported on a FR4 substrate to today's is very important. In order to reduce the risk of early failures peculiar to ceramic capacitors, technologists are using new polymer-ceramic materials embedded in the FR4 or FLEX substrate during the manufacturing step. In this paper the robustness of such embedded capacitors regarding the environmental conditions (temperature and humidity) was studied and compared to discrete ceramic capacitors.

1. INTRODUCTION

Since 1993 we work on the recurring problem of reliability of ceramic capacitors in all shapes and sizes. In 1993 [1], we optimized the size of a capacitor soldered onto a PCB substrate. The results revealed that the most important parameters for an assembly are: temperature of the process, length of the capacitor and nature of the substrate. The increase of the stress is caused by the mismatch of the thermal expansion coefficient and the thermal conductivity between the ceramic dielectric, the terminations, the solder, the copper land and the substrate. During cooling, the difference of dissipation due to heat flow between these elements creates important contraction or compression constraints on the different materials. Any concentration of stress can induce cracks (fracture of the leads, shear and fracture of the solder joint, lifting of the copper lands) or cause failure of the assembly. These results are still valid. However, capacitors are now becoming smaller and difficult to reflow. Today manufacturers proposed passive components with a smaller size: for example the 0201 package (L = 0.02 in.; W = 0.01 in.). From a manufacturing perspective, the size of the 0201 package poses significant challenges to the printed circuit board (PCB) assembly process. The many challenges with 0201 assembly can be attributed to the solder paste volume, pad design, aperture design, board finish, type of solder paste, pick-and-place and reflow profile. In a precedent FP6 European program (AMELIE) we have tested ceramic capacitors 0805 47pF in different environments. It is well known that it is reasonable to expect passive component densities [2] of 20–30 passives/cm² and the risk of failures becomes important. In order to alleviate this problem new materials are used today for embedded capacitors. The interest of this kind of material is the possibility to place a capacitor close to the active component, the saving of space and also the reduction of the parasitic inductances. We have characterized the robustness of embedded capacitors based on commercial materials regarding the environment. Embedded capacitors are made with plastic material subjected to moisture attack. This paper deals with the behaviour of this kind of material versus temperature and humidity.

After presenting results performed on our laboratory, we discuss about the interest of the use of such materials and we conclude the paper with a comparison between ceramic capacitors and embedded capacitors.

2. EMBEDDED CAPACITORS BASED ON POLYMER-CERAMIC DIELECTRIC

Embedded capacitors are made of a dielectric material layer between two metal layers (usually copper foils), buried in a PCB. Inorganic dielectric materials are partly replaced by organic polymers. Polymer-ceramic composites are expected to be the major candidate as dielectric interlayer for embedded capacitors because such composite materials present both characteristics of the processibility of polymers and a high dielectric constant (k) of inorganic materials as titanates [3, 4, 5]. Our study on embedded passive components is already in progress with different partners in various programs.

During this first study, such a commercial dielectric composite was studied.

The organic polymer is filled with high dielectric constant particles (BaTiO_3 according to EDX analysis presented Figure 1) modifying the epoxy film.

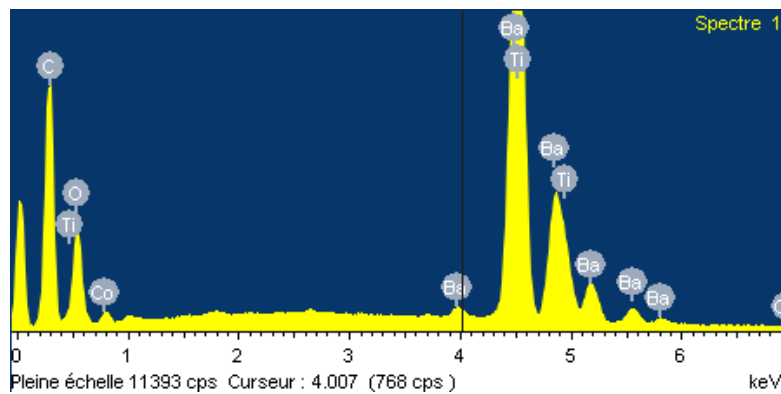


Figure 1: EDX analysis of a commercial dielectric layer based to BaTiO_3 .

2.1. ENVIRONMENTAL CONDITIONS INFLUENCE

In order to perform a first robustness study, the impact of temperature and humidity on embedded capacitors based on a polymer-ceramic material was successively studied.

2.2. 1. TEMPERATURE IMPACT ON CAPACITANCE

Capacitance measurements versus frequency were carried out using the impedance meter HP 4192A and the test fixture HP 16034E in the frequency range [100Hz – 10MHz].

Figure 2 shows the capacitance variation versus frequency in the temperature range [25-150°C]. The electrode area of the studied capacitor is $6.0 \times 6.0 \text{ mm}^2$ and the dielectric thickness is $16 \mu\text{m}$.

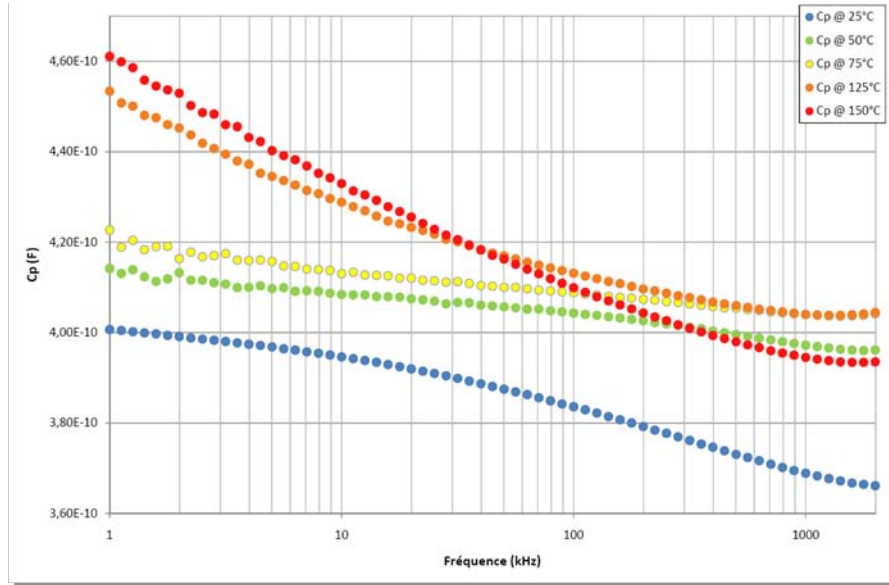


Figure 2: Capacitance variation Vs frequency in the temperature range ([25-150°C]).

Whatever the temperature, the capacitance decreases with frequency due to the decrease of the relative permittivity $\epsilon_r(\omega)$ with frequency. The capacitance $C(\omega)$ is linked to $\epsilon_r(\omega)$ by the following equation:

$$C(\omega) = \frac{\epsilon_r(\omega) \epsilon_0 S}{d} \quad (1)$$

Where ω is the excitation frequency, ϵ_0 the vacuum permittivity, S the electrode area and d the dielectric thickness.

Moreover the capacitance increases with temperature due to the increase of the relative permittivity $\epsilon_r(\omega)$ with temperature. A change of the behaviour of the capacitance is observed after 125°C because of the glass transition of the material (T_g close to 120 °C).

For robustness study, another commercial polymer-ceramic material is considered (also based on BaTiO₃). The electrode area of the studied capacitors is 1.0x1.0mm² and the dielectric thickness is 8µm.

Figure 3 shows the capacitance variation versus frequency after various exposure times to (a) 85°C and (b) 150°C for the first exposure hours.

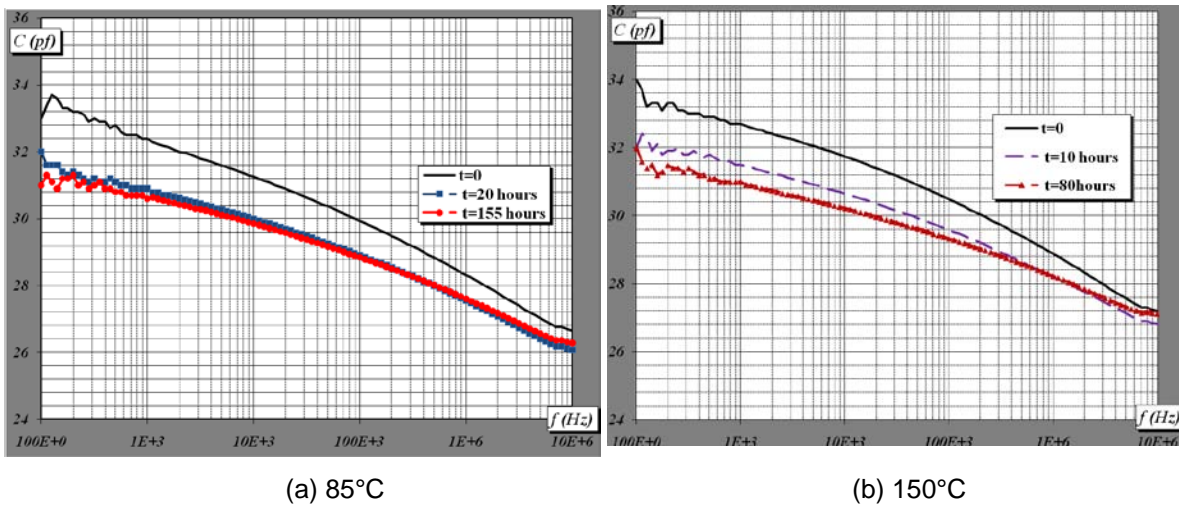


Figure 3: Capacitance variation Vs frequency after various exposure times to (a) 85°C and (b) 150°C

Whatever the temperature, the capacitance decreases with exposure time. At ambient temperature, the dielectric material contains a little part of water. After exposure to 85°C / 150°C, water is evaporated. Water permittivity is higher than material one whatever the frequency. So the material permittivity and then the capacitance decrease after exposure to 85°C / 150°C.

The behaviour is similar at 85°C and 150°C. However the capacitance decrease is accelerated at 150°C: the same variation is observed at 150°C after 80h and at 85°C after 155h.

Figure 4 presents the capacitance variation versus frequency after 1000h at 150°C after drying.

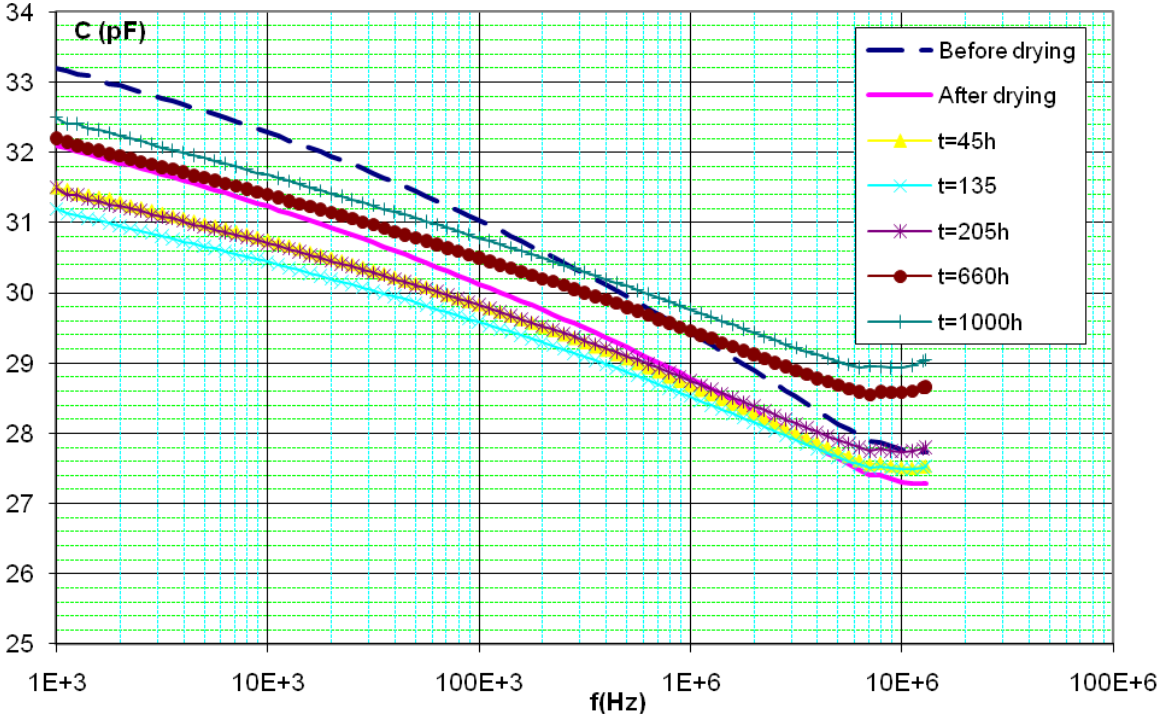


Figure 4: Capacitance variation (1*1 mm²) Vs frequency after various exposure times to 150°C

After drying, the capacitance significantly decreases due to water evaporation. A maximal capacitance variation of only 7% is observed at high frequency after 1000h.

At high frequency, a gradual slope change is observed with exposure time. This may correspond to a modification of the material during thermal ageing.

2.2.2. MOISTURE IMPACT ON CAPACITANCE

Capacitance measurements versus frequency were carried out after various exposure times to 85°C / 85% of humidity.

Figure 5 presents the capacitance variation versus frequency for the same embedded capacitor as previously (electrode area 1.0x1.0mm² and dielectric thickness close to 8µm).

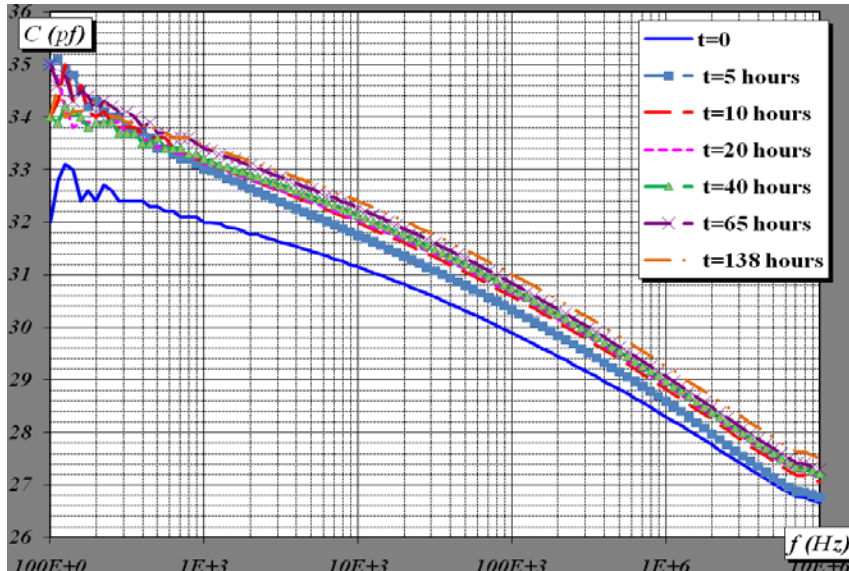


Figure 5: Capacitance Vs frequency after various exposure times to 85°C / 85% of humidity.

Whatever the dielectric material, capacitance increases with exposure time because of water absorption by the material (water permittivity higher than polymer-ceramic permittivity).

After 138 hours, no significant variation is observed.

3. DISCRETE CERAMIC CAPACITORS

During a precedent FP6 program (AMELIE), we have tested two lots of 25 X7R 0805 ceramic capacitors (2,03x1,27x1 mm +/- 0.2 mm) 47pF (showed Figure 6).

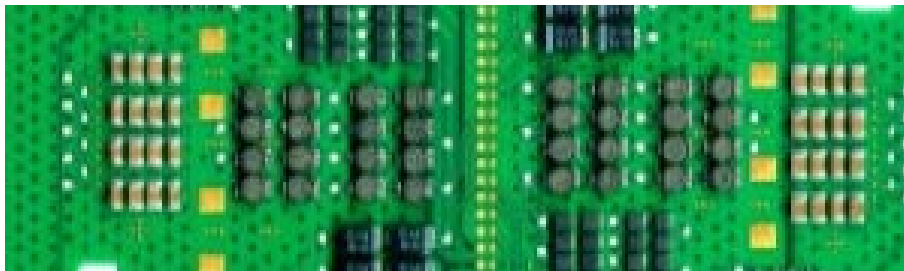


Figure 6: PCB test vehicle for ceramic capacitors in AMELIE FP6 program.

3.1 ENVIRONMENTAL CONDITIONS INFLUENCE

In this part a lot of papers have been performed on ceramic capacitors X7R type. We have synthesized different results in different European programs: AMELIE (FP6) and PROCURE (FP7) and some results coming from various papers.

3.1.1 TEMPERATURE IMPACT ON CAPACITANCE

After the reflow, the ceramic capacitors were stored at high temperature 150 °C and 85°C.

To measure the impact of the storage we used impedance spectroscopy based on piezoelectricity analysis existing on such capacitors [6] (example done Figure 7).

The piezoelectric test was performed just before the ageing test (storage) and at 200hours, 600hours and 1000hours. At 1000hours two components present a weakened piezoelectric signature.

The parameters are:

Number of cracked devices after 600h: 0

Number of cracked devices after 1000h: 2

Number of devices close of the failure (crack) after 1000h: 2

Number of devices with R_i failure: 0, $R_i > 1011 \text{ Ohm}$

Drift of the capacitance observed at the end of ageing.

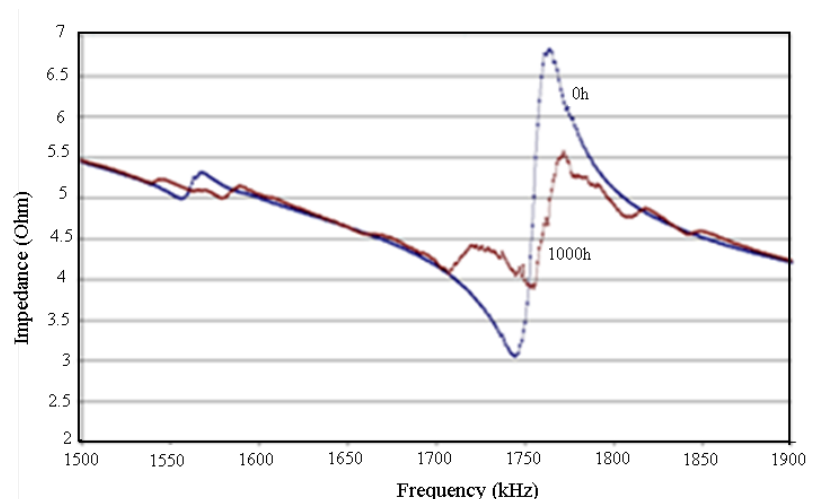


Figure 7: Example of piezoelectric response for a defective capacitor.

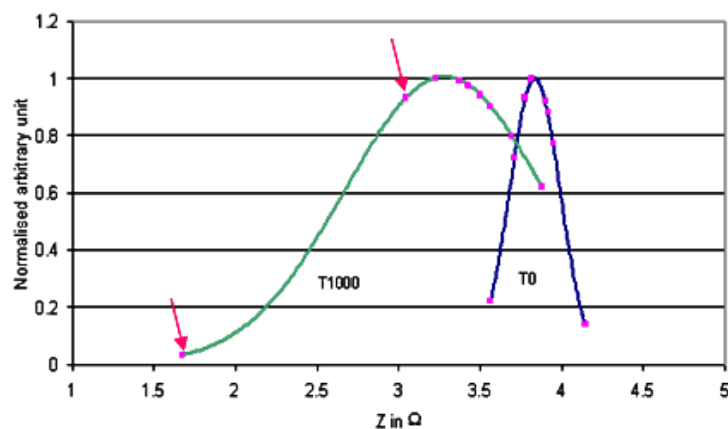


Figure 8: Statically dispersion of the impedance during ageing test.

After 1000h a strong dispersion of the impedance is observed. Two devices are defective (cracks). The position of weak devices is on the left zone of the Gaussian curve at 1000h (see arrows on Figure 8). At $t=0h$ the impedance value of both components was external values of the Gaussian.

These quality problems have been resolved by the manufacturer in the European program PROCURE - FP5 [6]. The decoupling capacitors (X7R) have become more robust by increasing the nickel barrier and by adding dopants.

3.1.2. MOISTURE IMPACT ON CAPACITANCE

Usually the humidity is not a recognized factor of failure for ceramic capacitors. DONAHOE Daniel N. and all [7] in their paper intituled “Moisture induced degradation of multilayer ceramic capacitors” explained that, when both precious metal electrode and base metal electrode (BME) capacitors were subjected to autoclave (121 °C/ 100% RH) testing after 500h, it was found that the precious metal capacitors aged according to a well known aging mechanism (average capacitance degraded less than 3% from their starting values), but the BME capacitors degraded to below the -30% specification limit.

4. DISCUSSION

As shown in Figure 9, the expected values of capacitance for the next years will be around 1000 $\mu\text{F}/\text{mm}^2$. These values come from the compilation of data from different manufacturers of ceramic capacitors. These values are smoothed, showing the tendency to be limited by the grain size of BaTiO_3 .

The decrease of the thickness of the dielectric is influenced by the use of nanoscale grains. We note the risk introduced by a thin layer on the stiffness of these layers.

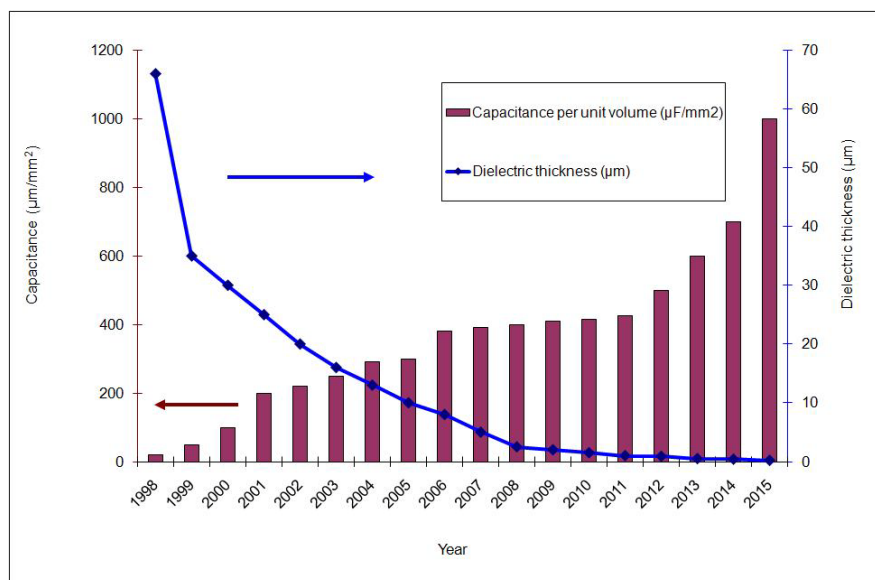


Figure 9: Evolution of the main parameters from different manufacturers of ceramic capacitors

The maximum time at temperature, number of reflow solder cycles or re-work cycles are not limited by ceramic capacitors but by the assembly laminate and plastic moulded components. The board can blister, delaminate and have plated through hole failures. Generally, defect induced on ceramic capacitors are due to manufacturing process and reflow problems. This kind of defects could generated failures during operational used of the components.

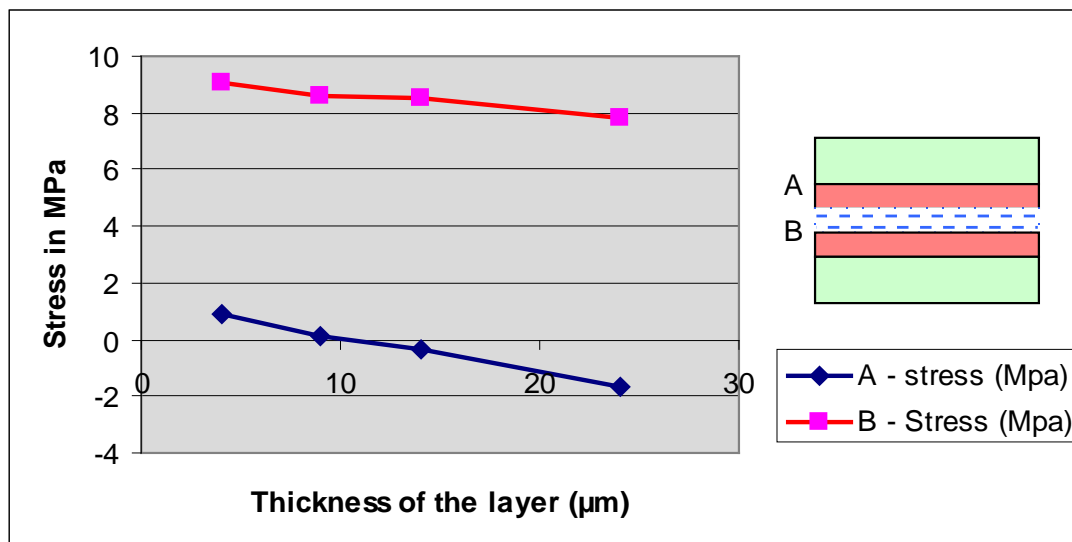


Figure 10: Strain value in the copper-dielectric and copper-PCB vs thickness of the dielectric for the capacitor calculated with CRITIDEL (www.eurelnet.org [8])

The strain value on the top and the bottom of the dielectric inside the PCB were calculated using an analytical program (CRITIDEL from EURELNET). The obtained values are less than the values encountered generally for a capacitor reflowed on a PCB [9]: close to 8 MPa to 10 MPa instead of 200 MPa to 300 MPa for the reflow process.

For electronic designers embedded capacitors are promising but the range value is not sufficient for the moment. They need a higher value of dielectric permittivity to reduce the size of the elementary capacitor and generate in one shot different kind of capacitance values. Today these values are closed to 0.5 to 2 nF/cm². The best will be 20 to 200 nF/cm², for a larger capacitance value range.

5. CONCLUSION

Whatever the studied organic polymer dielectric, the capacitance decreases after thermal exposure (max \approx 6%) because of water evaporation.

We can note a slope change after thermal exposure: there is a possible dielectric properties modification due to temperature (ϵ' increase after thermal ageing).

Whatever the studied organic polymer dielectric, the capacitance increases after humidity exposure (max \approx 6%) due to water absorption.

Embedded passives are more reliable by eliminating solder joints. Strains at the different interfaces are less than a solder joint good result for the reliability point of view.

With the added benefits of elimination of solder joints, inventory, assembly and rework vis-a-vis their surface mounted counterparts, embedded ceramic capacitors provide a very convincing and compelling option to meet the ever increasing need for miniaturization and improve performance in modern electronic designs.

6. ACKNOWLEDGEMENTS

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