HAL
open science

Design and characterization of a signal insulation coreless transformer integrated in a CMOS gate driver chip

Timothé Simonot, Nicolas Clément, Jean-Paul Rouger, Jean-Christophe Crébier, Jean-Daniel Arnould

To cite this version:

Timothé Simonot, Nicolas Clément, Jean-Paul Rouger, Jean-Christophe Crébier, Jean-Daniel Arnould. Design and characterization of a signal insulation coreless transformer integrated in a CMOS gate driver chip. Design and characterization of a signal insulation coreless transformer integrated in a CMOS gate driver chip, May 2011, San Diego, United States. pp.360-363. hal-00599260

HAL Id: hal-00599260

https://hal.science/hal-00599260v1

Submitted on 9 Jun 2011

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Proceedings of the 23rd International Symposium on Power Semiconductor Devices & IC's
May 23-26, 2011 San Diego, CA

Design and characterization of a signal insulation coreless transformer integrated in a CMOS gate driver chip

Simonot Timothé, Rouger Nicolas, Crebier Jean-Christophe
Grenoble Electrical Engineering Lab
UMR 5269 CNRS / UJF-Grenoble University 1/Grenoble-INP
St Martin d'Hères, France

Arnould Jean-Daniel
IMEP LAHC
UMR 5130 CNRS / UJF-Grenoble University 1/Grenoble INP/Université de Savoie
Grenoble, France

Abstract— **With the development of multi-level, multiphase or network converters requiring the implementation of numerous distinct power transistor gate drivers, the control signal insulation is becoming more and more important in power converters. This paper presents an isolation technique based on a coreless transformer integrated in a CMOS silicon die together with the gate driver and other required functions. The associated demodulation circuit will also be presented, as the control signal must be modulated at a high frequency through the coreless transformer. The chosen design methodology will be explained and experimental results will be shown in order to validate the functionality.**

I. INTRODUCTION

An insulation system is often required to carry and bring the control signal of power transistors at their reference potential. Indeed, the voltage difference between their reference potential and the external remote command can be brought to high floating voltages. Insulation systems in most power electronics circuits are level shifters [1], optocouplers [2] or discrete magnetic or piezoelectric transformers [3, 4]. The transformers' benefits over other insulated control signal transfer systems are that they are not as sensitive to EMI and voltage ratings as level shifters, they are faster and less consumer than optocouplers [5]. Moreover, they offer a fairly high dielectric insulation range (up to several kV), depending on the thickness and dielectric strength of the insulation material between the two windings. Initially, magnetic insulation was carried out with discrete pulse transformers [3], then with coreless PCB transformers [6] and now with silicon integrated coreless transformers [7]. The main benefits of this integration is that the insulation system can be directly implemented within a CMOS gate driver with no extra technological steps in the fabrication process, while consuming a reasonable silicon area, presenting a large bandwidth and being directly interconnected to the gate driver. The use of a CMOS process also allows the integration of complex logic functions, which can be required for the demodulation of the gate control signal, and other protection and driving circuits. Finally transformers can be used to transfer data in both directions to send back useful information to the control unit for example.

This paper presents the design methodology of an integrated coreless transformer and its associated demodulation circuit for power electronics transistor driving purposes. First, a geometrical layout of the transformer is presented, based on geometrical design considerations deduced from analytic formulas and technological constraints coming from the foundry characteristics. A simple model of the transformer is then established using analytic formulas and finite-elements simulations with the Flux^R 2D software. This model is used to design the associated demodulation circuit in a standard CMOS technology. Finally, the design is validated with a practical implementation, based on Austria MicroSystem's C35B4M3 technology, and experimental results and transformer characteristic curves are shown.

II. OPERATING PRINCIPLE AND DESIGN CONSIDERATIONS

A. Operating principle

Most of HF silicon integrated transformers have no magnetic core to guide the flux lines, which means that the coupling is severely reduced at low frequencies. The resonant frequency of this type of transformers is generally high, as the magnetizing inductance of the integrated transformer is small (around 100nH). Therefore, the remote control signal has to be modulated at a high frequency (hundreds of MHz) in order to minimize the losses inside the transformer. A modulation technique has to be chosen, depending on which signal is sent into the transformer. The PWM signal is generated in the external remote circuit. Corresponding to the ON state, a modulated high frequency sine wave carrier is applied to the transformer. When the OFF state is desired, a zero DC voltage difference is applied to the primary winding. This modulation technique is appropriate and simple. The carrier frequency can be set in a wide frequency range (between 90 and 500MHz) and the transmitted envelope is a square wave corresponding to the transistor triggering signal (PWM).

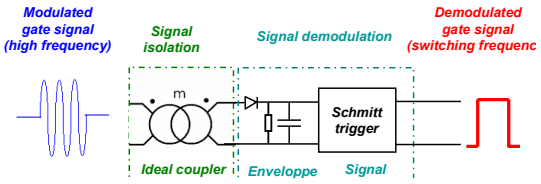


Figure 1: Control signal modulation principle

Figure 1 shows the principle of the insulation system. The sine wave signal is transferred through the transformer, then an envelope detection circuit at the secondary side winding of the transformer recovers the low frequency square wave modulating envelope. A Schmitt trigger is introduced to avoid false triggering of the transistor due to parasitic signals. The signal is finally demodulated and sent into the gate driver amplification circuit.

B. Design considerations

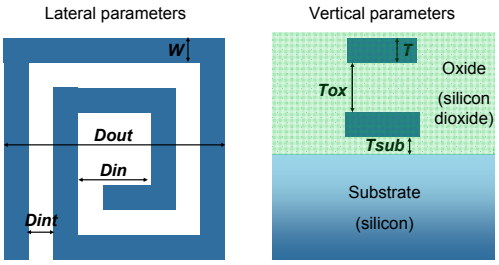
The design's main objective is to obtain the best coupling while using a silicon surface as small as possible. The technological data, conductor and isolator thicknesses and layout constraints, are then used to determine the geometry of the transformer. The chosen transformer topology is a stacked transformer, using the multiple metal layers available in the

selected CMOS technology to maximize the voltage insulation capability. As shown in figure 2, one can distinguish geometrical parameters such as outer and inner diameters, conductor width and spacing between the turns, and vertical parameters such as the conductor and oxide thicknesses between the windings, and oxide thickness between the windings and the substrate. The geometrical parameters are critical to determine the leakage and magnetizing inductances as well as the winding series resistance, and the coupling coefficient. The thickness of the conductors will modify the resistance of the windings, and the oxide thickness between the conductors and the substrate will change the capacitive coupling between the windings and to the substrate. The oxide thickness between the two windings is critical when insulation is needed, as the breakdown voltage is directly proportional to the thickness of the oxide according to equation (1)

$$Tox*DS=BV \quad (1)$$

(with Tox : oxide thickness, DS dielectric strength and BV breakdown voltage)

The oxide used in IC fabrication is often low temperature silicon dioxide (SiO2), which usually has a dielectric strength below 10MV/cm. As a result, the breakdown voltage of the oxide is around 1kV for a 1µm-thick oxide. One must notice that the designer can not modify the vertical parameters since they are technology dependant in standard CMOS processes (set by the foundry). The design is then focused on the geometrical parameters to obtain the desired inductance, resistance and coupling coefficient, while minimizing the parasitic elements which reduce the coupling.



Dout : outer diameter
Din : inner diameter
Dint : distance between the turns
W : conductor width

T : conductor thickness
Tox : oxide thickess between the two windings
Tsub : oxide thickness between the conductor and the substrate

Figure 2: Geometrical parameters of the integrated transformer

In the next section, it will be shown how the lateral parameters alter the typical values of the integrated transformer, and which compromises must be optimized.

III. DESIGN GUIDELINES

The typical values of an integrated transformer are the windings inductance and resistance, the mutual inductance between the windings, and the coupling coefficient. The parasitic elements which deteriorate the coupling are at first the leakage inductance and winding resistance and then the capacitances between the windings, the capacitances between the windings and the substrate, and the substrate capacitance and resistance. Analytic formulas found in refs [8] and [9] describe these elements as a function of the geometric parameters of the transformer. These formulas will be employed in this paper to see the evolution of the elements of the transformer depending on the geometry of the transformer in a simple manner

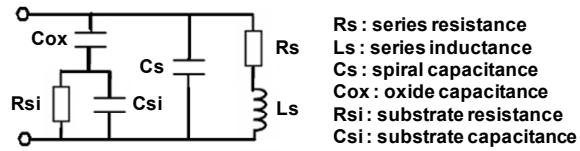


Figure 3: Physical model of an inductor on silicon

Figure 3 shows the equivalent model of an inductor on silicon, with the series inductance, resistance, and capacitance, and the parasitic elements. From this model, one can express the equivalent impedance of the parasitic elements Cox, Csi, Rsi of the spiral. The impedance of the spiral can be expressed with Rs, Cs and Ls. For high frequencies in the range of hundreds of MHz, it can be assumed that the term $(Ls*\omega)^2$ will be predominant over the term R^2 and $1/(C*\omega)^2$ in the equation of the spiral impedance, so the impedance of the spiral is only a function of the inductance of the spiral. Equation (2) expresses the equivalent parasitic impedance Zparas, and equation 3 the impedance of the inductance Xs.

$$Zparas := \left[\frac{1}{\left[\frac{1}{\frac{1}{Rsi^2} + (Csi \cdot \omega)^2} \right] + \frac{1}{(Cox \cdot \omega)^2}} \right]^{0.5} \quad (2)$$

$$Xs := \left[(L \cdot \omega)^2 \right]^{0.5} \quad (3)$$

From equations (2) and (3), the ratio Xs/Zparas can be expressed. It is a good parameter for the designer to see at which point the impedance of the spiral is predominant over the impedance of the parasitic elements for a given frequency. Another significant parameter that can be used to design the transformer is the coupling coefficient of the transformer. This parameter is the ratio of the spirals mutual inductance divided by their series inductance, as shown in equation (2), where Lp and Ls are respectively the primary winding and secondary winding inductances, and M the mutual inductance. In the case of a stacked transformer, the windings have identical geometries, so that Lp=Ls=L. One can then obtain the mutual inductance M=k*L. The coupling coefficient can be expressed as a function of the geometrical parameters with equation (4), where ds is the center to center distance of the turns, and davg the average diameter [8].

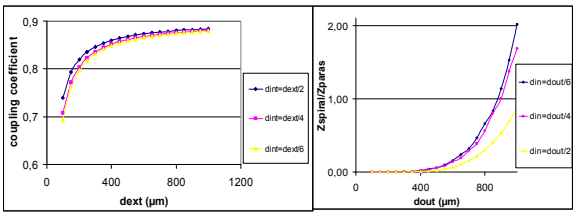
$$k := 0.9 - \frac{ds}{davg} \quad (4)$$

The equations stated above show both the effect of parasitic impedance over spiral inductance and the coupling between the spirals as a function of the geometry of the transformer. On this basis, the design of the transformer's geometry can be made by searching the largest ratio of inductance impedance over parasitic impedance, while optimizing the coupling coefficient k.

A. Influence of the outer and inner diameters

First, the outer diameter is varied while setting the inner diameter as a the portion of the outer diameter (e.g.

din=dout/4). As a result, the number of turns N will then increase when dout increases. The other geometrical parameters which are the conductor width and the distance between the turns are set respectively to 10µm and 2µm. The frequency is set to 100MHz.



a) b)

Figure 4: a) Ratio Zspiral/Zparas as a function of the outer diameter b) Coupling coefficient as a function of the outer diameter

As one can see on figure 4-a, the ratio Xs/Zparas is close to zero for outer diameters below 500µm, showing that parasitic impedance is predominant, and starts to increase exponentially for outer diameters above 500µm. The ratio is lower when the inner diameter is half the outer diameter, but is roughly the same when it is a quarter or a sixth of the outer diameter. Figure 4-b shows a weak coupling coefficient for small outer diameters, and coupling above 0.85 for outer diameters larger than 500µm. Figure 4-b also introduces that there is no significant influence of the inner diameter on the coupling coefficient. Then, to achieve a satisfactory coupling and low parasitic influence on the spiral inductance, the outer diameter should be larger than 500µm for the chosen frequency and spiral geometry. A compromise has then to be made between the silicon space used by the transformer and the desired ratio.

B. *Influence of the spiral width*

To see the influence of conductor width and spacing between the turns, these parameters will be wept while setting the outer and inner diameters respectively to 1mm and 250µm, and keeping a same frequency. As it can be deducted from equations, (2), (3) and (4), both the ratio Xs/Zparas and the coupling coefficient decrease when the width of the conductor increase, showing that the conductor width should be kept as small as possible. The width can then be chosen as a function of the skin depth, which should be the smallest value of the conductor width for the chosen design frequency. From the same equations, the influence of the spacing between the turns on both the impedance ratio and coupling coefficient is comparable to the influence of the conductor width, it should also be chosen as small as possible. The smallest value of this spacing is determined by the design rules of the technology used for the fabrication of the transformer.

IV. EXPERIMENTAL VERIFICATION

After having set these design guidelines, the transformer can be designed in the chosen technology and for the chosen frequency. We chose the technology AMS C35B4M3 from Austria MicroSystems, with 4 metal layers available. The chosen topology of the transformer is to use the upper metal layer for the primary winding and the lower metal layer for the secondary winding. The largest oxide thickness between the two windings is therefore achieved. The chosen geometry for the spirals is 600µm for the outer diameter and 100µm for the inner diameter, resulting in a 1/6 ratio to maximize the spiral inductance. The chosen design frequency is 100MHz, so the conductor width is set to 16µm which is two times the aluminum skin depth at this frequency. The spacing between the turns is set to 2µm, which is the minimum spacing between two thick metal tracks in the C35B4M3 technology.

A. *Analytic and Finite Elements simulation comparison*

The resulting values of the transformer elements are calculated from the formulas previously used from [8] and [9], and compared to the values computed with the finite elements simulation software Flux 2D. The resulting values are shown in table I.

TABLE I. COMPARISON OF TRANSFORMER MODEL VALUES

Transformer element	**Calculated values**	
	Analytic	***Finite Elements***
Series spiral inductance	90 nH	85 nH
Mutual inductance	76.9 nH	76,5 nH
Coupling coefficient	0.85	0.9
Primary winding series resistance (DC)	23.2 Ω	25.8 Ω
Secondary winding series resistance (DC)	97.7 Ω	107.5 Ω

The values in Table I show small differences between the analytic values and the values obtained with simulations. It can then be assumed that values computed from analytic equations are accurate enough over a wide range of parameter values. The series resistances of the windings are frequency dependant due to skin and proximity effects. In this case only signal is transmitted, so the current needed is only the magnetizing current of the transformer. As the period of the modulated signal is small, it can be assumed that the current needed will be small, so these effects can be neglected even at the high operating frequency of the transformer. This has been confirmed with numerical simulations. These values will be compared to the fabricated transformer measurements.

B. *Analytic model and experimental measurements comparison*

The characterization of the transformer at frequencies from 40MHz to 40GHz has been performed using an ANRITSU ME7808C vector network analyzer. Figure 5 shows the comparison between the model and the measurements for both the primary and secondary winding impedance real and imaginary parts. The model curve fits the measurements up to the first resonant frequency around 500MHz, but differ after this frequency due to other capacitive and inductive couplings. Figure 6 shows that the transmission parameter S21 model fits the measurements up to 5GHz, except for the two resonant frequencies around 500MHz. From this curve one can deduct that the optimal operating point of the transformer is around 490MHz, since the transmission coefficient S21 is maximum at this frequency and starts to decrease after 500MHz. From these measurements it can be said that the transformer model is incomplete, as model curves don't fit the measurements above 500MHz. However, for our frequency range of operation, it is sufficient to have a good idea of the transformer's impedance and coupling behavior, as the design has been made for a 100MHz operating frequency.

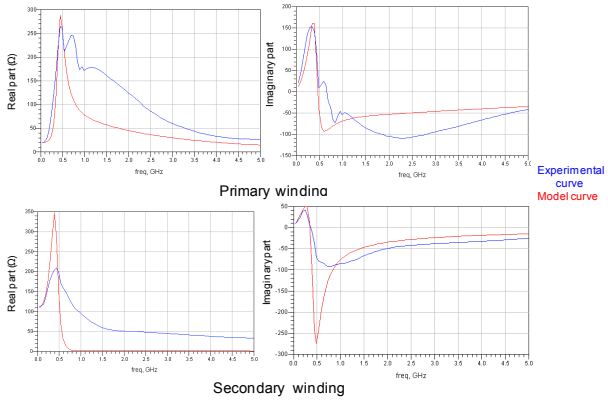


Figure 5: Transformer real and imaginary parts model and measurements comparison

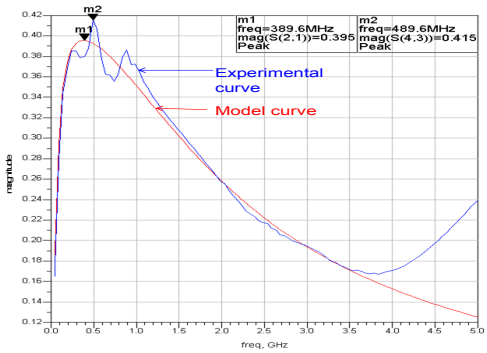


Figure 6: Transformer S21 parameter model and measurement comparison

C. *Demodulation circuit and breakdown voltage experimental measurements*

Experimentations of the transformer and its demodulation circuit showed good results with a modulation of the carrier at a 90MHz frequency and for a 12V peak to peak amplitude signal at the primary winding (figure 7). A 10ns response delay was observed, which is fast compared to standard optocouplers. The isolation voltage capability of this transformer was also tested and the dielectric breakdown of the oxide was observed for a voltage of 1200V between the two windings, making this transformer suitable for many applications.

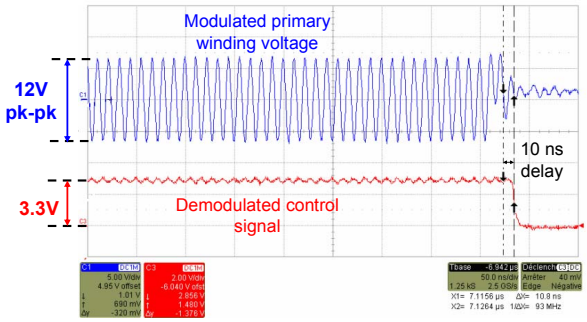


Figure 7: Waveforms of the modulated primary winding voltage and demodulated control signal

V. Summary and Conclusions

The design of an integrated transformer and its associated demodulation circuit has been presented in this paper. The purpose of this transformer is the insulation of the remote control signal of a power MOSFET, which can be integrated within a power MOSFET gate driver processed in a standard CMOS technology at no extra cost. To help the designer to achieve an efficient design, design guidelines taking into account the parasitic impedance and the coupling coefficient of the transformer as a function of its size and geometry have been given. Therefore, a good coupling can be obtained while minimizing the transformer's size and parasitic elements. Experimental results of an integrated transformer fabricated using Austria Microsystems AMS C35B4M3 standard CMOS technology have been shown. The analytical model used for the design showed good accuracy in the desired frequency range of operation compared to the measurements. The fabricated transformer was capable to withstand a voltage of up to 1200V, while exhibiting a small propagation delay of 10 ns.

Acknowledgment

The authors would like to gratefully acknowledge the contributions of N. Corrao from IMEP-LAHC (Grenoble - France) for the characterization of the coreless transformer. We would also like to thank O. Deleage for his contribution to the modeling of the coreless transformer.

References

[1] Yongcheol Choi, Changki Jeon, Minsuk Kim, "Design and process considerations for 1200V HVIC technology," ISPSD 2009. 21st International Symposium on , pp.311-314, 14-18 June 2009

[2] Mazumder, S.K., Sarkar, T., "Optically-activated gate control of power semiconductor device switching dynamics," ISPSD 2009. 21st International Symposium on pp.152-155, 14-18 June 2009

[3] Herzer, R.; Pawel, S.; Lehmann, J., "IGBT driver chipset for high power applications" *Power Semiconductor Devices and ICs, 2002. Proceedings of the 14th International Symposium on*, pp. 161- 164

[4] Vasic, D.; Costa, F.; Sarraute, E.; , "Piezoelectric transformer for integrated MOSFET and IGBT gate driver," *Power Electronics, IEEE Transactions on* , vol.21, no.1, pp. 56- 65, 2006

[5] Munzer, M. et al, "Insulated signal transfer in a half bridge driver IC based on coreless transformer technology," PEDS 2003. The Fifth International Conference on, pp. 93- 96 Vol.1, 17-20 Nov. 2003

[6] Pawel, S., Thalheim, J, "1700V Fully Coreless Gate Driver with Rugged Signal Interface and Switching-Independent Power Supply," ISPSD '08. 20th International Symposium on , pp.319-322, 2008

[7] Baoxing Chen; , "Isolated half-bridge gate driver with integrated high-side supply," *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE* , pp.3615-3618 2008

[8] Hasaneen, E.-S.A.M.; , "Modeling of on-chip inductor and transformer for RF integrated circuits," *Power Systems Conference, 2006. MEPCON 2006. Eleventh International Middle East* , pp.65-69, 2006

[9] del Mar Hershenson, M.; Mohan, S.S.; Boyd, S.P.; Lee, T.H.; , "Optimization of inductor circuits via geometric programming," *Design Automation Conference, 1999. Proceedings. 36th* , pp.994-998, 1999