Integrated Low Power and High Bandwidth Optical Isolator for Monolithic Power MOSFETs Driver

Nicolas Clément, Jean-Paul Rouger, Jean-Christophe Crébier, Olivier Lesaint

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Nicolas Rouger, Jean-Christophe Crébier and Olivier Lesaint
Grenoble Electrical Engineering Lab (G2Elab)
Centre National de la Recherche Scientifique, Grenoble-INP, UJF-Grenoble university 1, Saint Martin d'Hères, France
Email: nicolas.rouger@g2elab.grenoble-inp.fr

***Abstract*—An integrated solution for the galvanic isolation between power transistors and their control unit is presented in this paper. This solution is based on a monolithic integration of a photodetector within a power MOSFET without any modification of its fabrication process. This photoreceiver can be associated with a monolithic driver to drive high side switches. Exhaustive characteristics for several integrated photodetectors are presented and discussed: quantum efficiency, step response, small signal analysis and sensitivity to the High Voltage MOSFET's Drain. The results of this analysis are photoreceivers with a Full Width at Half Maximum above 300MHz and a responsivity above 0.15A/W at a wavelength of 500nm. This leads to an integrated low power and high bandwidth optical isolation.**

***Index Terms*—Monolithic integration, Power ICs, integrated optical sensor, power transistor gate driving circuits.**

I. Introduction

SiC or GaN based power transistors are very attractive and start to exhibit outstanding performances [1]. However, the Silicon platform still has numerous advantages, most significantly its availability, reliability and performances. The heterogeneous and monolithic integration within Silicon power transistors is still a great way to improve not only the transistor itself, but the whole power switch function in power converters [2], [3]. Although several integrated solutions for driver supplies or gate drivers are available, only a few solutions have been presented to date for the integration of the required isolation between the power switch and its external control driver [4], [5]. However, these solutions remain difficult to monolithically integrate within power transistors. Considering integration related issues, the optical isolation is the perfect candidate for power transistors [6], annihilating Electro Magnetic Interferences between the remote control circuit and the power transistor. The most advanced and attractive solution so far for an integrated optical isolation has been recently presented in [7], [8]. This solution, however, requires more than one optical Watt for the power transistor's turn ON and is based on a heterogeneous assembly of a GaAs optical detector and a power transistor. Following our preliminary results [6], we propose hereinafter a different approach than in [7], [8]. The monolithically integrated photo receiver acts as an optocoupler and delivers a small current to a monolithically integrated or flip chipped gate driver [9]. The gate driver will then use an efficient and integrated supply [10] to deliver the energy for the switching of the power transistor. In this paper, we will demonstrate the benefits and possible drawbacks of an integrated photodetector.

II. Integration Approach

In order to optimize the efficient operation of power transistors, their associated drivers must be located as close as possible to them. Indeed, any parasitic inductance between the power transistor and the driver circuit can drastically reduce the switching performances dynamics and can even introduce undesired firing. The monolithic integration of all the required driving functions looks therefore attractive. Our goal is here to provide a generic power switch function that can be used either as a high side or low side switch, while integrating the required isolation circuit with the highest isolation capability. Our integration approach in this context is to monolithically integrate a light-sensitive detector within the power VDMOS without any modification of its fabrication process. As previously demonstrated, other required functions can also be monolithically integrated within VDMOS (loss free gate driver supply [3]). In the view of improving the driver's intelligence (advanced sensors and protection circuits), a flip chipped CMOS driver die [9] can be preferably used. The resulting approach is presented in figure 1.

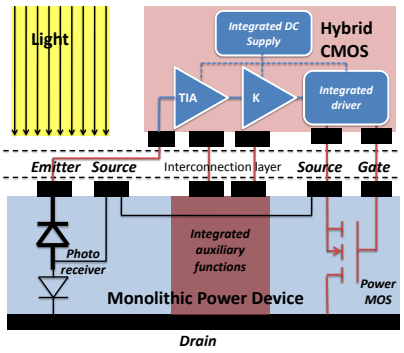

Fig. 1. Integration approach: a monolithically integrated photodiode, connected to a flip-chipped readout circuit (TransImpendance Amplifier + K voltage gain), a gate driver and an efficient self driver supply.

The power die monolithically integrates the power transistor cells, the photodetector and other required functions for the driver self supply technique [11]. The CMOS die integrates the required circuits for the photodiode readout circuit, the

self supply operation and the gate current amplification. Since the switching of power MOSFET usually requires at least hundreds of mW, transferring this power by light will definitely not be efficient (limited by the light emitter efficiency, transmission channel attenuation and detector responsivity). The integrated photoreceiver acts here as a sensor while converting optical power into a generated low current which is then filtered, amplified and detected by the CMOS circuits. The required energy for the power transistor's switching transitions is then taken from a storage capacitor. This integrated Power System On Chip would be very attractive since it will be autonomous, externally driven by a low power optical signal. However, this solution will be possible only with a highly sensitive and fast photodetector, which must not be affected by the common High Voltage drain. The next sections will focus on these requirements.

III. Design and Numerical Simulation of Integrated Photodetectors

A. Photodetector structure

The integrated photo receiver takes benefit of the parasitic NPN bipolar structure built in power VDMOS figure 2. Additional P+ highly doped base regions can be required, depending on the P- well concentration. The Collector backside electrode is merged with the High Voltage VDMOS Drain electrode. While connecting the Base region to the VDMOS lowest potential (Source), the vertical Collector-Base N++/Nν/P- junction will always be reverse biased. As a consequence, the N+/P- Emitter-Base junction can be used as an integrated diode, as long as the Emitter-Base junction is not forward biased. Since this Emitter-Base junction will act as the photo sensitive junction and should not be affected by the Drain/Collector potential, the Emitter-Base junction must always be reverse biased and the vertical bipolar transistor must not be activated neither during Drain voltage transients nor steady state or dynamic photo generation within the vertical device.

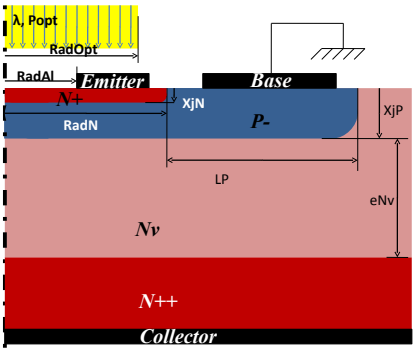

Fig. 2. Cross section of the integrated photodiode and its parameters. The center vertical axis represents the axis of revolution corresponding to the cylindrical structure of the photodiode.

Considering the proposed structure, the Base current will be the sum of the Emitter-Base leakage current and the Collector-Base leakage current. In this structure, the Emitter current will be used as the optically generated electrical current. One can notice that this structure with diffused P and N regions is definitely not optimized for a photodetector. Usually, fast and efficient optical detectors are made of an intrinsic/lightly doped region and two thin highly doped contact regions. Such classical designs maximize the drift phenomenon of the free carrier generated by light absorption within a wide space charge region. Diffusion currents are kept to a minimum due to the quantum efficiency and electrical bandwidth reductions by recombination and diffusion. In our design, diffusion currents generated by optical absorption are not negligible relatively to drift currents. Long current paths (recombination) must be avoided between the Emitter contact and the free carriers generation regions in order to increase the responsitivity of the device. However, shadow effects and strong optical absorption of the Emitter contacts must also be prevented. The control of carrier lifetimes is also challenging in this context and for fast integrated photodetectors.

B. DC modeling

Since doping profiles of the integrated Emitter-Base junction are not uniform and close to Gaussian profiles, an analytic modeling is therefore impossible especially in 3D. Numerical simulations were conducted in the Silvaco software Suite with the following assumptions:

- The epi $N\nu$ drift layer is designed for a 600V voltage breakdown capability. Accordingly, the epi region doping is $2 \cdot 10^{14} cm^{-3}$ with $eN\nu = 50\mu m$,
- The Base thickness X_{jP} is $5\mu m$ with a surface concentration of $5 \cdot 10^{16} cm^{-3}$,
- The Emitter surface concentration is $1 \cdot 10^{20} cm^{-3}$,
- The optical beam power P_{opt} is uniformly distributed to the photodetector sensitive area (collimated beam). Therefore, the Irradiance I_{opt} is constant within the optical beam with the relationship $P_{opt} = I_{opt} \cdot \pi Rad_{Opt}^2$,
- The complex refractive index of Silicon is wavelength dependant,
- For faster simulations, only $5\mu m$ of the backside N++ contact region are simulated,
- Since intrinsic performances are first to be demonstrated, the electrical contacts are assumed ohmic, and aluminium contacts' thickness infinitely thin,
- Shockley-Read-Hall and Auger recombination processes are activated during simulations, as well as band-gap narrowing, concentration and field dependent mobilities,
- Impact ionization is also activated for high Collector voltages.

Figure 3 presents the total Quantum Efficiency (QE) of several different devices, where the N+ Emitter thickness X_{jN} was varied in the range of $0.7\mu m$, $1\mu m$ and $1.2\mu m$. The QE is calculated accordingly to $QE(\lambda) = \frac{I_(\lambda)}{S \cdot \frac{q \cdot I_{opt} \cdot \lambda}{h \cdot c}}$ for each current. The denominator in the QE equation is commonly called the source photocurrent, as it represents the maximum possible current that can be generated by the detector, i.e. a 100% QE optical detector. Knowing that the light absorption coefficient

α is reduced for higher wavelengths, free carriers will be generated deeper in the Silicon device for higher wavelengths. For wavelength below $400nm$, α is higher than $10^5\ cm^{-1}$, corresponding to an absorption depth below $100nm$. As a result, most of the free carriers generated close to the sensitive surface are recombining through diffusion. Moreover, Silicon is highly dispersive at short wavelengths, leading to increased reflections below $400nm$. The overall QE is therefore limited when short wavelengths are used. The highest QE for the Emitter current is 40% at $\lambda = 500nm$ whereas the highest QE for the Base current is 60% at $\lambda \approx 700nm$. Considering the Air/Silicon optical interface, more than 33% of the incident optical power is lost due to reflections.

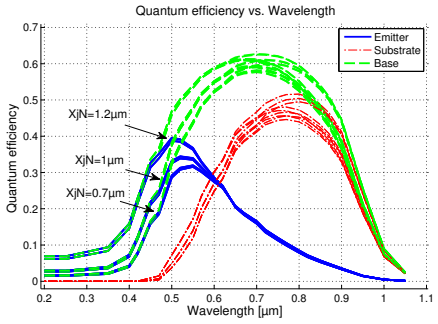

Fig. 3. Quantum Efficiency computed with a 3D Finite Element Analysis. Device parameters: $Rad_{Opt} = Rad_N = 4.5\mu m$, $P_{Opt} = 10; 20; 100\mu W$, $Rad_{Alu} = 0; 2.5\mu m$ and $X_{jN} = 0.7; 1; 1.2\mu m$.

Since both surface concentration of the N+ Emitter region and P- Base region are fixed, and both doping profiles are Gaussian, increasing the N+ Emitter region's depth X_{jN} will reduce the doping charge density around the P-/N+ junction. As a result, the space charge region at zero Emitter-Base bias will be wider with larger values of X_{jN}. Therefore, the QE of deeper Emitter regions will be increased due to reduced recombination levels. This is clearly shown by figure 3. However, N+ implantation dose limitation and width reduction of the P- pinched region reduces the maximum possible X_{jN}. The relationship between the QE and the responsivity of the photodetector is $R_\lambda(\lambda) = QE(\lambda) \cdot q\frac{\lambda}{h \cdot c}$. For the best detector with $X_{jN} = 1.2\mu m$ the responsivity is around $0.16A/W$ at $500nm$. No significant effects have been noted with small modifications of the Aluminium contact nor the optical power, considering our assumptions. It was also verified that the generated current does not increase significantly the base potential to guarantee the Emitter-Base reverse bias - Figure 4.

C. Small signal and large signal modeling

Both the transient response and the small signal analysis must be investigated. Figure 5 presents the emitter current transient response for different optical detectors where the optical beam and emitter radii have been modified as well as the wavelength, while keeping a same optical power step. All the simulated designs exhibit a step response below $3ns$, even

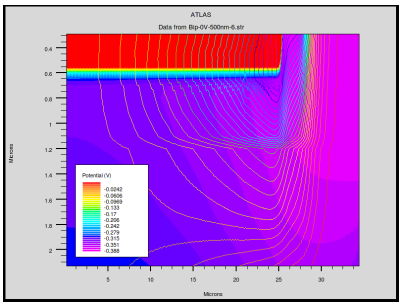

Fig. 4. Potential distribution with a $100\mu W$ - $\lambda = 500nm$ - $Rad_{Opt} = 25\mu m$ optical beam. Locally, the potential is increased by less than 0.05V. Current flow lines are also plotted.

for larger optical devices. One can also notice that when the optical beam radius is much higher than the emitter radius, the QE of the device is clearly decreased due to increased recombination. Since smaller devices also have smaller capacitances and smaller current paths, the best transient response is obtained with $Rad_{Opt} = 4.5\mu m$ and $Rad_N = 4.5\mu m$. This analysis is confirmed by the small signal analysis - figure 6. The dynamic behavior of the transient response is confirmed by the small signal analysis. The fastest detector has a 3dB bandwidth above $1GHz$ whereas the slowest is still above $300MHz$. Small devices are definitely attractive when illuminated by a $500nm$ or $550nm$ wavelength optical beam.

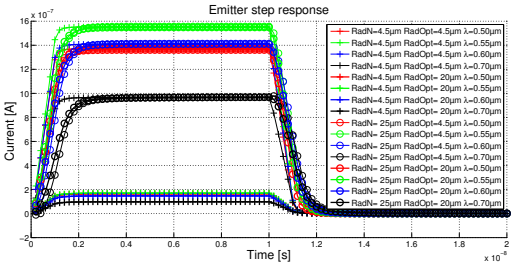

Fig. 5. Emitter current transient response to a $10\mu W$ optical power step. Device parameters: $Rad_{Opt} = 4.5; 20\mu m$, $Rad_N = 4.5; 25\mu m$, $\lambda = 500; 550; 600; 700nm$ and $X_{jN} = 1\mu m$.

D. Effects of the high voltage drain

When the Drain/Collector voltage is increased, several phenomena are affecting the isolated Emitter-Base photodetector. First, the Collector-Base space charge region is extending within the Base region, therefore reducing the Emitter QE. Numerical simulations show that the Emitter QE is reduced by 12% at $\lambda = 600nm$ and 3% at $\lambda = 500nm$ when the Collector is biased at 400V. Second, a high leakage current is created when a positive dV/dt is applied to the Drain/Collector. This Collector-Base capacitive current locally increase the potential of the base region therefore locally activating the vertical bipolar transistor. This is also more important when a high optical power is injected at the center of the photodetector. Applying a $400V/50ns$ Collector transient dV/dt within $50ns$

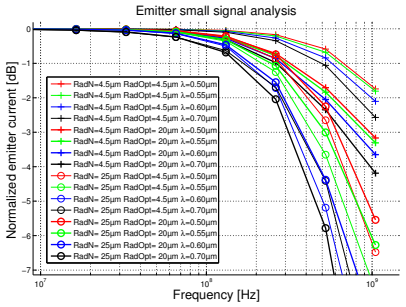

Fig. 6. Emitter current small signal analysis. Bias optical power is $10\mu W$ and small signal optical power amplitude is $1\mu W$. Device parameters: $Rad_{Opt} = 4.5; 20\mu m$, $Rad_N = 4.5; 25\mu m$, $\lambda = 500; 550; 600; 700nm$ and $X_{jN} = 1\mu m$. The emitter current was normalized relatively to the DC current for each design.

and under a $100\mu W$ optical beam did not locally forward bias the Emitter-Base junction. This dynamic self shielding was observed for every design with reduced Emitter and Base radii.

IV. Device characterization

An electro-optical setup has been realized - figure 7. Since low power coherent optical sources at $500nm$ are difficult to obtain, our first experimental characterizations use a $2mW$ - $640nm$ HeNe laser. The laser optical beam is spatially filtered and focused to the packaged photodetector. The laser was directly modulated. The radius of our devices was $Rad_N = 50\mu m$ and the best transient response observed was $0.2\mu s$. At such long wavelength, the substrate voltage also has a significant effect. However, this first experimental result demonstrates that an integrated photodetector is capable of a sufficient bandwidth, higher than 1MHz. The highest measured responsivity was 0.08A/W at 640nm. The differences between the numerical modeling and the experimental results are explained by larger devices (more than 4 times larger than a $25\mu m$ radius emitter region) and required parameters fitting.

V. Discussion and future works

A detailed numerical analysis has been presented. Shorter wavelengths, smaller detectors and thicker emitter regions must be used in order to optimize both the DC and AC performances of the devices. Although the numerical analysis investigated key parameters, temperature effects must be taken into account. A deeper characterization of both DC and AC performances of the integrated photodetectors is also required. We are currently improving the electro-optical setup in order to characterize the QE of integrated detectors for a wide range of wavelengths. DC and AC performances for large detectors and long wavelength have been demonstrated as a first proof of concept.

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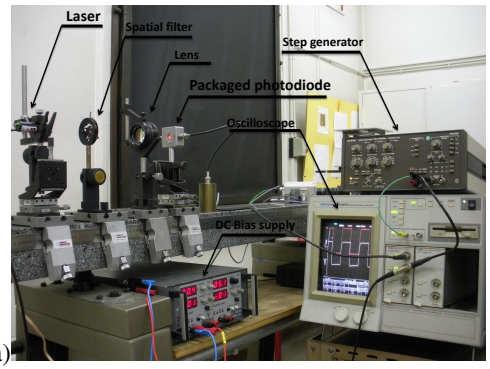

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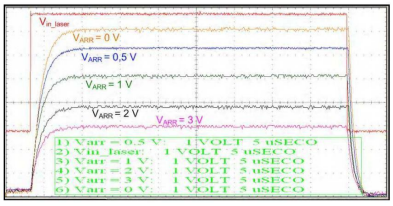

b)

Fig. 7. a) Electro optical setup. b) Characterized substrate effect and photodiode step response.

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