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The vertical voltage termination technique – characterizations of single die multiple 600V power devices

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Abstract— Deep trench terminations are commonly known as a technique to achieve ideal breakdown voltages for high voltage devices. This paper presents the use of deep trench terminations as an original concept to integrate multiple vertical power devices on a common die. The concept is based on the creation of vertical deep trench terminations on the periphery of the devices, thus allowing to separate the drift regions and to completely insulate the multiple power devices sharing the same backside contact electrode. Power diodes in the range of 600V are fabricated and experimentally tested to validate the concept. The prototypes demonstrated excellent forward and reverse biased static characteristics.

I. INTRODUCTION

Deep trench terminations have been widely investigated for high voltage device edge termination and are commonly known as a solution providing ideal voltage handling capability whereas consuming small junction termination area [1, 2]. Recently, a new technology for power integrated circuits using a combination of top and back trenches was presented. The demonstration was made for vertical power devices in the range of 5V [3]. Lately, [4] presented the evolution of this approach for high voltage power devices with breakdown levels in the range of 600V and higher. Several vertical PIN diodes sharing the same backside cathode were integrated in the same power die. Each power diode was individually separated, from its "neighbor" with a peripheral vertical voltage termination. This concept consisted of creating a deep trench vertical termination on the periphery of the devices, allowing to reduce surface electric field peaks but also to separate the different active regions. Thus, effective insulation between neighbor devices is guaranteed although they share a common backside contact electrode. Multidiode devices in the range of 600V are fabricated, packaged and passivated with silicone dielectric gel. The experimental validation of the concept showed near ideal breakdown voltage with small leakage current ratings but also a highly resistive behavior of the forward biased diodes.

This paper presents deeper investigation of this original concept for wafer-level integration of single die multiple vertical power diodes.

The paper focuses on the special care taken to improve the characterization of the manufactured power dies while adding new data and characteristics.

More specifically, the paper presents the new results obtained for the static characteristics of the fabricated devices and an evaluation of the reverse blocking characteristics as function of the temperature. In order to improve the static characterization of single and multiple diodes power die, special packages have been developed in order to use Kelvin probe measurement technique. The resulting characteristics matched completely with the theoretical ones, allowing to validate the approach. Power devices with deep trench edge terminations are known to exhibit larger leakage current than planar devices [5]. Therefore, the reverse biased characterization is carried out in a thermal chamber to investigate more specifically the evolution of the leakage current and the breakdown voltage levels with respect to the temperature.

II. DEVICE STRUCTURE AND FABRICATION

This section shortly recalls the main concept and the realization of the single die multiple 600V vertical power diodes.

A. Single die multiple power vertical diodes

The concept of the vertical voltage termination relies on the creation of a deep trench termination on the periphery of the devices. The same trench termination serves not only to ensure the voltage handling capability of the device but also to separate the active regions of the different devices sharing the same backside electrode terminal. The trench termination is then filled with a dielectric material and thus effective insulation between the different devices is guaranteed. Fig. 1

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shows a schematic view of the principle using vertical power diodes as example.

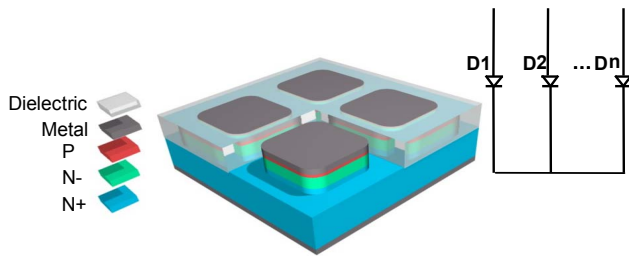


Figure 1. Schematic view of multiple power diodes integrated in a common die using the vertical voltage termination technique

As fig. 1 demonstrates with this technique multiple vertical power devices can be “islanded” on a common power die. This approach could be of great interest for the building of multiphase 3D power module assemblies [6]. Significant reductions in interconnect number as well as self aligned device chip are among the advantage of such approach. It appears as a key element of the package of power devices at wafer levels where several components are interconnected throughout the technological process, leading to reproducible and highly reliable the assembly.

B. Main manufacturing steps

In order to demonstrate the feasibility and the effectiveness of the proposed technique, vertical power diodes with vertical voltage terminations were fabricated. In our case 500 μ m N+ type (100) substrate plus 55 μ m lightly doped (20 Ω .cm) epitaxial layer was used for the realization of the prototypes. These parameters were chosen so that the breakdown voltage of the optimum plane junction should be 800V. All process steps are performed full wafer. After the deposition of 3 μ m thick layer of aluminum on both sides of the silicon substrate the different patterns are distinguished by a lithography step followed by wet etching of the metal on the surface and the trenches realization. The trenches were realized with Deep Reactive Ion Etching. After the DRIE process step the depth and the width of the trenches are 100 μ m and 150 μ m respectively. We used the aluminum metal layer as masking material. No post processes for surface or wall treatment were performed after the silicon etching step. Fig. 2 and 3 show the realized prototypes.

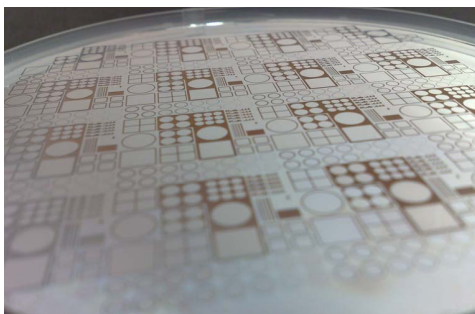


Figure 2. Photograph of the manufactured wafer : various patterns can be seen containing multiple “islanded” diodes

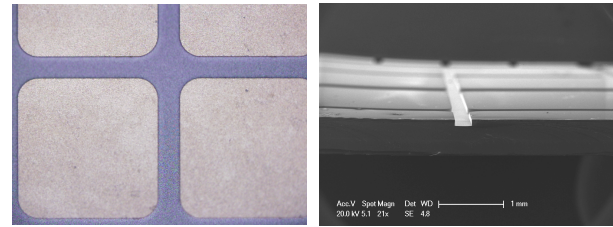


Figure 3. Top surface and cross sectional view showing multiple power diodes integrated on a common silicon die and separated by vertical voltage terminations

After the wafer sawing the chips containing several devices are individually packaged and passivated with silicone oil or gel.

III. RESULTS AND DISCUSSION

A. Forward characterizations

The forward biased characterization requires the use of Kelvin probes technique in order to optimize the quality of the measurements. A specific packaging architecture must be designed in order to optimize the power interconnections and to add two sensor terminals. A schematic of the designed packaging is given in fig. 4 below. The important issue here is related to the wire bond interconnects. Since our equipment is only able to solder wires with 33 μ m diameter, it is important to solder several wires but also to spread them at the surface of the chip in order to improve the homogenous distribution of the current over the cross section of the power devices.

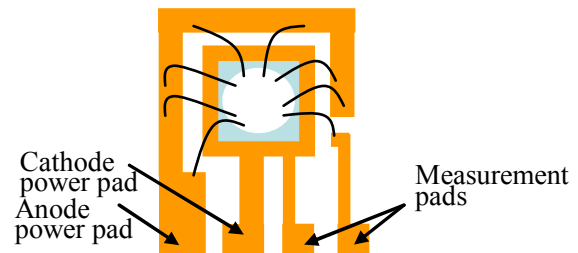


Figure 4. Schematic of the package for effective forward characterization.

Two packages have been developed. One is specifically used to maximize the current distribution and the quality of the measures of a single diode component. With this aim, wire bonds are connected to a metal track which is almost completely surrounding the power device. In such manner, the distribution of the power current is assumed to be ideal even if the wires are not fully adapted to the current ratings used in this experiment. A picture of the package is given in fig. 5 where it can be seen that the power device is soldered on a PCB track and surrounded by another track and two Kelvin probes on one side of the die.

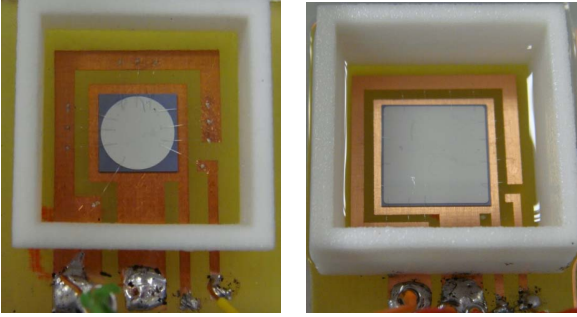


Figure 5. Pictures of the packages dedicated for forward bias characterization of single power diodes with vertical voltage terminations.

A second package has been designed for the characterization of a single die, four 600V vertical power diodes, each of them being connected on the anode side with several wire bonds spread at the surface of the metal layer plus a Kelvin probe on each of them. Fig. 6 presents a picture of the package in this case.

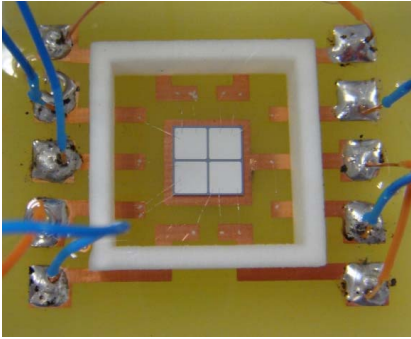


Figure 6. Picture of the package dedicated for forward bias characterization of single die 4 diodes component including multiple Kelvin probes.

The forward characterization of the single diode component is given in fig. 7 below. It is a $1.4 \times 1.4 \text{ cm}^2$ large diode (prototype fig. 5) with blocking capability in the range of 600 to 800V.

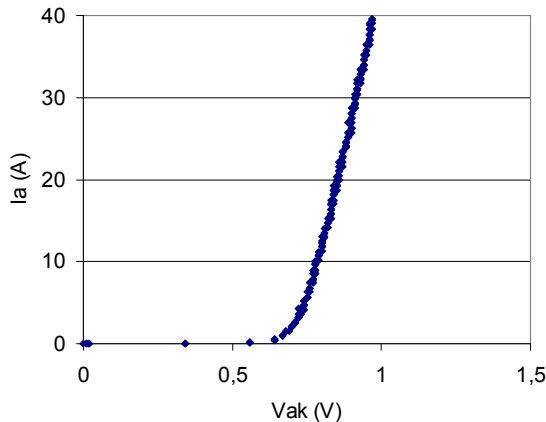


Figure 7. Forward biased characteristic of a single diode with vertical voltage terminations.

Testing the device under forward biased polarization with a power curve tracer HP 371A, 40A forward current was

measured under 1V forward voltage drop. This result is fully in accordance with our expectations, allowing to demonstrate the quality of the manufactured devices and the measurement technique that has been used.

Nonetheless, it must be mentioned that above a certain current level the devices passivated with silicon oil demonstrated a non expected behavior. Deeper investigations are required to identify the reason of such operation. Besides, this outstanding forward characteristic hides probably poor dynamic behavior. This will have to be investigated in the future.

B. Reverse biased characterization

Considering the reverse characterization of the power devices terminated with vertical edges manufactured in DRIE, the observations of three main data were carried out:

- -the ability of single die multiple diodes to withstand voltage while terminated and separated by the vertical edge termination technique
- -the ability of single or multiple diodes dies to withstand nominal voltage breakdown levels under minimized leakage current level
- -the ability to minimize leakage current level at nominal reverse voltage levels and under high temperatures (up to 100°C)

1) Single die multiple diode reverse characteristics

Fig. 8 shows the reverse characteristics in the case of testing the monolithic integration of prototype fig. 6. The four curves correspond to the four power diodes integrated in the same die. All four devices fulfill the initial design specifications considering the breakdown voltage rating of 600V.

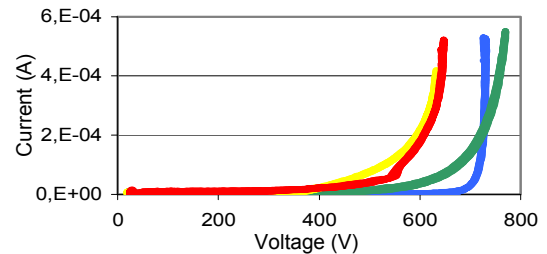


Figure 8. Static characteristics of reverse biased four power diodes sharing the same power die

The results show clearly that all four diodes have different voltage handling capabilities. It can be noticed in fig. 8 that one of the diodes has a leakage current of $10 \mu\text{A}$ at 600V while two others have leakage currents in the range of $200 \mu\text{A}$.

2) Reverse biased characterization at room temperature

Fig.9 represents one of the most significant achievements of blocking capability of a device with vertical voltage

terminations. The device demonstrated a breakdown voltage of 720V with a leakage current of 1.7 μ A at 600V.

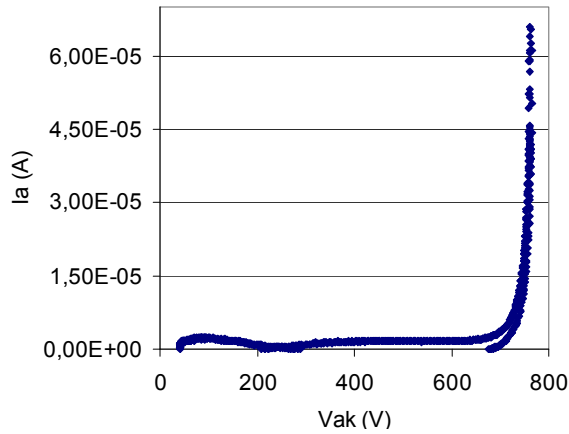


Figure 9. Reverse biased characteristic of one of the best single die multiple diodes

3) Reverse blocking characteristics as function of the temperature

Fig.10 shows the leakage current measurements at high temperature. The current level is in complete accordance with our expectations with leakage current dependence of temperature similar to that for planar devices. These results consolidate the choice of the technology and the measurement approach that we have presented in this paper.

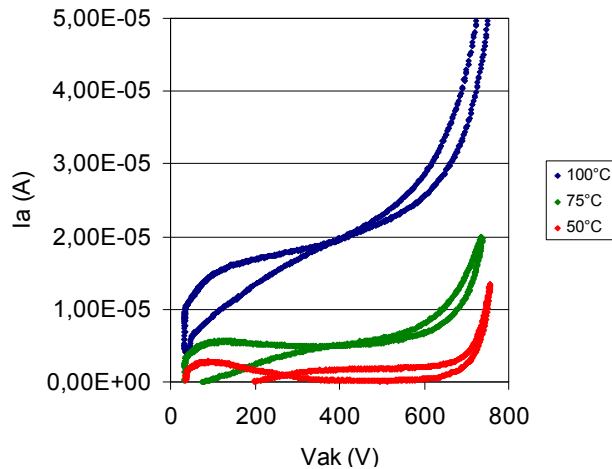


Figure 10. Reverse biased characteristics as function of temperature

IV. CONCLUSION

This paper presented the practical results of the continuation of the static characterization of single die multiple vertical diodes terminated and islanded with vertical edge terminations. Precise static forward and reverse biased characterizations have proven the ability of the termination technique to offer outstanding voltage breakdown with minimum leakage current at nominal voltage levels of 600V. Islanded multiple diodes were identified functional and exhibiting satisfactory performance levels. The robustness of the implementation still needs further investigations as well as the dynamic responses of the power devices. Nevertheless, this edge termination technique provides the possibility of wafer level packaging with collective assemblies and interconnections. Besides, with such surface treatment and edge terminations power devices could benefit from 3D power chip on chip packaging configuration, advantageous for effective high frequency double side cooling implementations.

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