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G. Beylier, D. Benoit, P. Mora, S. Bruyère, G. Ghibaudo. Contact etch stop a-SixNy:H layer: A key factor for single polysilicon flash memory data retention. *Journal of Vacuum Science and Technology*, 2009, 27 (1), pp.486-489. 10.1116/1.3071846 . hal-00596103

HAL Id: hal-00596103

<https://hal.science/hal-00596103>

Submitted on 2 May 2023

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Contact etch stop $a\text{-Si}_x\text{N}_y\text{:H}$ layer: A key factor for single polysilicon flash memory data retention

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(Received 30 May 2008; accepted 15 December 2008; published 9 February 2009)

The silicon nitride ($a\text{-Si}_x\text{N}_y\text{:H}$) contact etch stop layer strongly affects data retention performances in single polysilicon nonvolatile memories by acting on the initial charge loss phenomenon. Its improvement has required an analysis of influent plasma enhanced chemical vapor deposition process parameters through a design of experiment approach. The $a\text{-Si}_x\text{N}_y\text{:H}$ physico-electrical analysis points out that silicon rich compositions especially of its interfacial layer must be avoided to reduce $a\text{-Si}_x\text{N}_y\text{:H}$ charge amount and as a result to improve the data retention. Indeed, the $a\text{-Si}_x\text{N}_y\text{:H}$ being near the floating gate, its charges modulation could act as a parasitic memory screening charges stored in the floating gate by capacitive effects. © 2009 American Vacuum Society. [DOI: 10.1116/1.3071846]

I. INTRODUCTION

Data retention (DR) is one of the main reliability concerns affecting nonvolatile memory (NVM).¹ It must be guaranteed over ten years at quite high temperature (85 °C). However, when considering low cost (no added process step) single polysilicon (SP) flash cells, this requirement become even more critical. Indeed, the floating gate (FG) being no longer encapsulated by the control gate, its sensitivity to various process steps increases, increasing charge loss mechanisms. Recently, two charge loss phases have been distinguished for such a cell during accelerated 250 °C DR bake. During the first seconds of the experiment, a fast initial threshold voltage (V_{th}) shift appears and is followed by the standard long term charge loss from the FG.^{2,3} A Mielke cycle analysis has demonstrated that this abnormal initial shift is not induced by the traditional ionic contamination.³ In this context, after having observed a data loss reduction by taking away the amorphous silicon nitride ($a\text{-Si}_x\text{N}_y\text{:H}$) contact etch stop layer (CESL) from the FG,³ we have suspected this layer. The CESL, integrating in the premetal dielectric (PMD) stack, is deposited by plasma enhanced chemical vapor deposition⁴ (PECVD) and previous electrical characterizations have highlighted a high defect amount in this dielectric.⁵ Thus, the most probable hypothesis is that charges contained in the $a\text{-Si}_x\text{N}_y\text{:H}$ induced capacitive effects on the FG one.^{3,5} In this context, the aim of this study is to understand how physico-electrical $a\text{-Si}_x\text{N}_y\text{:H}$ properties impact the SP NVM DR by a design of experiment (DOE) on PECVD process conditions.

II. DOE CONSTRUCTION AND RESULTS

The analysis is performed on a 0.13 μm complementary metal oxide semiconductor technology SP NVM with a 85 Å gate oxide.³ The cell under consideration is defined by two areas: one corresponds to the control gate, with a high coupling coefficient to modulate the FG potential, and another used to program, erase, or select the bit [Fig. 1(a)]. Programming sequence is a two step operation, using a bipolar and an NMOS transistor, respectively, used to generate hot electron and to inject them into the FG. The cell is erasing by Fowler-Nordheim conduction. The 500 Å $a\text{-Si}_x\text{N}_y\text{:H}$ CESL is deposited by PECVD process and separated from the FG by LPCVD dielectrics used for silicide protection. Due to process deposition condition, the $a\text{-Si}_x\text{N}_y\text{:H}$ layer composition is not uniform and consists of an “interfacial” layer at the bottom, whose composition differs from the “bulk” [Fig. 1(b)]. Taking this into account, film deposition conditions were varied in accordance with a DOE plan, composed of four factors of three levels each and defined by a D optimal matrix (23 recipes with three centers points). Thus, the CESL “bulk” composition is defined by a first set of parameters: the silane (SiH_4) flow, the ammoniac (NH_3) one, and the radio frequency (rf) power. They were selected from a preliminary study, performed on a metal insulation semiconductor structure, where an increase of defect with silicon rich (Si-rich) film has been observed.⁶ The last parameter is the rf power ramp up speed, since it modifies the bottom “interface.” Indeed, as the SiH_4 is more easily dissociated than the NH_3 ,⁷ the low power at the beginning of the power ramp up gives a more Si-rich interfacial layer, suspected to act as a charge sink.

The DOE responses focus on physico-electrical properties involving numerous analysis tools, as described in the Table I. Some of them were determined as well as for the bulk than

*No corrections received from author prior to publication.

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TABLE I. DOE responses with method and variation range (b and i indices were for bulk and interface, respectively).

DOE responses		Methods	Minimum	Maximum
Si-H _b (cm ⁻³)		Fourier transform infrared spectroscopy	3.34×10^{20}	1.05×10^{22}
N-H _b (cm ⁻³)		Fourier transform infrared spectroscopy	4.9×10^{20}	2.2×10^{22}
Stress _b (MPa)		Wafer curvature	-1013	783
Density (g cm ⁻³)		Weighing	2.28	2.66
Refractive index	RI _b	Spectroscopic ellipsometry (630 nm)	1.88	2.36
	RI _i		1.88	2.93
Growth rate (Å/s)	GR _b	Constant current V _{th}	10.8	45.6
	GR _i		10	47
V _{th1h} (%)		HP4156	4.7	42.45
V _{th24h} - V _{th1h} (%)			2.02	19.21
J (A/cm ²) at -75 V			8.3×10^{-9}	3.2×10^{-6}

for the interface and distinguished respectively by b or i indices. Note that to determine the interfacial properties, the film is deposited by applying a rf power corresponding to the rf power ramp up at 1 s deposition time. Concerning electrical properties, leakage current in the PMD stack and DR of programmed cell after 1 and 24 h bake at 250 °C were analyzed.

A large composition domain is investigated as illustrated by the large bulk index $1.88 < \text{RI}_b < 2.36$ and an even larger interface one $1.88 < \text{RI}_i < 2.93$ (Table I). Table II summarizes all Pareto and variation analysis and shows, by arrow or nonmonotone dependence, each significant response variation when factors increase. A cell blackening illustrates their importance. For example, Si-H bond concentration is first controlled by the rf power and second parameter is the SiH₄ flow. It decreases when the rf power increases and it increases when the SiH₄ flow increases.

III. PHYSICAL $a\text{-Si}_x\text{N}_y\text{:H}$ PROPERTIES ACCORDING TO PECVD PROCESS PARAMETERS

Overall, the rf power and SiH₄ flow appear of huge importance. For the hydrogen bonds and RI_b, this dependence is clearly understood by the bonding decomposition effects. Indeed, at low rf power and high SiH₄ flow, the SiH₄ decomposition is predominant. It results in an increase of the silicon rate contained in the film, as displays by the RI increase. RI_i could be interpreted by the same way by reasoning with the power ramp up instead of rf power. Concerning the hydrogen bonds, the dependence with precursor gas ratio and rf power is well known: high SiH₄/NH₃ ratio and low rf power make Si-H predominant than N-H and inversely for N-H one. Then, tensile stress and low density value are obtained at low rf power because of lower electronic bombardment

during the process. Film physical properties knowledge will be used to understand how they impact the DR in the following part.

IV. IMPACT OF $a\text{-Si}_x\text{N}_y\text{:H}$ PROPERTIES ON DR

DR experiments have been performed at 250 °C on programmed cells. Figure 2(a) depicts the normalized V_{th} variation. This is represented according to bake time for the best and the worst cases of the DOE recipes. If the long term charge loss follows a similar dynamics (similar slope between V_{th1h} and V_{th24h}), the fast initial one varies from few percent up to 40%. It highlights how much the initial shift is a $a\text{-Si}_x\text{N}_y\text{:H}$ composition matter contrary to the intrinsic one. Thus, two DR DOE responses were defined to make the distinction between both mechanisms. The initial charge loss is monitored after 1 h bake time (V_{th1h}) and the intrinsic one at 24 h through V_{th24h} - V_{th1h}. This last is confirmed to be independent of deposition parameters, contrary to V_{th1h} (Table II). Precisely, it is shown that the SiH₄ flow mainly drives the V_{th1h} shifts. Putting this flow in its high level or increasing the SiH₄/NH₃ precursor gas ratio accelerates the initial charge loss. Consequently, degradation is increased with Si-rich CESL film. In addition, V_{th1h} increases when the rf power ramp up decreases, i.e., when interfacial layer is thick. This interfacial layer, being more Si-rich than the bulk, confirms the previous conclusion and explains the strong quasilinear relationship between the initial charge loss and RI_i [Fig. 2(b)]. On the other hand, stress and density do not play a role on the DR degradation—even on the intrinsic long term one, which is of importance for silicon nitride

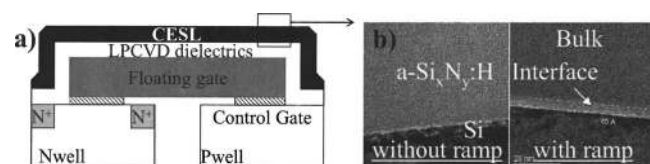


FIG. 1. (a) Schematic SP NVM and (b) $a\text{-Si}_x\text{N}_y\text{:H}$ CESL transmission electron microscope images without or with rf power ramp up.

TABLE II. DOE analysis responses vs factors (interactions not presented).

	[Si-H] _b	[N-H] _b	Stress _b	Density _b	RI _b	RI _i	GR _b	GR _i	V _{th1h}	V _{th24h} - V _{th1h}	V _{th1h}	J
A: SiH ₄ flow	↘	↘	↘	↘	↗	↗	↗	↗	↗	↗	↗	↗
B: NH ₃ flow		↗	↗		↘	↘	↘	↘	↘	No significant factor	↘	↘
C: Ramp RF					↘	↘		↗	↗			↘
D: RF Power	↘	↗	↘	↗	↘		↘					↘

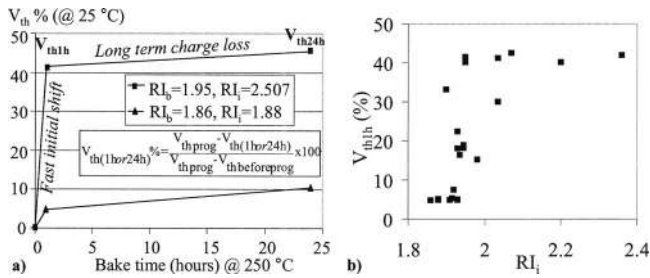


FIG. 2. (a) V_{th} for the worst and the better data retention $a\text{-Si}_x\text{N}_y\text{:H}$ recipe and (b) link between V_{th1h} and composition illustrated by the RI_i .

strained technologies,⁸ but in contradiction with stress reported results on double poly Flash cell.⁹ In conclusion, to minimize the initial charge loss, Si-rich film and thick interfacial layer must be avoided.

Why such a $a\text{-Si}_x\text{N}_y\text{:H}$ composition is degrading? First assumptions are based on a larger defect amount. To confirm it, leakage current (J) has been measured in the complete PMD stack, between the polysilicon gate and the metal 1 electrodes at room temperature [Fig. 3(a)]. Hysteresis method is used with scanning voltage between ± 150 V after an initial sweep from 0 V. Different defect contributions can be distinguished in the I - V characteristic represented with symbols. First of all, the more defect amount, the more leakage current. Then, a leakage current plateau appears, while voltage increases. It reduces the $a\text{-Si}_x\text{N}_y\text{:H}$ ability to store charge and is correlated to the large hysteresis opening observed between up and down sweeps. These different defect contributions are strongly dependent on the $a\text{-Si}_x\text{N}_y\text{:H}$ recipes and seem to be particularly linked with DR response. Indeed, the I - V of Fig. 3(a), in which the largest leakage and widest plateau are observed, corresponds to the worst DR case presented in Fig. 2(a). Note that almost no hysteresis opening and lower leakage are observed on the best recipe (curve without symbol). To be interpreted in the DOE analysis, the J parameter has been extracted at -75 V on the initial sweep. It ensures to characterize an initial defect state without trapped charge during previous cycle, which is not realistic during flash DR measurements. The bias is chosen to be sufficiently high to be outside the noise level and low to not enter in the trapping plateau. Results reported in Fig. 3(b)

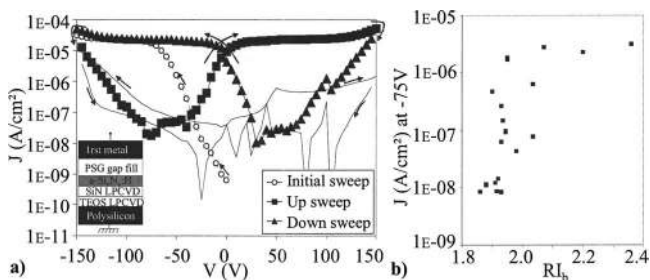


FIG. 3. (a) J - V on PMD stack. Curve with symbols refers to the worst $a\text{-Si}_x\text{N}_y\text{:H}$ data retention case ($RI_i=2.507$ and $RI_b=1.95$). Curve without symbol refers to the best $a\text{-Si}_x\text{N}_y\text{:H}$ data retention case ($RI_i=1.88$ and $RI_b=1.86$) and (b) leakage current measured at -75 V on the initial I - V sweep according to RI_b .

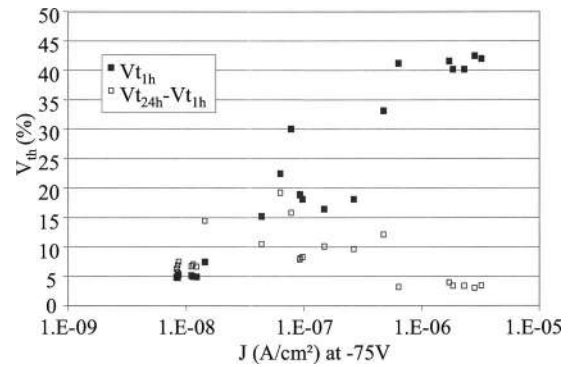


FIG. 4. Correlation between data retention degradation and defect amount contained in $a\text{-Si}_x\text{N}_y\text{:H}$ V_{th} as monitored by leakage current.

reveal an increase of leakage current, i.e., defect amount, with Si-rich $a\text{-Si}_x\text{N}_y\text{:H}$ film composition. Moreover, the quasilinear dependence between V_{th1h} and J (Fig. 4) indicates the strong relationship between DR and the CESL defect monitored through J . It is necessary to remind that J is only used to give information about defects amount in CESL. Indeed, it is not realistic to correlate directly the CESL leakage to DR due to the good quality thick LPCVD dielectric that encapsulates the memory and keep the CESL separated from the floating gate.

V. DR DEGRADATION MODEL

In Ref. 6, we have identified unexpected $a\text{-Si}_x\text{N}_y\text{:H}$ charge behaviors from electrical measurements performed on MIS structures. These charges have the ability to exist under two states: positive and negative, leading us to suspect a K center origin.¹⁰ UV erase enables us to neutralize this charge transforming K center in its neutral configuration K^0 . Moreover, under thermal activation, an electrical field leads to a charge displacement or more probably a carrier exchange between trap centers. It is supposed that during the DR bake, the FG polarity, under its programmed or erased states, creates an electrical field that can displace CESL charges from one interface to the other very similarly than during ionic contamination issue. An illustration is proposed on Fig. 5. At the beginning, the memory is in its virgin state and $a\text{-Si}_x\text{N}_y\text{:H}$ charges are uniformly distributed. This simplification gives a layer globally neutral and has ever been suggested by Warren

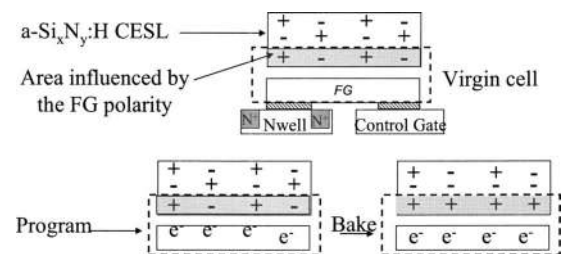


FIG. 5. Illustration of initial shift during data retention experiment of a programmed SP NVM cell. Gray area is influenced by polarity of the FG, which under its programmed states and under thermal activation attracts positive $a\text{-Si}_x\text{N}_y\text{:H}$ charges that screen those of the FG.

et al. for K centers.¹¹ Then, memory is programmed, giving a negative polarity in the FG. This negative “electrode” induces an electrical field in the $a\text{-Si}_x\text{N}_y\text{:H}$. This FG field influence is, of course, higher close to the FG and explains the strong influence of the CESL bottom interfacial layer—schematized by the gray filling. It was only during the high temperature bake that the $a\text{-Si}_x\text{N}_y\text{:H}$ charges can be displaced by the electrical field. It leads to a positive charge sheet at the bottom of the CESL due to hole attraction or electron repulsion between traps centers. Thus, these CESL charges screen the ones stored in the FG. This capacitive effect has been well modeled by Mora *et al.*³ The only way to distinguish this mechanism with classical ionic contamination effect is based on the Mielke cycle: During program and bake sequence, the behavior is similar and correction to charge motion. During UV erase step, in ionic contamination case, only memory is erased and the ionic charge are still present; on the contrary, in the case of CESL impact DR, the memory is erased and the K centers become neutral. This leads to completely different state and different response to the following bake. Note that such a difference is not visible when electrical erase is performed.

VI. CONCLUSION

The $a\text{-Si}_x\text{N}_y\text{:H}$ CESL influence on DR mechanism is clearly identified here. We have demonstrated, on a large

$a\text{-Si}_x\text{N}_y\text{:H}$ composition range, that Si-rich film and “interfacial” layer must be avoided to minimize memory charge loss. On the other hand, stress and density do not play a role. To optimize process deposition, it is particularly important to lower the SiH_4 flow and the rf power ramp up parameters. Indeed, they promote Si-rich films that were suspected to contain larger charge amount that screen charges stored in the FG.

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