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STUDY OF REAR PECVD DIELECTRIC STACKS FOR INDUSTRIAL SILICON SOLAR CELLS

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ABSTRACT: In this article, we used 2D simulation to evaluate the influence of the Metal-Insulator-Semiconductor (MIS) and fixed charge density contained in the dielectric layers which may be used for the passivation of the rear side of silicon solar cells. Negative fixed charge densities were found in PECVD SiO_x:H and SiN_x:H dielectrics by dark-capacitance-voltage measurements, using a new method more adapted to solar cell applications. Next, multicrystalline silicon solar cells based on the i-PERC process were made with PECVD SiO_x:H / SiN_x:H stacks of different thicknesses. I-V characterization showed open-circuit voltage and fill factor degradations for the processed cells compared to the reference. These degradations were analyzed by spectral response measurements, scanning electron microscopy and infrared thermography. It was found that the serigraphy paste and the laser impacts on grain boundaries were responsible for the degradations.

Keywords: Capacitance-Voltage Measurement, PECVD, Silicon-Oxide, Silicon-Nitride

1 INTRODUCTION

Reduction of the material cost share is needed to enhance the economic attractiveness of the photovoltaic technology [1]. One of the solution is to reduce the wafer thickness of crystalline silicon solar cells.

The standard aluminum back surface field (Al-BSF) induces mechanical constraint problems on thin wafers, typically below 180 μm-thick. This increases the breakage risk and may affect the production output. Al-BSF is also insufficient for surface passivation, since rear surface recombinations become of predominant importance in this thickness range. Therefore minimizing the aluminum coverage and developing new passivation schemes for the rear surface is one of the key points for decreasing silicon solar cell thickness [1-5].

A literature review tells us that three major cell architectures are currently under development to handle the rear surface passivation problem. They are mainly based on dielectric layers for passivation combined with aluminum contacts. The actual technology under study are: bifacial cells [2-3], Laser Fired Contact cells (LFC; Fraunhofer ISE) [4] and industrial-Passivated Emitter and Rear Cells (i-PERC; IMEC) [5].

The dielectrics used for passivation often consist in SiO_x:H (SiO) and SiN_x:H (SiN) layers deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD). This technology is one of the most promising solutions due to its limited thermal budget needed for the deposition, its reasonable surface passivation capabilities [6-8], and the availability of the PECVD system, widely used for SiN antireflection. Although the PECVD SiO/SiN stack is reputed to be one of the best candidate to passivate the rear side of the cells [7, 9], the SiO layer dielectric properties are not yet fully understood. The effects of the Metal-Insulator-Semiconductor (MIS) structure that is present in the i-PERC and LFC structures are still under investigation [1].

In the present article we used simulation in order to investigate the influence of the MIS structure and the dielectric fixed charge density on the cell efficiency. Then we determined the fixed charge density of the SiO and SiN layers by dark Capacitance Voltage measurement (dark-C-V) technique, modified to better meet the solar cell application. Lastly, solar cells based on the dielectric

structures were processed and characterized by I-V, quantum efficiency measurements, infrared thermography and Scanning Electron Microscopy (SEM).

2 DESSIS SIMULATION

2.1 Parameters

The 2D simulation was performed using ISE TCAD DESSIS [10]. The cell parameters used for the simulation are detailed in the table I. To highlight the rear side influence on the solar cell efficiency, a high value of the minority carrier lifetime was chosen (typical of FZ substrate). The rear surface recombination velocity (SRV) is similar to the result recently obtained using PECVD SiO/SiN stack [1, 9].

Table I: Solar cell parameters for the simulation.

Substrate		
Substrate type & doping	P (boron)	1.10 ¹⁶ cm ⁻³
Thickness	150 μm	
Minority carrier lifetime	240 μs	
Rear side		
Al-BSF doping & thickness	5.10 ¹⁸ cm ⁻³	5 μm
Contact coverage & material	12.5%	Aluminum
Dielectric materials tested	SiO ₂	Si ₃ N ₄
Dielectric thicknesses tested	100 nm	500 nm
Rear SRV	300 cm.sec ⁻¹	

Two rear structures were simulated. The first structure is similar to bifacial solar cell: the contacts are present only where the dielectric layer is absent. The second structure is based on LFC and i-PERC cells: the contacts cover the whole rear surface including the dielectric layer.

For both structures, we varied the type of dielectric used on the rear side (SiO₂ or Si₃N₄) and the thickness of the layer (100 nm or 500 nm). The dielectric permittivity of SiO₂ and Si₃N₄ are respectively close to those of SiO and SiN.

2.2 Simulation Results

The evolution of the solar cell efficiency with the dielectric fixed charged density (Q_f) is plotted on the Figure I. Under high inversion or high accumulation, the cell efficiency is nearly the same. For all rear sides simulated, there is a Q_f range where the efficiency falls deeply and which may correspond to high rear surface recombination rate. The carrier recombinations become maximal when the free carrier ratio of electron and hole is equal to the inverse of their respective capture cross section ratio:

$$\frac{n}{p} = \frac{\sigma_p}{\sigma_n}$$

with n (p) the electron (holes) density and σ_n (σ_p) the electron (hole) capture cross section. Since σ_n is about 100 time superior to σ_p , $p \approx 100 n$ when the recombination rate is maximal [11-12]: the interface Si/Dielectric is thus in desertion condition.

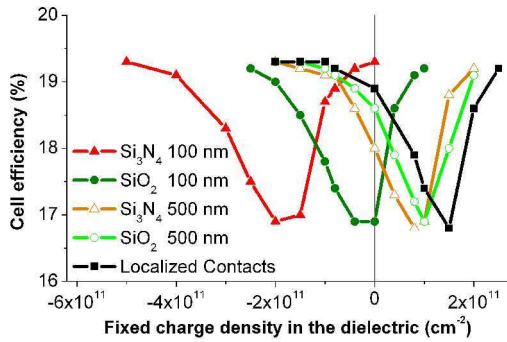


Figure I: Evolution of the solar cell efficiency with Q_f for SiO_2 and Si_3N_4 dielectrics of two different thicknesses. The aluminum contacts cover the whole surface, except for the localized contacts case.

In the case of localized contacts, this condition happens when the dielectric has Q_f near $1.5 \cdot 10^{11} \text{ cm}^{-2}$, independently of the dielectric thickness. When the contacts cover the whole surface, including the dielectric, we have to take into account the band diagram modification at the Si/Dielectric interface. The difference between the aluminum work function (4.08 eV) and the P-Type silicon work function being negative, the metal presence makes the energy bands of the silicon to bend to lower energy at the interface. The metal has thus a similar influence as a positive Q_f on the band diagram at the interface. This explains why the recombination rate becomes maximal for lower Q_f in the dielectric when the contacts are on the whole surface.

Moreover, depending on the dielectric constant and thickness, the influence of the aluminum may be enhanced. When the layer is thin, the metal is nearer the Si/Dielectric interface and the aluminum-silicon work function difference has a greater impact on the band bending. This effect might be stronger if the insulator has a high dielectric constant (Si_3N_4 in this case).

Consequently, thickness and dielectric constant values can strongly affect the Q_f condition for the maximal carrier recombination rate, as it can be seen in the Figure I. With a 100 nm thick layer of Si_3N_4 , the cell efficiency becomes minimal when Q_f is negative.

2.3 Conclusion

The simulation shows two important points. Firstly, an inversion layer on the rear side may not be problematic towards the solar cell efficiency, as it was also established by Mittelstadt et al. [13]. Secondly, depending on the dielectric thickness and permittivity, negative Q_f is not always beneficial for a field effect passivation on P type silicon.

3 CAPACITANCE-VOLTAGE MEASUREMENTS

To measure the fixed charge density of our PECVD dielectric films, we used the capacitance-voltage method (C-V). Two types of measurements were carried out. The standard dark-C-V was made by applying a voltage ramp from the accumulation to the inversion conditions, and back from the inversion to the accumulation conditions, in order to reveal a possible hysteresis effect.

From this first measurement, the flat band capacity (C_{FB}) is extracted. Then, we performed a second characterization by applying a null voltage during five minutes and slowly polarized the samples to the flat band voltage (V_{FB}). We called this method “weak polarization” (WP).

The WP method is more similar to the working conditions of the dielectric films on the rear side of solar cells than the standard dark-C-V measurement. The metal and the silicon stay indeed nearly at the same potential. This method can avoid traps charging effect when the MIS is strongly polarized, which may change the determination of Q_f .

3.1 Experimental

Three dielectric layers and one dielectric stack were studied: a standard silicon nitride usually used as antireflection coating (SiN), a rich-silicon silicon nitride (SiNr), a silicon oxide layer (SiO) and a stack of silicon oxide cover by a standard silicon nitride layer (SiO/SiN). All these structures have been deposited on 2 inches N-type monocrystalline wafers, (100) oriented. They have a 5 ohm.cm resistivity and a thickness of 280 μm .

The deposited layers thicknesses were verified by ellipsometric measurements and were contained between 40 and 50 nm, except for the SiO/SiN stack (40 nm of SiO and 25 nm of SiN). All these layers were elaborated in a direct PECVD working at 440 kHz and 370°C with ammonia (NH_3), silane (SiH_4) and nitrogen protoxide (N_2O) as precursor gases.

After the deposition, the samples were annealed in a belt furnace from Photowatt. Next, aluminum plots were evaporated in order to form the Metal-Insulator-Semiconductor structure on all the samples. The rear contact was made with indium-gallium and silver pastes.

The C-V characterizations were performed with a probe station using standard dark-C-V measurements followed by the WP characterization (performed on a neighboring aluminum plot). The Q_f determination was done from the flat band capacity value [14].

3.2 Q_f results

The fixed charge density results are presented in the Table II. Two values are given for Q_f with the dark-C-V measurement. This is due to the hysteresis effect present in all the samples. This hysteresis is caused by electrons trapping and holes injection from the dielectric in accumulation condition (see Figure II). The opposite effect may also happen in inversion condition. This hysteresis

effect is avoided when using the WP method. We will thus rely mainly on the fixed charges density obtained by this second method.

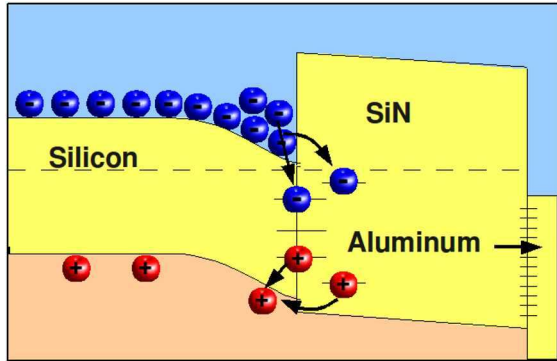


Figure II: Illustration of the influence of SiN traps which may create a hysteresis effect.

Table II: Q_f values calculated with the dark-C-V and the WP results. The blue (red) value means that the global charge is negative (positive). The value is black when the sign is not determined.

Fixed charge (cm^{-2})	by dark-C-V	by WP
SiN	-2.0.10 ¹¹ /+1.9.10 ¹²	-1.5.10 ¹¹
SiN annealed	-1.5.10 ¹² /+1.9.10 ¹²	-1.3.10 ¹¹
SiNr	+0.3.10 ¹¹ /+1.2.10 ¹¹	+0.6.10 ¹¹
SiNr annealed	-0.2.10 ¹¹ /-1.8.10 ¹¹	-1.2.10 ¹¹
SiO	-8.0.10 ¹¹ /-1.6.10 ¹²	-2.3.10 ¹¹
SiO annealed	-2.6.10 ¹² /-7.0.10 ¹²	-1.3.10 ¹²
SiO/SiN	-1.3.10 ¹² /+1.1.10 ¹¹	-2.7.10 ¹¹
SiO/SiN annealed	-0.2.10 ¹¹ /-1.5.10 ¹²	-1.8.10 ¹¹

Surprisingly, most of the dielectric layers exhibit negative fixed charge before and after annealing. This is even true for the standard SiN, reputed to have positive fixed charges [15-16]. The detection of positive fixed charge may be caused by holes capture or electron release in the dielectric with the polarization when using the standard C-V measurement.

The Figure III highlights the behavior of the SiN layer with six consecutive measurements: the hysteresis effect is strongly reduced and the calculated fixed charge becomes clearly positive and superior to 10^{12} cm^{-2} , as it can be found in the literature. The measurement reproducibility for the other layers is clearly better than for the SiN. The SiO keeps a negative Q_f even after several dark-C-V characterizations. Nevertheless, more investigation is in progress to identify the type of traps responsible of the negative charge in the dielectrics.

Annealing the layers does not change the sign of Q_f (except for SiNr) but strongly increase the hysteresis effect due to trap formation in the dielectric layer near the Si/Dielectric interface. The layers seem to degrade more or less with the annealing, depending on their type. The SiO/SiN stack is one of the most stable structures. The Figure IV shows the dark-C-V curve for SiO, SiN and SiO/SiN after annealing. A smaller hysteresis effect is indeed visible for the SiO/SiN stack than for the other dielectrics. This is in agreement with Agostinelli et al.: they pointed out the thermal stability of this structure, even after successive annealing, due to its stable passivation properties [1, 17].

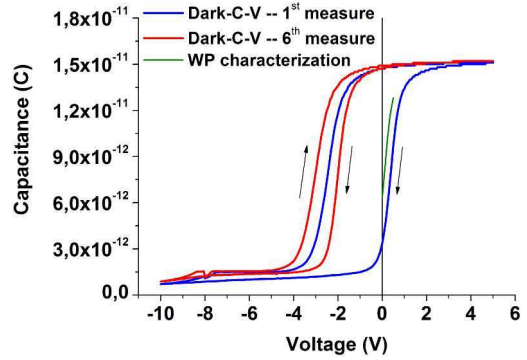


Figure III: C-V curves for the SiN sample before annealing obtained by C-V measurement. The Q_f evolution toward positive fixed charge is clearly visible.

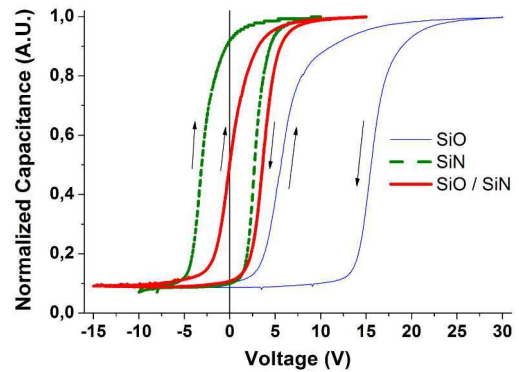


Figure IV: Comparison between normalized dark-C-V curves for the SiO, SiN and SiO/SiN layers after annealing.

3.3 Conclusion

The C-V characterizations show that the PECVD dielectric layers may have negative fixed charges in their bulk. Moreover, the SiO/SiN stack seems more thermally stable in comparison with the other dielectric layers. Thus, it may be more efficient for an application on the rear side of solar cells.

4 SOLAR CELL RESULTS

4.1 Experimental

Multicrystalline silicon solar cells were elaborated, on $125 \times 125 \text{ mm}^2$ wafers, $200 \mu\text{m}$ thick and with resistivity of 1 ohm.cm . SiO/SiN dielectrics stacks are deposited by PECVD on the back side. Three different SiO/SiN stacks thicknesses were tested: thin (65 nm), standard (900 nm), and thick (900 nm). The layers are opened by UV laser ablation ($\lambda=355 \text{ nm}$) and covered with standard aluminum serigraphy before being annealed. A set of standard solar cells with a full rear side aluminum back surface field (Al-BSF) was also made in order to compare the efficiency.

4.2 Current-Voltage characterization

The electrical results (Table III) depend strongly on the thickness of the SiO/SiN stacks. The best results for the cells with a dielectric stack are obtained for thick layers, in accordance with IMEC results [17-18]. Minority

carrier lifetime investigation shows that the improvement of the V_{oc} and J_{sc} is due to a better passivation effect, mostly caused by the reduction of the MIS effect and a thicker SiN layer. In fact, as we presumed in the simulation part, the Si/Dielectric interface is less affected by the aluminum coverage with a thick dielectric stack. It may also bring additional hydrogen to passivate the rear surface and the bulk of the substrate.

Table III: Solar cells results for various SiO/SiN stacks thicknesses.

Cells	V_{oc} (mV)	J_{sc} (mA.cm ⁻²)	FF(%)	η (%)
Al-BSF	591	31.68	74.2	13.77
SiO/SiN 65 nm	573	29.04	74.0	12.21
SiO/SiN 500 nm	582	30.34	72.7	12.72
SiO/SiN 900 nm	585	31.33	71.5	12.97

The fill factor decreases when the SiO/SiN stack is thickened. In fact, for thick dielectric stack, the serial resistance of the cells can be 20 percent higher than for the reference cells. As illustrated in the SEM picture of the rear contact (Figure V), instead of having a thick Al-Si alloy as presented by Ma et al. [18], a cavity is formed under the dielectric layers and limits the contact between the aluminum and the silicon. When the aluminum begins to dissolve the silicon during the firing step, an insufficient viscosity might prevent the serigraphy paste from filling up the hole, and cause the silicon to be absorbed in the paste. An optimized paste and firing conditions, or larger laser point contacts, may be needed to avoid this phenomenon.

4.3 Spectral Response measurement

Even with increasing the dielectric stack thickness, the open circuit voltage stands below the Al-BSF reference. In order to investigate which factor may cause lower V_{oc} , we carried out spectral response measurements. We performed two characterizations with and without a bias light to avoid a low rear passivation due to a weak minority carriers injection [7, 13]. A typical internal quantum efficiency (IQE) obtained for solar cells with a thick SiO/SiN stack is displayed in the Figure VI.

Although the additional bias light is less powerful than the standard solar spectrum, the comparison of the IQE in the infrared range proves that the rear passivation by the SiO/SiN stack is effective. The low V_{oc} value may thus be ascribed to another cause. Note that the low infrared response does not disappear for thin SiO/SiN stack (65 nm) due to a limited passivation effect.

On the other hand, the cell with the dielectric stack exhibits a lower IQE than the reference cell on the whole spectrum. These results point out a homogeneous degradation affecting the whole current. In order to identify the source of the degradation we performed on the standard cells a laser firing step before the serigraphy of the contacts, in the same condition than for the “dielectric” cells. The processed cells show similar V_{oc} and efficiency degradations as the cells with a rear dielectric stack. We may thus conclude that the V_{oc} degradation is mainly caused by the laser step, which probably entails parasitic shunting problems. To confirm this hypothesis, we use infrared thermography to detect abnormal heating.

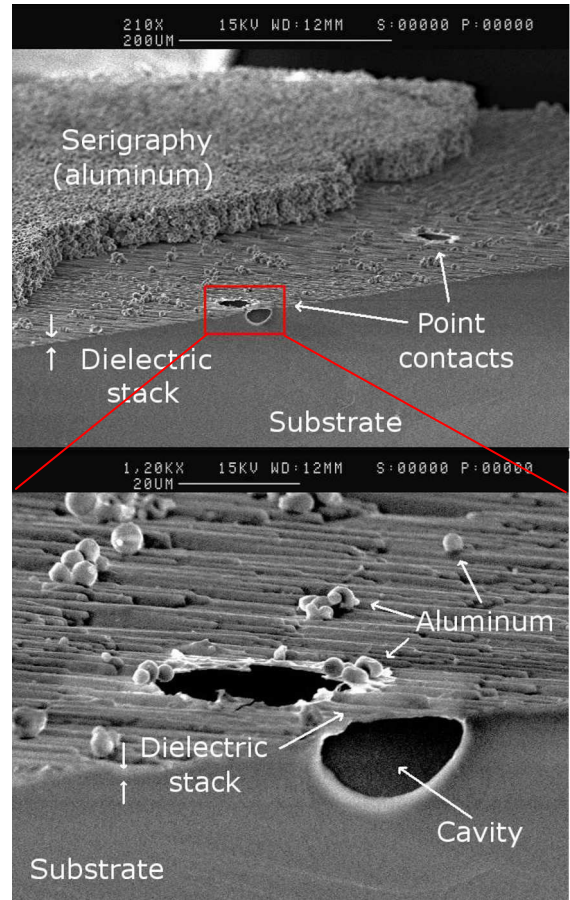


Figure V: SEM pictures of the cross section of a cell with a dielectric stack. The serigraphy was partially removed due to the cell cut.

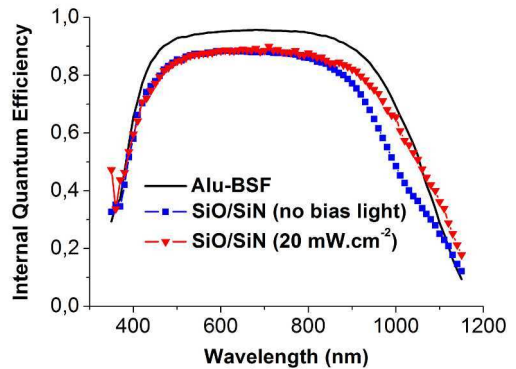


Figure VI: Internal quantum efficiency of a cell with a 700 nm SiO/SiN stack, with and without a bias light.

4.4 Infrared thermography characterization

By polarizing the cells in inversion, the infrared thermography is able to detect abnormal heating due to local parasitic shunting [19]. Although the reference cells, without laser, do not show significant shunt, the cells with dielectric stacks exhibit several places where a high current is detected. The high majority of the heating sources are localized near grains boundary of textured gains, corresponding to the position of front side metallization. The Figure VII emphasizes the localization of the shunts in comparison with the corresponding front side

(the picture was mirrored to make it correspond to the rear side).

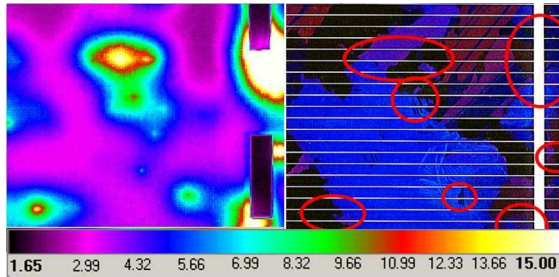


Figure VII: Infrared Thermography picture of the rear side of a solar cell with a SiO/SiN stack (900 nm) (left). Mirrored photography from the front side of the same cell zone (right), with the shunt positions underlined.

We note that the laser impacts are not directly responsible of the shunts because large surfaces exist without any abnormal heating. To explain the localization of the shunts, we may suppose that the texturized surface might be sufficient to concentrate locally the laser pulse, as it was demonstrated by Knorz et al. [20]. Then, when the laser hits the surface between two grains, the energy might affect the grain boundary integrity, by increasing the extended defects concentration, dissolving the impurity precipitates and degrading the front emitter. This phenomenon might be enhanced by the constraints occurring during the contact formation and also by the rear reflectivity in the ultraviolet range. More investigations are in progress to verify this hypothesis.

5 CONCLUSION

In the present article we found that the MIS structure and the Q_f of the dielectrics used as passivation coating on the back side of solar cells can strongly enhanced the carrier recombination. The stack thickness, the dielectric constant and the Q_f have to be carefully chosen to avoid high rear recombinations.

Q_f was investigated in PECVD SiN and SiO layers with capacitance voltage measurement a global negative charge was found. Besides, with a reduced hysteresis, the SiO/SiN stack appears to be more thermally stable than the other layers.

Solar cells with SiO/SiN stacks were made. The solar cells efficiency depends strongly on the thickness of the SiO/SiN structures, with better results for thick stacks. The reasons of the medium fill factor and V_{oc} are studied by spectral response, scanning-electron microscopy and infrared thermography. It was found that the serigraphy is not optimized for point contacts because it entails cavity formation instead of a good silicon-aluminum alloy in the hole created by the laser. Several parasitic shunts were also detected along the grains boundary. They seem to be caused by the laser impacts on the boundary which might degrade the front emitter.

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