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# Low Cost SU8 Based Above IC Process for High-Q RF Power Inductors Integration

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**Keywords:** Above-IC, Copper, Electroplating, High-Q, Inductor, Process, Negative Photoresist, SU8.

**Abstract:** This paper presents a new process for integration of high-Q RF power inductors above low resistivity silicon substrates. The process uses the SU8 resin as a dielectric layer. The aim of using the SU8 is to form thick dielectric layer that can enhance the performance of the inductors. The flexibility of the process enables the possibility to realize complex shaped planar inductors with various dielectric and metal thicknesses to meet the requirements of the application. Q values of 55 at 5GHz has been demonstrated for an inductance value of 0.8nH using a 60  $\mu\text{m}$  thick SU8 layer and 30  $\mu\text{m}$  thick copper ribbons.

## Introduction

Above-IC integration of passive devices is one of the most promising enabling technologies for developing high performance low-cost miniaturized RF components. During the last decade, several achievements were realized in terms of technological developments. However, these technologies are restricted to low or medium power devices because of several limitations such as, mainly, high mechanical strain and low achievable thickness for dielectric films. Thus, these above-IC technologies are not able to meet the requirements for high-Q inductor integration on top of low resistivity silicon substrates, such as high power LDMOS substrate.

In order to overcome these limitations and to fulfill the high-Q inductors requirements for RF power devices, we developed a low cost, SU8 based above-IC process. Up until recently, the SU8 resin was used as a photoresist in microelectronics industry, to provide a high-resolution mask for fabrication of semiconductor devices. In a previous work [1], we demonstrated the interest of this resin as a dielectric material for RF applications below 10GHz. In this paper, we will present the technological steps of an above-IC process and prove its effectiveness for RF power applications by designing and integrating High-Q above-IC inductors.

## Above-IC process technological steps

In order to integrate high performance passive RF power devices like inductors, it has been advised to use a thick dielectric layer ( $> 50\mu\text{m}$ ) to decrease magnetic loss into the substrate or the ground shield [2]. After investigating several dielectric photoresists (BCB, Intervia ...), the SU8 was chosen for its great technological properties (high thicknesses, low mechanical stress, easy deposit ...).

However, using high dielectric thicknesses results into technological challenges since vias must be used to connect the integrated passive device to the underlying chip's access pads. Thus, filling these vias cannot be done using conventional metal evaporation or sputtering techniques because of their limitations (low thicknesses, high price ...). Instead, metal electroplating must be used.

Electroplating requires the deposit of a seed layer and the usage of molds to restrict the growth of metal to required areas/locations (Fig. 1b). These molds are formed using a thick photoresist which technological properties (viscosity, opening aspect ratio,...) set via characteristics such as height, shape and minimum sizing. Moreover, the photoresist must be cleaned out at the end of the step in order to be able to etch the seed layer. For this process, we used a negative sacrificial photoresist called the BPN.

The developed above-IC process is composed of here after major steps (Fig. 1):

1. Vias electroplating: This step requires the sputtering of a Ti/Cu seed layer (a) ( $500\text{\AA}/1000\text{\AA}$ ), the deposition of the sacrificial photoresist BPN (b), the electroplating of Cu vias (c), the stripping of the BPN (d) and the etching of the seed layer (e).
2. Dielectric deposit: Deposit of the SU8 (3050) resin using spin-off (f). After this step, mechanical polishing can be necessary to level the surface (g).
3. Ribbons electroplating: This step requires the sputtering of a Ti/Cu seed layer (h) ( $500\text{\AA}/1000\text{\AA}$ ), the deposition of the sacrificial photoresist BPN (g), the electroplating of Cu ribbons (i), the stripping of the BPN (j) and the etching of the seed layer (k).

The deposition of the BPN requires a prebake at  $120^\circ\text{C}$ , an UV (365nm) exposure and a development phase. The parameters of these steps depend on the desired thickness of the photoresist [3].

The deposition of the SU8 requires a prebake at  $95^\circ\text{C}$ , an UV (365nm) exposure, a post exposure bake at  $95^\circ\text{C}$ , a development phase using PGMEA (Propylene Glycol Methyl Ether Acetate) developer and finally a hard bake (can be omitted). As for the BPN, the parameters of these steps depend on the desired thickness [4].

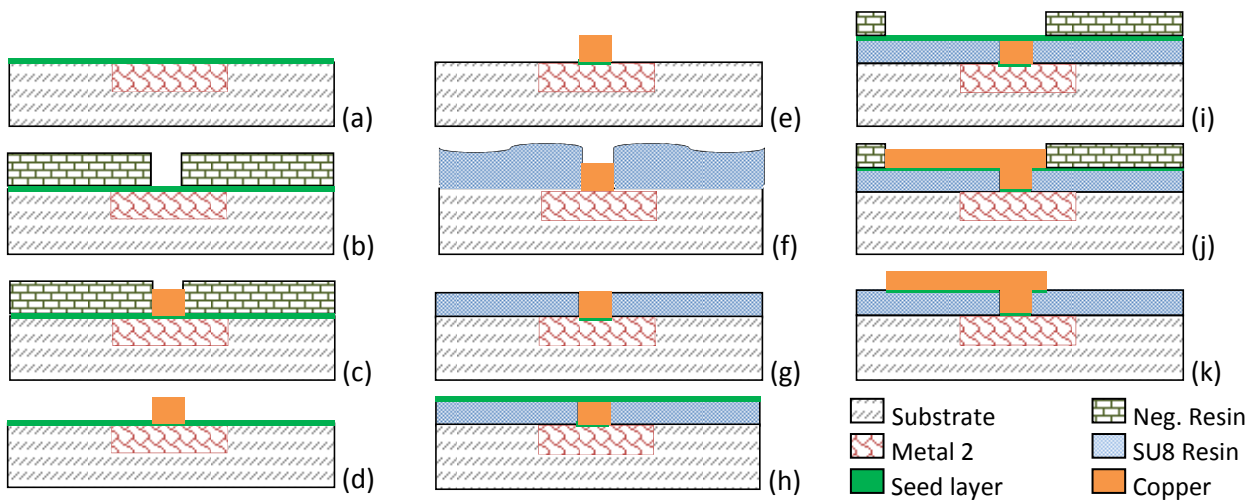


Fig. 1: Above-IC technological steps

### Above-IC inductors: Experimental result

To demonstrate the effectiveness of the developed process, we have fabricated high-Q inductors (Fig. 2) above a low resistivity silicon substrate ( $8\text{m}\Omega\cdot\text{cm}$ ). The structures are formed by firstly electroplating a  $2\mu\text{m}$  thick copper Cu solid ground shield, then growing  $60\mu\text{m}$  thick Cu vias followed by spin-coating a  $60\mu\text{m}$  thick SU8 layer, and finally, electroplating  $30\mu\text{m}$  thick Cu ribbons. Vias and ribbons can achieve a height /size aspect ratio of 16/1.

A vector network analyzer (Anritsu 37397C) and a probe station are used for microwave S-parameter measurements up to 20 GHz. A SOLT calibration is performed to locate the reference

planes at the probe tips and thru/open/short standards have been implemented and are used to de-embed the coplanar tapered probing pads.

Measurements of these inductors exhibit a  $Q$  value of 55 at 5 GHz for a total inductance value of 0.8 nH (Fig. 3). The good agreement between measurements and simulations must be pointed out, which validates both our inductor optimization and the technological process control.

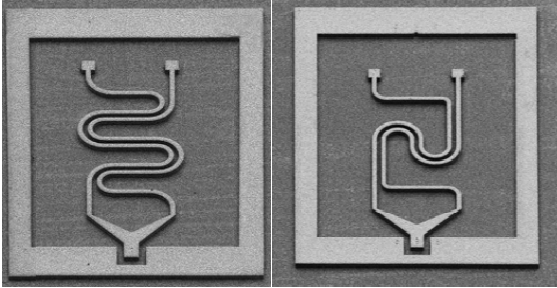


Fig. 2: SEM micrograph of SU-8 based power inductors

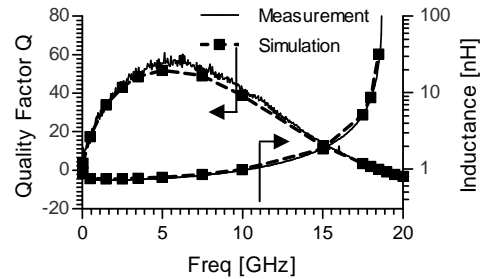


Fig. 3: Measurement vs. simulation of the inductor's  $Q$  factor and inductance value

## Conclusion

In this work, we have detailed an SU8 based above-IC process that enables the integration of high- $Q$  RF power inductors. The presented process uses only few easy technological steps, which make it low cost and suitable for manufacturing. The effectiveness of the process has been demonstrated by integrating high- $Q$  (55@5GHz) power inductors on an  $8\text{m}\Omega\cdot\text{cm}$  high power LDMOS silicon substrate. Its potentialities are quite important as well: since we processed SU8 thicknesses up to  $400\mu\text{m}$ , this technology can fit a large range of applications like on chip antenna integration, packaging ...

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