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Small Size High Isolation Wilkinson Power Splitter for 60 GHz Wireless Sensor Network Applications

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Abstract—This paper shows a very compact Wilkinson power splitter for high integrated millimeter wave systems. The approach, to reduce the component's size, is based on the lumped component transformation for the lines. The simulation on the splitter structure shows a very wide band with 0.5 dB of maximum insertion loss and only 0.07 dB of maximum output amplitude imbalance. The input return loss is better than -21 dB within the whole band of interest (57 - 67 GHz) the output return loss is better than -21.5 dB for the same band. The isolation between the two outputs is better than -20 dB. The occupied area for the entire structure is around 0.0055mm^2

Index Terms—CMOS, divider, power splitter, Wilkinson.

I. INTRODUCTION

During the last decade the research on transceiver systems operating on 60 GHz free band had an unstoppable growth. Thanks to the reduction of the gate size, the cut-off frequency in the silicon device increases achieving the CMOS employment in this slice of market. After the 130 nm generation, the CMOS device has prevailed the III-V group materials in particular for commercial applications. The Monolithic Microwave Integrated Circuits (MMICs) have been left to military and spatial applications. The Radio Frequency Integrated Circuits (RFICs) had become the new low cost commercial way.

In terms of performances the two devices categories are very different. In the RFIC there are different constraints compared to MMIC. First of all the performance on the active devices: in the CMOS technology the short channel and the very thin gate oxide impose limited supply voltage to avoid the break of the transistor. Consequently the admitted output power is highly limited. For the MESFET or HEMT thanks also to their physical constitution the supply voltage is higher as well as the achievable output power. Another not negligible aspect for the CMOS technology is the losses on the substrate; these conditions impose a limitation on the interconnection lines' dimension, to limit the power dissipation on the substrate.

Considering the last constraint the target for the RFIC architecture is the minimization of the entire system size to mitigate the substrate losses. In the wireless sensor network, minimizing the losses in the payload signal path, allows a smaller power dissipation and this is fundamental for battery driven systems. To increase the rejection of

the spurious signal and perform the transfer of information architecture with balanced architecture and in phase and quadrature signal (I/Q) have been developed. In the

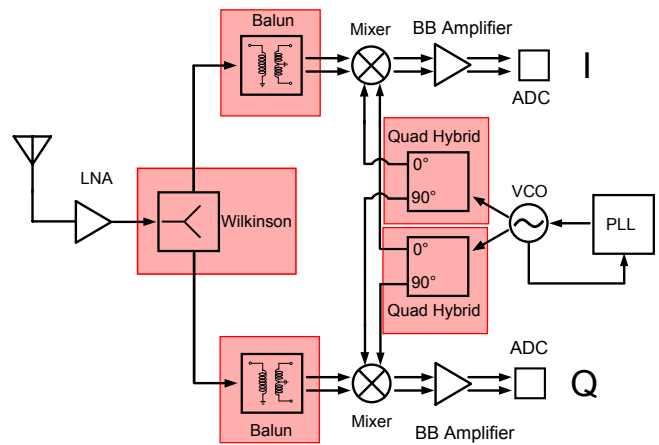


Fig. 1. Principal passive blocks (highlighted) for a full balanced I/Q receiver in 60 GHz application.

architecture shown in Figure ?? there are many different passive blocks to allow power splitting, imbalanced to balanced transformation and a 90 degree phase shift. The effectiveness of the system is strictly dependent on the behaviour of these passive components. The quality of the active blocks become useless if the passive parts have a poor response. In MMIC technology the employment of Wilkinson splitters, Marchand balun, hybrid branch line or Lange coupler are widely used. The dimensions of MMICs chips allow the use of this components because the dimension of each single blocks is proportional to the wave length of the signal. Hence, the design of the passive block is relative easy and allows good response. In the RFIC the wavelength is much smaller than the block dimension and with a relative permittivity around the 4.12 the dimension of $\lambda/4$ is near to $650\text{ }\mu\text{m}$. These dimensions are huge if compared to the typical dimension of 65 nm active building blocks. The dissipation in the silicon substrate attenuates the radio frequency (RF) signal and the derived noise destroys the Signal to Noise Ratio (SNR). In the literature there are many different approaches to reduce the block dimension. Slow wave approach is one. By this technique

is possible to reduce the length of the lines by a factor of 0.7 [?]. Another approach, proposed by J-G Kim [?] is based on the lumped component. This second approach is interesting and it will be investigated in this paper. The build of the Wilkinson has been done in seven metal layer plus Alucap metal layers of the ST Microelectronics 65nm CMOS technology. Section II gets a brief description about the architecture and features of Wilkinson divider. Section III summarizes the principle of function of the lumped component representation. Section IV explains the model of the inductance taking into account the influence of the technology constraints and their implication on the complete structure. Section V shows the obtained Wilkinson structure with the complete simulation results. The aim of this paper is to propose a design flow for the Wilkinson power divider underlying the principal issues, shown in the next sections and giving the solution to overcome them.

II. WILKINSON DIVIDER ARCHITECTURE

The Wilkinson divider is an important component with a very simple architecture. The role of this element is the split of its input signal into two different parts maintaining the phase and amplitude equilibrium between the two output ports. An important characteristic in the Wilkinson splitter is the reciprocal high isolation between the two output port. This feature is the great advantage of the Wilkinson splitter. If a little structural difference on the two symmetrical chains occurs, a part of signal can be returned back. In the Wilkinson divider a shunt resistance placed in correspondence of the output port blocks the signal and avoid the interfering propagation through the other parts of the circuit.

III. LUMPED ELEMENT REPRESENTATION

It is know that there are two different lumped component architecture to reproduce the behaviour of a section general lines: the T and Π representation. Figure ?? shows the second one. Adopting the Π scheme the admittance matrix

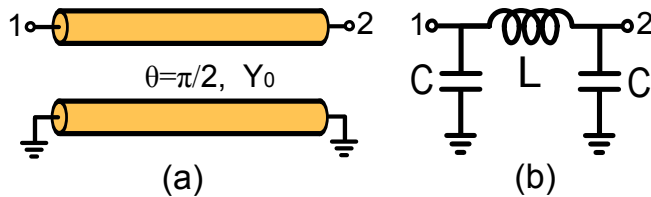


Fig. 2. Lumped model representation for a quarter wave line length.

for a lines with an electrical length of θ are:

$$Y_{Line} = \frac{-jY_0}{\sin \theta} \begin{bmatrix} \cos \theta & -1 \\ -1 & \cos \theta \end{bmatrix} \quad (1)$$

with

$$\theta = \frac{\pi}{2} \frac{2\pi f}{2\pi f_0} \quad (2)$$

Where f_0 is the central frequency and $Y_0 = 1/Z_0$ is the characteristic impedance (50Ω) of the input and output ports. For the frequency $f = f_0$ i.e. $\theta = \pi/2$ is obtained a quarter wave length for the line. Applying the equation for the ABCD matrix [?] at Formula ??, it becomes:

$$Y_{\Pi} = \frac{1}{-j\omega L} \begin{bmatrix} 1 - \omega^2 LC & -1 \\ -1 & 1 - \omega^2 LC \end{bmatrix} \quad (3)$$

Where L and C are the series inductance and shunt capacitance of the lines. For the Wilkinson $\lambda/4$ lines the lumped component values are:

$$L_{\sqrt{2}Z_0\Omega} = \frac{1}{Z_0 2\pi f_0} = 187.5pH \quad (4)$$

and

$$C_{\sqrt{2}Z_0\Omega} = \frac{Z_0}{2\pi f_0} = 37.5fF \quad (5)$$

The equivalent circuit composed by the previous lumped element is shown in Figure ??(b). A circuit simulation by Agilent ADS software was done, (not showed here), to confirm the theoretical behaviour of the circuits.

IV. LUMPED INDUCTOR DESIGN

In the ST Microelectronic technology is possible to use the last three metals (6th, 7th an Alucap layer) to build an inductor having good performance. The choice of the inductor shape is critical to achieve the best performance: multi-metal or planar structure is the first step in the inductor design. The advantage of the multi-metal approach is the concentration of the magnetic field and the reduction of the coil planar surface. The drawback is a parasitic coupling capacitance between the superimposed coils causing structure auto-resonance frequency dropping. The design of a coil with an operative band near the auto-resonance frequency is not allowed because the inductance value changes for a large bandwidth signal and destroys the ideal response of the entire block. Instead, a planar structure minimize this problem as the parasitic capacitive coupling is limited at the fringing coupling between each following run of the line. This second shape increases the occupied surface indeed, but also increases the resonance frequency. The choice of the metal layer to use for the coils' design has been determinate by practical considerations based on the physic of the system. To build the principal coil of the inductor, the best solution is using the 7th copper metal layer. This layer combine the higher conductivity property compared to 8th aluminium layer and minimize the losses influence in the silicon substrate. In this condition the obtained quality factor for the inductor increases. [?].

Once fixed the shape of the inductance, the second step is the inductance value optimization. Differently from the lumped capacitance existing on the CMOS Design Kit, the equivalent circuit of the coils is far from an ideal lumped inductance. Dickson et al. in [?] show an equivalent lumped circuit to model the spiral inductor. During the integration phase between the two coils and the shunt capacitance these parasitic effects are not negligible. To consider these effects, an iterative procedure has been employed to design the optimal spiral inductor.

The software used to conduct this optimization are:

- 1) ASITIC, for the first step sizing of the coil;
- 2) Sonnet 12.52, for the electromagnetic simulation;
- 3) Agilent ADS, for the synthesis of the complete structure.

The first step on the coil design has been fixed with ASITIC. This software in fact gets a good compromise between the accuracy and simulation speed. To maximize the accuracy on the simulation the successive analysis have been executed with Sonnet environment. The experience in spiral inductor in 60 GHz applications with Sonnet has been demonstrated by Kraemer et al. in [?]. In this paper another aspect is also taken into account i.e. the influence of the "dummy" metal around the coils. These parts of small floating copper are present to assure the minimal concentration of metal among the different layers. Their presence is necessary to avoid undesired mechanical stress on the superimposed layers and to allow a smooth surface in the different metal level. The presence of these inactive metals changes the magnetic flows around the coils as well as the inductive response. Figure ?? is a 3D Sonnet representation that highlights the difference between the same coils with and without the dummy metal. As is possible to see the presence of the dummies has a strong influence on the inductor value. The EM simulation of the structure

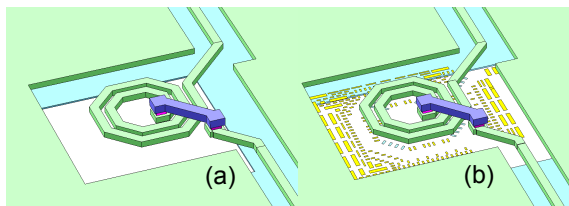


Fig. 3. Example of simulated inductance with (a) and without(b) dummy metal. The size the mesh and the boundary condition are the same for the two different structures.

with dummy is very difficult to do because it needs a large amount of memory that usually is not possible to satisfy. In this case to estimate the dummy influence an approximation on the metal characteristics has been done. Instead to consider the dummies like a solid blocks they have been model like a ideal metal sheet. In this condition the number of mesh cells remains low and it is possible to understand the variation on the inductance response. This

method does not confirm an exact prevision on the realized coils response but contributes to increase the fitting from the measure results with the EM simulation. Figure ??

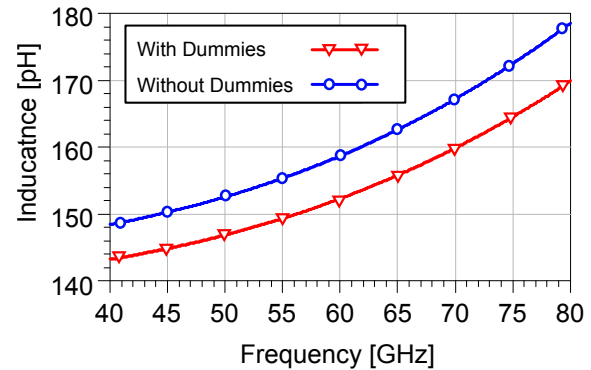


Fig. 4. Difference in terms of inductance value between the same structure, (represented in Figure ?? with(b) and without (a) dummy metal.

shows the inductance of the two inductor shown in Figure ??. As it is possible to see, the difference between the two coils is remarkable.

V. COMPLETE WILKINSON STRUCTURE

The inductor design for the Wilkinson divider block is only the first step. Another important effect to take into account and simulate is the potential EM coupling between the two coils that create the output branch. Figure

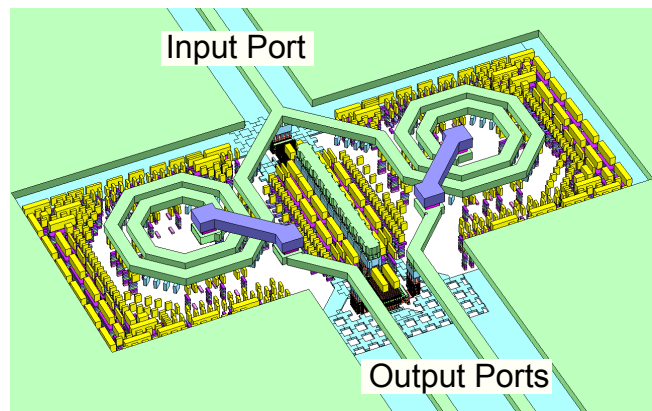


Fig. 5. 3D view of lumped Wilkinson power splitter. A thick metal model representation of dummy metal are showed. In this configuration a complete EM analysis is impossible because it requires an huge quantity of memory (higher than 163 GB!)

?? show the 3D complete structure of the Wilkinson divider. A metallic wall, joined to the ground, divides the 2 coils to attenuate the undesired mutual coupling effect. A simulation of the entire structure is needed to evaluate the entire structure at the same time. Otherwise, a not considered effects like parasitic coupling, can modify the response of the splitter and change mainly the input and

output return loss. After the simulation using Sonnet tool, a small coupling effect that changes the total response has been found and a second optimization run is needed. At this state of the design, small variation in terms of coils size, are enough to re-establish the expected response. Figure ?? shows the input and output return loss for the splitter. As is possible to see, the divider shows a very large band. This behaviour, differently of classical $\lambda/4$ architecture, is achieved by the lumped component approach. The input return loss is better than -13dB for all the simulated band. The output return loss is still improved with -15 dB. In the interest band: 57-67 GHz the values have been optimized with a maximum amount around -21 dB for all reflection coefficients.

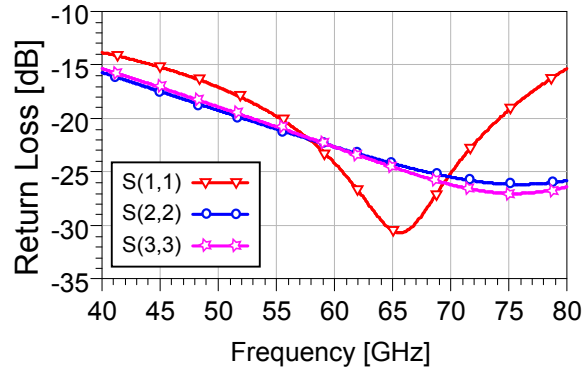


Fig. 6. Lumped Wilkinson splitter input and output return loss.

Concerning the transmission values, the losses showed in figure ?? are lower than 0.5dB within the whole band of interest. The isolation instead was optimized by a transformation of the output shunt resistance. Theoretically the requested value is 100 Ohm resistance but, to allow the maximum isolation value in the center of the band of interest. A R-C circuit has been developed. The optimum value for the R-C net is a series of R-C-R with two 27 Ohm resistance and one 50 fF capacitance. Thanks to this combination, the maximum isolation value is placed in the center of band (-25 dB) with a minimum value of -20 dB around 50-70 GHz. As shown in Figure ??.

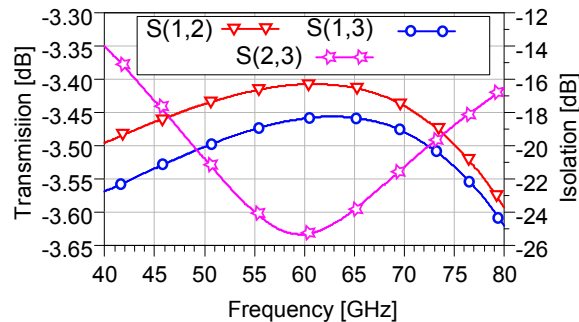


Fig. 7. Principal passive blocks (highlighted in red) for a full balanced I/Q receiver in 60 GHz application.

The synthesized splitter shows a good behaviour. Comparing to the state of the art presented in [?] the Wilkinson divider proposed in this paper has better performance combining with a size of $115 \times 50 \mu\text{m}^2$: 15 times smaller than the reference ($536 \times 150 \mu\text{m}^2$).

VI. CONCLUSION

In this paper an optimized version of lumped Wilkinson power splitter is showed. The main work is based on the characterization of the boundary condition of the structure. The influence of the dummies, the parasitic coupling and a new circuit to increase the isolation have been analysed and developed. The performances of the structure have been simulated. Previous experience in our research group [?] [?] [?] the inductance design and measurement confirms the quality of the simulation as well as the behaviour of the designed structures. The obtained result shows a excellent behaviour for the splitter that overcome the state of the art in terms of isolation, insertion loss and principally in size.

ACKNOWLEDGMENT

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