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A Wideband Single-balanced Down-mixer for the 60 GHz Band in 65 nm CMOS

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Abstract—This paper presents a single-balanced direct down conversion mixer for the unlicensed 60 GHz band. It is based on a differential pair employing the current bleeding technique. An integrated 60 GHz wideband passive balun allows the use of a single ended local oscillator (LO). The circuit is fabricated using the 65 nm bulk CMOS technology of ST Microelectronics.

The mixer's baseband reaches from DC to 2 GHz. The measured radio frequency (RF) bandwidth exceeds 11 GHz, ranging from 54 GHz to at least 65 GHz. The measured RF, IF (intermediate frequency) and LO port return losses lie below -20 dB, -15 dB and -10 dB, respectively, within this entire band.

A maximum conversion gain of 9.1 dB at 100 MHz from the carrier is achieved, while typical values measured at 1 GHz IF lie around 6 dB throughout the entire band. The mixer delivers these optimum results for LO powers as low as -5 dBm. The output referred 1 dB compression point reaches -5 dBm for -1 dBm of LO power. The simulated single sideband (SSB) noise figure is of 9 dB.

Including the differential IF buffer that can drive two single-ended 50 Ω loads, the circuit draws 16.8 mA from a 1 V supply. The pad-limited die size is only 0.52 x 0.49 mm².

I. INTRODUCTION

A major research topic in the domain of microwave engineering today is the design of low-power low-cost silicon transceiver front-ends for the unlicensed frequency band around 60 GHz. While the first CMOS circuits for this purpose were designed in a 130 nm technology [1], the use of lower scale CMOS technologies (like 65 nm for the circuit in this paper) with higher unity gain frequencies (f_T , f_{max}) is one way to improve performance. However, the potential advantages are accompanied by drawbacks such as lower supply voltages (and thus decreased linearity), more stringent density rules and scaling of the metal back-end. This has to be taken into account during design.

Furthermore, many early 60 GHz radio frequency integrated circuits (RFICs) employ transmission lines for matching purposes. This often results in large circuit sizes and thus increased cost. The better solution is the use of spiral inductors, as they do not only reduce circuit size, but also improve performance [2], [3].

This paper presents the design and implementation of one of the basic building blocks of a 60 GHz direct conversion receiver: the down-mixer. Different mixer circuits down-converting signals from the 60 GHz band are described in literature, employing a multitude of topologies (cf. to [1],

[4], [5], [6], [7], [8], [9], [10]). Compared to these circuits, the solution discussed in this paper presents a better compromise for integrated low-cost low-power receivers operating in the 60 GHz band by achieving excellent performance while maintaining small size, low LO power requirements and a low power consumption (cf. section IV). The characterization of the circuit is facilitated by an integrated passive balun and a differential IF output buffer.

II. MIXER DESIGN

Fig. 1 illustrates the block diagram of the designed mixer. The RF input port is single-ended, because the preceding circuit block is going to be the single-ended low noise amplifier presented in [11]. The differential intermediate frequency (IF) output of the mixer is connected to a buffer amplifier based on a differential pair. The IF buffer is designed to drive a differential 100 Ω load (or alternatively two grounded 50 Ω terminations). The total circuit's power consumption is dominated by this buffer, which dissipates around 14 mW. In an integrated receiver circuit, this power-wasting buffer is not necessary because higher load impedances can be employed. The differential local oscillator (LO) port of the mixer core is connected to a passive on-chip balun. The balun is composed of two symmetrical spiral transformers connected as indicated in Fig. 1. Its layout can be identified in Fig. 3, where the balun is connected to the LO pad by an inductor that resonates

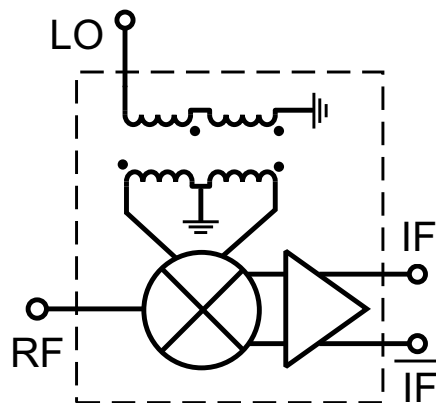


Fig. 1. Block diagram of the downconversion mixer with integrated balun and IF buffer

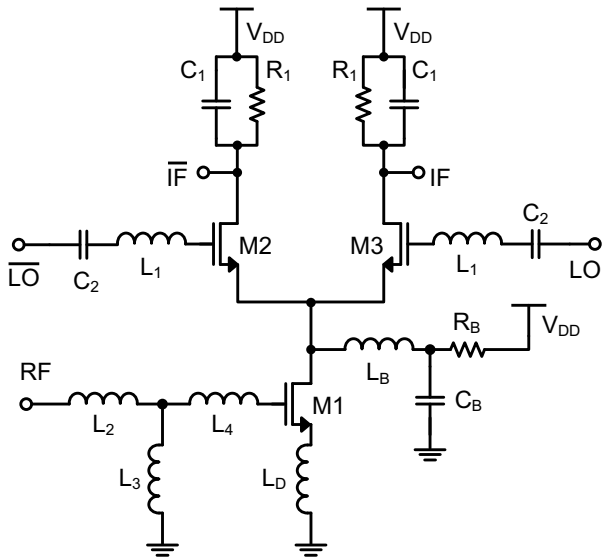


Fig. 2. Simplified schematic of the mixer core without biasing details

the pad capacitance. The employed balun topology allows a much better amplitude and phase balance compared to a single transformer with center tap. For further details on the balun design refer to [10].

Fig. 2 illustrates the schematic of the mixer core. A current bleeding [12] approach is employed to permit ideal biasing of both transconductance (M1) and switching (M2, M3) transistors. The current which by-passes the switching pair is determined by the resistor R_B . It passes by the inductance L_B , which at the same time resonates the parasitic capacitances present at the drain of M1 [4].

The transistor M1 is biased at the minimum noise current density of $0.15 \text{ mA}/\mu\text{m}$. Its width is $14 \times 1 \mu\text{m}$. M1 is degenerated by the inductor L_D . This improves linearity and allows a simultaneous noise and power match. Inductors L_2 , L_3 and L_4 realize this match (taking into account also the pad capacitance) over a wide bandwidth.

Transistors M2 and M3, which are $35 \times 1 \mu\text{m}$ wide, are biased at very low current densities to allow fast switching. The resistive loads R_1 are short-circuited by C_1 for RF and LO frequencies to increase conversion gain G_C and improve isolation. The inductor L_1 is used to match the gates of the switching pair to the balun's impedance. The capacitor C_2 is inserted to cut the DC path and permit a bias voltage at the gates of M1 and M2.

A. Transistors

The transistors used in the mixer circuit are general purpose (GP) devices. GP devices exhibit higher f_{max} as low power (LP) devices at a given bias current, thus mandating their use for low power RFIC design. A consequence of the use of GP transistors is the lower breakdown voltage of 1 V, which limits the circuit's supply voltage.

While the intrinsic performance of the transistors is well represented by the BSIM4 model, it does not take into account

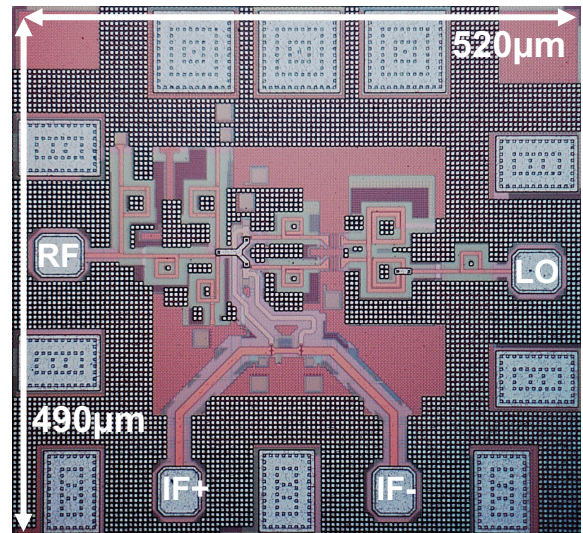


Fig. 3. Die photo of the fabricated down-mixer

the custom layout. To obtain an extrinsic model that includes the optimized multi-finger layout used, a parasitic extraction is performed for all devices.

B. Passive Devices

As inductive matching elements, spiral inductors are used rather than transmission lines. Their performance with respect to size, realizable values and quality factor are superior even when using CMOS technologies with low resistivity substrates [3].

The design of the spiral inductors is lined out in [2]. The focus lies on minimizing the parasitics rather than maximizing the quality factor. Electromagnetic simulations using Sonnet are employed to do quantitative optimizations [2]. The S-parameters obtained by simulation of the final geometry are used to parametrize a $2-\pi$ model, which is employed in the circuit simulations to precisely predict the inductor's behavior. A similar approach is employed for the balun [10].

C. Fabricated Circuit

The presented circuit was fabricated in the 65 nm CMOS technology of STMicroelectronics with two thick copper metal layers. Fig. 3 shows a photo of the fabricated circuit. A very small, pad limited die size of only $0.49 \text{ mm} \times 0.52 \text{ mm} = 0.255 \text{ mm}^2$ is obtained, which is further reduced when integrating the mixer into the receiver.

III. RESULTS

The mixer circuit of Fig. 3 is measured on-wafer up to 65 GHz. The return loss is determined using an Anritsu ME7808A vector network analyzer (VNA). The LO signal is generated by an Agilent E8257D source that provides up to 14 dBm output power at 60 GHz.

Power conversion gain and power sweep measurements are done using the VNA as RF signal source and connecting

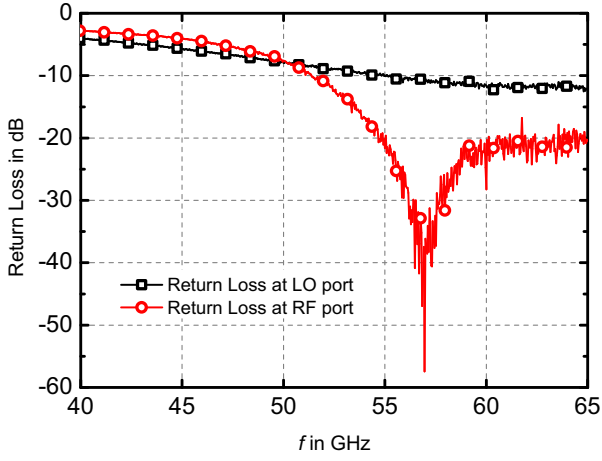


Fig. 4. Measured return loss at LO and RF port

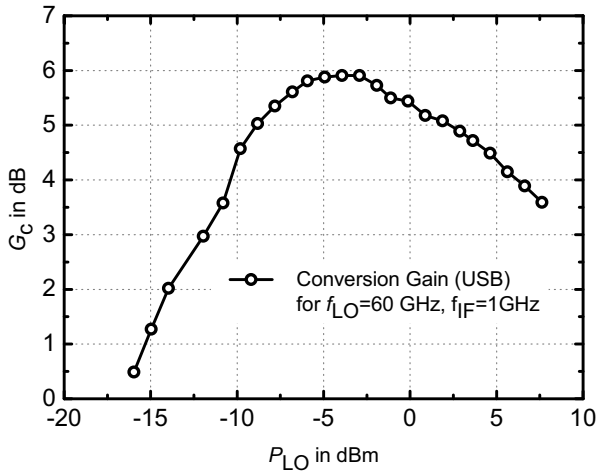


Fig. 5. Measured conversion gain versus LO power at $f_{LO} = 60$ GHz and $f_{IF} = 1$ GHz from the upper sideband

a Rohde & Schwarz FSU 67 GHz spectrum analyzer to one of the IF ports, while terminating the other one. All loss originating from cables and probes are subtracted from the obtained results, and 3 dB are added to the IF output power to account for the differential signal.

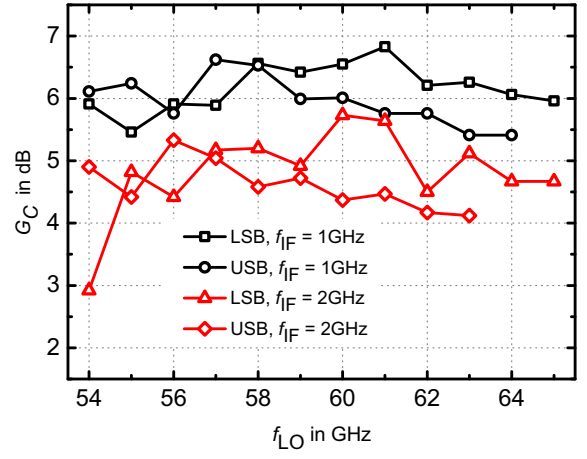


Fig. 6. Conversion gain G_C versus LO frequency for two different intermediate frequencies, both in upper (USB) and lower sideband (LSB).

While measuring, the mixer is biased at the current densities determined during design. The bias of the switching pair depends on the LO power and is set to 0.7 V for the LO power sweep. For the other measurements, P_{LO} equals -1 dBm and the switching pair is biased at 0.56 V. The circuit including buffers is drawing 16.8 mA from a 1 V supply, from which only 2.8 mA are attributed to the mixer core.

Fig. 4 illustrates the measured return loss (RL) at the RF and LO ports. An excellent broadband match is assured, contributing to a very flat, wideband response of the mixer. The measured IF RL stays below -15 dB up to 5 GHz.

The LO power is swept for $f_{LO} = 60$ GHz and $f_{RF} = 61$ GHz to find the value that achieves maximum conversion gain G_C . According to Fig. 5, this is the case at the low LO power value of -5 dBm.

Fig. 6 plots the conversion gain G_C in the lower (LSB) and upper sideband (USB). A very flat, wideband response can be observed for IF frequencies of 1 GHz and 2 GHz, while both sidebands are very symmetric. The conversion gain is around 6 dB at 1 GHz from the carrier over the whole band. The measurement frequency range was bounded to below 65 GHz due to the used equipment.

Fig. 7 shows the conversion gain for five fixed LO frequencies

TABLE I
COMPARISON OF PUBLISHED 60 GHz DOWN-CONVERSION MIXERS IN CMOS

Reference	Topology	Technology (nm)	IF (GHz)	RF (GHz)	G_c (dB)	NF (SSB) (dB)	P_{LO} (dBm)	OP_{-1dB} (dBm)	P_{diss} (mW)	Die Size (mm ²)
Emami et al., 2005 [1]	single gate	130	2	55-61	-2	11.5	0	-5.5	2.4	1.6x1.7
Razavi, 2006 [4]	half Gilbert cell	130	N.A.	60	12	18*	N.A.	N.A.	0.9	N.A.
Tsai et al., 2007 [5]	Gilbert cell	90	0.01	25-75	3 ± 2	N.A.	6	-4	93	0.55x0.55
Zhang et al., 2007 [6]	Gilbert cell	130	1	55-63	3	N.A.	0	-12	N.A.	0.9x0.9
Kantanen et al., 2008 [7]	resistive	90	0.4	60	9.8	N.A.	5	-2	14	1.1x0.7
Kim et al., 2009 [8]	half Gilbert cell	130	5	60	4.9	N.A.	N.A.	-15	8.2	N.A.
Sakian et al., 2009 [9]	Gilbert cell	65	0 - 1.3	60	4	12	N.A.	-16**	6	N.A.
Ercoli et al., 2010 [13]	passive	65	N.A.	50-70*	-6.9*	11.4*	-5*	N.A.	15*	N.A.
this work	half Gilbert cell	65	0-2	54 - 65	9.1	12*	-5	-5	16.8	0.49x0.52

*simulated; **obtained from OIP3-10 dB # voltage conversion gain;

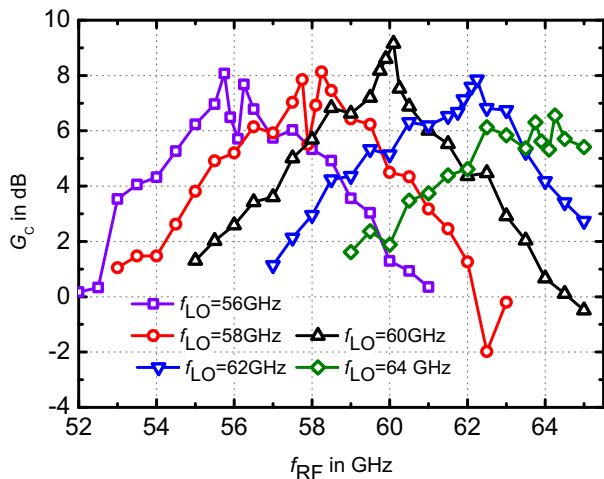


Fig. 7. Conversion gain G_C versus f_{RF} for different LO frequencies. The IF is varying from 100 MHz to 5 GHz.

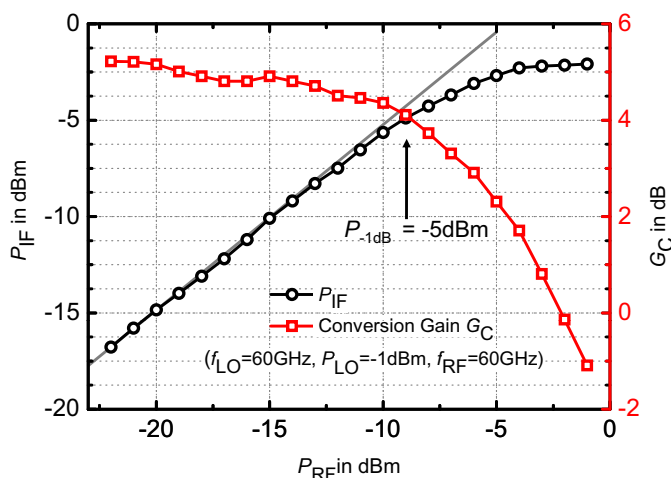


Fig. 8. P_{IF} and G_C versus P_{RF} to illustrate nonlinearity and 1 dB compression point

while sweeping the RF over both sidebands. The peak in G_C is achieved close to the carrier, while the 3 dB IF bandwidth is around 2 GHz (i.e. 4 GHz of band around the LO frequency). Fig. 8 plots IF output power and conversion gain versus input power to illustrate the linearity of the circuit. An output referred 1 dB compression point OP_{-1dB} of -5 dBm is obtained for $P_{LO} = -1$ dBm.

Isolation is less important for this mixer, due to the distance from baseband to LO/RF which allows inexpensive low pass filtering on-chip. LO to IF isolation is observed to be around 30 dB, while RF to IF isolation is around 28 dB. The former value is expected to increase if an integrated differential oscillator with even better phase balance provides the LO signal.

The simulation of the Noise Figure (NF) using SPECTRE RF shows a double sideband (DSB) value of around 9 dB, which gives a theoretical SSB value that lies at 12 dB. Measurement results are expected to be very close due to the use of BSIM4

models and the fact that all parasitics are taken into account during simulation.

IV. COMPARISON TO THE STATE OF THE ART

Table I compares the presented work to 60 GHz CMOS mixers found in literature. The proposed mixer has the smallest chip size, one of the highest gain values and a very wide IF and RF bandwidth that makes it one of the best candidates for an integrated receiver covering the worldwide available 60 GHz band. The fact that its DC power consumption is relatively high originates from the IF buffers that drive two 50Ω loads. Yet, the proposed mixer requires the lowest LO power.

V. CONCLUSION

The single balanced down-mixer presented in this paper is the perfect choice for low-cost low-power direct conversion receivers due to its conversion gain of up to 9.2 dB, its low LO power requirement of -5 dBm, its moderate DSB noise figure of 12 dB and its high OP_{-1dB} of -5 dBm. Its ultra-wide bandwidth respects the channel requirement of all standards that exist for the unlicensed 60 GHz band. The very small (pad-limited) size of only $0.49 \times 0.52 \text{ mm}^2$ allows low cost integration.

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