A Dual-gate 60GHz Direct Up-conversion Mixer with Active IF Balun in 65nm CMOS

Michael Kraemer, Daniela Dragomirescu, Robert Plana

A Dual-gate 60 GHz Direct Up-conversion Mixer with Active IF Balun in 65 nm CMOS

Michael Kraemer[1,2], Daniela Dragomirescu[1,2], and Robert Plana[1,2]

[1] CNRS; LAAS; 7 avenue du colonel Roche, F-31077 Toulouse, France

[2] Université de Toulouse; UPS, INSA, INP, ISAE; LAAS; F-31077 Toulouse, France

E-mail: mkraemer@laas.fr, daniela@laas.fr, plana@laas.fr

Introduction

In the effort of building high performance CMOS millimeter-wave front-ends for the unlicensed frequency band between 57 GHz and 66 GHz, the mixer design is an essential step. When research on 60 GHz CMOS circuits started, it focused on demonstrating receiver front-ends. Thus, down-conversion mixers were in the center of interest. Meanwhile, fully integrated transceivers are designed, fostering the research on up-conversion mixers, where noise figure is less and linearity more of an issue.

A multitude of up-conversion mixers in CMOS technology have been published recently (e.g. [1], [2], [3], [4] and [5]). They mostly use the double-balanced Gilbert cell to achieve high conversion gain and good LO and IF rejection. This paper presents a mixer using a balanced dual-gate [6] topology for the use in low-power direct conversion transmitters. While being demonstrated for simple unbalanced up-converters in the 60 GHz band (e.g. [7]), to the knowledge of the authors this architecture has never been used in CMOS up-conversion mixers for the 60 GHz band.

A passif integrated balun allows to deal with a single-ended local oscillator (LO) signal. Buffer amplifiers for the intermediate frequency (IF), radio frequency (RF) and LO signals are implemented. The IF buffer comprises an active balun to enable mixer characterization by a single-ended IF signal. The implementation is done in a 65 nm bulk CMOS technology.

The mixer's IF band ranges from DC to around 3 GHz, while the RF output lies inside the unlicensed 60 GHz band. The total power consumption, including IF, RF and LO buffers is 23 mW, while the mixer core is consuming only 3 mW. When a 6 dBm 65 GHz LO signal is applied, the maximum conversion gain for an IF frequency of 1 GHz is -2.4 dB. The input-referred 1 dB compression point and 3rd order intermodulation point are measured to be -13.5 dBm and -4.8 dBm, respectively. Even for LO powers as low as -5 dBm a conversion gain around -10 dB can be realized, while the nonlinearity does not increase considerably.

Mixer Design

Preliminary Considerations The requirements on the up-conversion mixer are low-power consumption (and thus, to obtain a low overall transceiver power consumption, also low required LO power), good linearity and low conversion loss. Its IF bandwidth has to exceed the channel bandwidth defined by the 60 GHz standards (i.e. from DC to around 1 GHz, because IF bandwidth is doubled due to direct up-conversion). The RF bandwidth should cover the whole unlicensed band from 57 GHz to 66 GHz.

Furthermore, LO and RF rejection is an important issue. While the optimum solution is a fully balanced topology like the Gilbert cell, it uses at least six transistors and thus becomes quite complex.

A possible solution using only four transistors is the double balanced dual gate mixer proposed in this paper (cf. Fig. 1): It uses a *differential* LO signal to convert a *differential* IF signal to a *single-ended* RF output. Thanks to the addition of the two branches containing the positive and negative LO and IF signals, respectively, both IF and LO signals are rejected at the output node. Only the up-converted signal adds at the RF output. The fact that this output is not differential is desired for a low power, high performance transmitter with single-ended power amplifier.

Overview of the Mixer Test Circuit The mixer core is given in Fig. 1, its function is discussed in the following subsection. The block diagram of the complete mixer circuit is given in Fig. 2. The RF output signal is amplified and matched to a 50 Ω load by a singe stage common source buffer amplifier.

The single-ended LO input is connected to a transformer balun, which is implemented in the top-most copper metal layers in the form of two vertically stacked spiral inductors. Unfortunately, the resulting signal exhibits a certain phase and amplitude-imbalance which impacts the LO-to-RF isolation of the mixer test circuit. The balanced LO signal is amplified by a differential common source stage which improves common mode rejection. Its output is matched to the mixer's LO input.

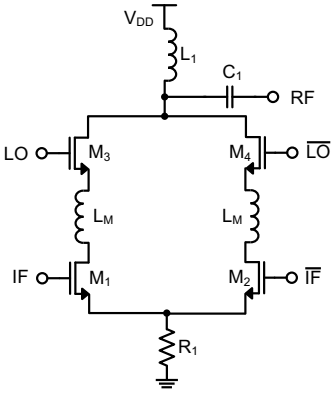


Figure 1: Schematic of the dual-gate mixer core (without biasing)

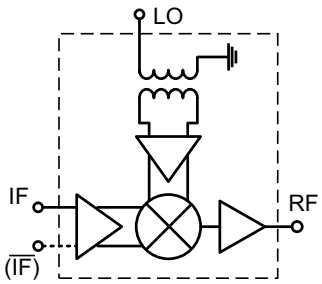


Figure 2: Mixer surrounded by IF, LO and RF buffers/baluns.

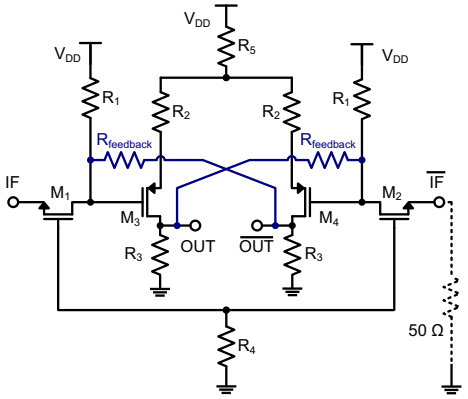


Figure 3: Simplified schematic of the IF buffer / active balun

The IF input of the mixer core requires a well balanced differential signal. The two-stage IF buffer presented below generates this signal from a single-ended input. If a balanced IF input signal is available, the IF buffer acts as a differential amplifier.

Dual-Gate Double-Balanced Mixer Core The schematic of the mixer core is given in Fig. 1. As in [6], rather than using a single dual-gate MOSFET with constant width, a cascode connection of two transistors is employed. The advantage of this approach is that different widths for the lower (here $W_{1,2} = 50\,\mu\text{m}$) and upper (here $W_{3,4} = 26\,\mu\text{m}$) transistors can be chosen to optimize their bias current. Furthermore, a middle inductor with $L_\text{M} = 87\,\text{pH}$ is used to create an artificial broadband transmission line together with the parasitic capacitances of the MOSFETs to improve millimeter-wave performance.
The principle of operation of a dual gate mixer is quite different from the one of a Gilbert cell [6]: Rather than switching the IF current from one branch of the mixer to the other one, the potential at the source nodes of transistors M_3 and M_4 follows the LO signal. Since the transconductances of M_1 and M_2 change according to their drain-source voltage, their drain current is modulated, and thus the mixing takes place. In order to well exploit this effect, transistors M_1 and M_2 need to be biased in the linear region, while transistors M_3 and M_4 work in saturation.
The resistor R_1 increases the common mode rejection of the differential input signals. The inductor $L_1 = 43\,\text{pH}$ and the capacitor $C_1 = 67.5\,\text{fF}$ match the mixer output to the gate of the MOSFET of the subsequent common source buffer. Note that all the inductors used are lumped spiral inductors designed according to [8], due to their higher Q factor and lower occupied area compared to transmission lines.

The IF Buffer with Active Balun A novel IF buffer stage is shown in Fig. 3. It is based on a two stage broadband differential amplifier with common mode rejection realized by resistors R_4 and R_5. The input stage is a common gate amplifier, whose transistors M_1 and M_2 are sized in order to exhibit an input impedance of $50\,\Omega$ over a large bandwidth. The second stage is a common source amplifier based on p-channel MOSFET transistors with degeneration resistors R_2 to improve linearity.
In order to improve common mode rejection up to a point where the buffer can be used as an active balun (second input matched to $50\,\Omega$ as indicated in Fig. 3), cross-feedback is introduced from the output of the second stage of one branch to the input of the second stage of the other branch by the resistors R_feedback. Because the second stage inverts the signal, this measure helps to balance the outputs of the IF buffer.
Throughout the entire IF amplifier stage no coupling capacitor is used. This allows a response down to DC, however implies that the output of one stage has to bias the transistor of the subsequent stage. This is also true for the interface between IF buffer and mixer core. As consequence the value of the employed resistors have to satisfy both bias (low gate voltages at the IF buffer's transistors in order to decrease channel length modulation and increase gain) and AC behavior requirements.

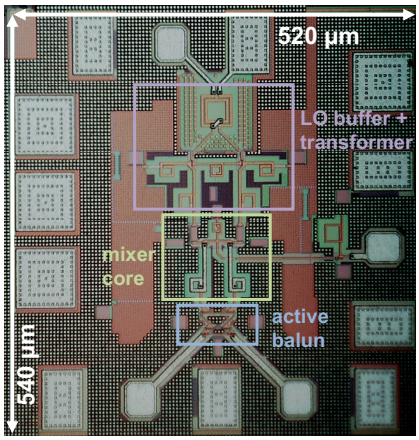


Figure 4: Die photograph of mixer circuit, size pad-limited

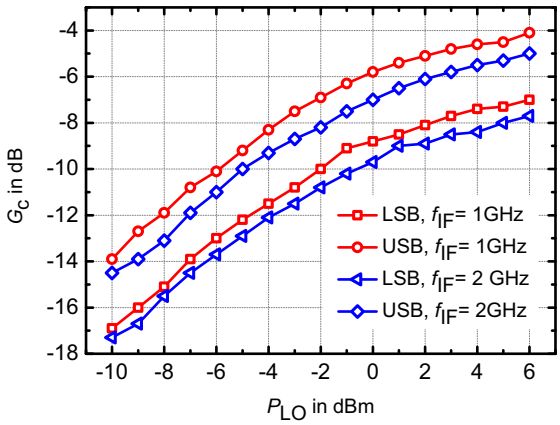


Figure 5: Conversion Gain versus LO power for two IF frequencies with $f_{\mathrm{LO}} = 62\,\mathrm{GHz}$ and $P_{\mathrm{IF}} = -20\,\mathrm{dBm}$.

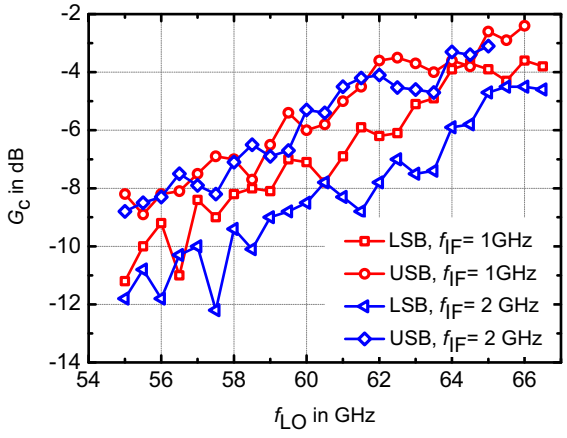
Measurement Results

The mixer circuit described above was fabricated using the 65 nm CMOS technology of ST Microelectronics. Its die photo is given in Fig. 4. The circuit draws 23 mA from a 1 V supply, including the active balun as well as RF and LO buffers. The mixer core's power consumption is estimated to be 3 mW.

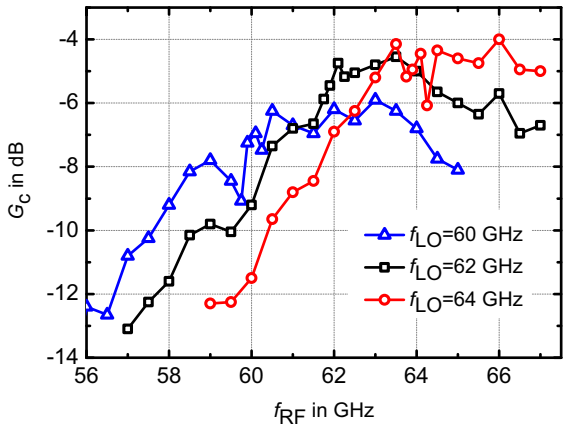
The mixer is measured on-wafer using Picoprobes, a Rohde & Schwarz FSU 67 GHz spectrum analyzer, an Agilent E8257D PSG 70 GHz synthesizer which delivers up to 14 dBm output power at 60 GHz and an Anritsu synthesizer to generate the baseband signal. The connections are made using V-type coaxial cables. The over-all loss in both the RF and the LO path is each about 8 dB, the IF loss is 0.5 dB at 1 GHz. The presented results are corrected by these values if not mentioned otherwise.

Fig. 5 shows the conversion gain G_c achieved for different LO power levels at an LO frequency of 62 GHz. The IF frequencies are 1 GHz and 2 GHz, respectively. Results for both the lower side-band (LSB) and the upper side-band (USB) are plotted. The maximum measured conversion gain is -4.1 dB at f_{IF} = 1 GHz (-5.0 dB at $f_{\mathrm{IF}} = 2\,\mathrm{GHz}$) for an LO power of 6 dBm at the LO port of the mixer chip. An asymmetry between the LSB and the USB can be observed which is both due to the frequency response of the RF buffer stage and the phase imbalance of the differential inputs.

The results presented in Figure 6 are obtained using an LO power of 6 dBm. Fig. 6(a) shows the conversion gain at different LO frequencies. It can be observed that G_c increases towards higher frequencies and is higher in the USB



(a) Conversion gain versus LO frequency for two different IFs



(b) Conversion gain versus RF for three LO frequencies

Figure 6: Frequency-swept conversion gain measurements using $P_{\mathrm{LO}} = 6\,\mathrm{dBm}$ and $P_{\mathrm{IF}} = -20\,\mathrm{dBm}$

Table 1: Comparison to published up-conversion mixers in CMOS

Ref.	Topology	IF (GHz)	G_c (dB)	P_{LO} (dBm)	P_{diss} (mW)	Die Size (mm^2)
[1]	Gilbert	1-5	-4	-	70	0.36
[2]	resistive	1-5	-13.5	8.7	0	0.47
[3]	Gilbert	0-3.5	-5.6	-	8.6	0.69
[4]	Gilbert	10	-6.5	5	28	≈ 0.5
[5]	Gilbert	1	-2	0	24	0.21
this work	dual-gate	0-3	-4.1	6	23	0.28

than in the LSB. This can be confirmed by Fig. 6(b), which shows that a rather flat response is obtained especially in the USB, and that gain increases towards higher frequencies. An explication for this characteristics can be given by the phase imbalance of the LO signal at the transformer output: Similar to an image reject mixer, one sideband will be enforced (here the USB) and the other weakend (LSB) due to this effect. As the mixer will be driven by a differential on-chip VCO in the transmitter circuit (under fabrication), this effect is expected to disappear in the integrated version. (Note that measurements above 67 GHz were not possible due to the limitations of the spectrum analyzer.)
To characterize the linearity of the mixer, input referred compression (P_{-1dB}) and third order intermodulation (IIP3) points are measured. For P_{LO}= 6 dBm, $P_{-1dB} = -13.5\,\mathrm{dBm}$ and $\mathrm{IIP3} = -4.8\,\mathrm{dBm}$. These values decrease by around 2 dB if an LO power of -5 dBm is used. An LO-to-RF isolation of 22.5 dB is obtained for P_{LO}= 6 dBm. It decreases to 15.4 dB if the LO power is reduced to P_{LO}= -5 dBm.
In Table 1 the presented balanced dual-gate mixer is compared to other 60 GHz up-converters found in literature. It shows that the chosen architecture is a good alternative for applications where a Gilbert cell is to complex and small chip area is desired.

Conclusion and Perspectives

This paper presents a low-power balanced dual-gate direct up-converter for the unlicensed 60 GHz band. To the author's knowledge, the proposed architecture has never been used for a CMOS up-converter working in this band before. The maximum conversion gain achieved by the fabricated test circuit for $P_{LO} = 6\,\mathrm{dBm}$, $f_{LO} = 62\,\mathrm{GHz}$ and $f_{IF} = 1\,\mathrm{GHz}$ is -2.4 dB.
Furthermore, a novel IF buffer topology with integrated broadband active balun has been proposed. It allows to test the mixer circuit using either a single-ended or differential IF signal.
Future work will include the redesign of the RF buffer's matching networks as well as the direct connection of an on-chip differential VCO. These measures are expected to improve conversion gain and LO-to-IF isolation and lead to a better symmetry between upper and lower sidebands.

References

[1] S.P. Voinigescu, S.T. Nicolson, et al. CMOS SOCs at 100 GHz: system architectures, device characterization, and IC design examples. In *IEEE ISCAS 2007*, pages 1971–1974, 27-30 May 2007.

[2] M. Varonen, M. Karkkainen, and K.A.I. Halonen. V-band balanced resistive mixer in 65-nm CMOS. *33rd ESSCIRC 2007*, pages 360–363, September 2007.

[3] Min-Chiao Chen, Huan-Sheng Chen, et al. A CMOS up-conversion mixer with wide IF bandwidth for 60-GHz applications. *IEEE SiRF 2009*, pages 1–4, January 2009.

[4] A. Valdes-Garcia, S. Reynolds, and J.-O. Plouchart. 60 GHz transmitter circuits in 65nm CMOS. In *IEEE RFIC 2008*, pages 641–644, April 2008.

[5] F. Zhang, E. Skafidas, and W. Shieh. 60 GHz double-balanced up-conversion mixer on 130 nm CMOS technology. *Electronics Letters*, 44(10):633–634, May 2008.

[6] A. Verma, K.K. O, and J. Lin. A low-power up-conversion CMOS mixer for 22-29-GHz ultra-wideband applications. *IEEE Transactions on Microwave Theory and Techniques*, 54(8):3295–3300, August 2006.

[7] H.C. Kuo, C.Y. Yang, et al. Design of a 60-GHz down-converting dual-gate mixer in 130-nm CMOS technology. *EuMC, 2009*, pages 405–408, October 2009.

[8] M. Kraemer, D. Dragomirescu, and R. Plana. Accurate electromagnetic simulation and measurement of millimeter-wave inductors in bulk CMOS technology. *IEEE SiRF 2010*, January 2010.