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To cite this version:

Nicolas Delaunay, Nathalie Deltimple, Eric Kerherve, Didier Belot. A RF Transmitter Linearized Using Cartesian Feedback in CMOS 65nm for UMTS Standard. RWW2011, Jan 2011, Glendale, United States. pp.49, 10.1109/PAWR.2011.5725376 . hal-00586818

HAL Id: hal-00586818

https://hal.science/hal-00586818v1

Submitted on 18 Apr 2011

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A RF Transmitter Linearized Using Cartesian Feedback in CMOS 65nm for UMTS Standard

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***Abstract*— A fully CMOS transmitter including a power amplifier (PA) using a Cartesian Feedback (CFB) technique is presented. This system aims at improving the linearity of the transmitter, designed in 65nm CMOS technology from STMicroelectronics, essentially the power amplifier linearity. This transmitter delivers a maximum output power of 23dBm. Thanks to this linearization technique, the ACPR has been improved by 22dB at 5MHz from the carrier.**

***Index Terms*— Linearization techniques, Power Amplifier, CMOS technology, Wireless communication.**

I. Introduction

Nowadays, abundant research focuses on the improvement of power amplifier's linearity performances [1]; [5-9]. Linearization techniques remain an important and hot domain of research with UMTS (Universal Mobile Telecommunications System) standards [2] and the future 4G standards called LTE (Long Term Evolution). These standards have been created for high data rate wireless communications and use a non-constant envelope modulation like HSPK (Hybrid Phase Shift Keying) for UMTS. As a consequence, both linearity and efficiency in the design of a cellular PA are becoming harder to maintain. A useful parameter to observe the complexity of a modulation is the PAPR (Power Average to Peak Ratio) – also called PAR (Peak Average Ratio). The PAPR of GSM, UMTS, and LTE are 3dB, 3.5-7dB, and 5-8.5dB respectively. Hence, designing a linear and efficient PA is a difficult task regarding to the PAPR value.

In the past years, a lot of solutions have been proposed to improve PA performances. These solutions can be divided into two purposes: the first ones, such as Envelope Elimination and Restoration (EER) [3], Envelope Tracking (ET) [4], improve the PA efficiency; while the others improves its linearity: Indeed, the power amplifier is one of the most critical component and a major source of distortion for a transmitter. These techniques mainly work on the signal and not on the power amplifier, as pre-distortion (analog, digital or both) [5], feedforward, Cartesian Feedback [6] etc. Despite the excellent results of these techniques on the linearity, studies to integrate such methods on Silicon remain very recent [7].

We propose to apply Cartesian feedback technique on an integrated transmitter in a 65nm CMOS technology from STMicroelectronics. This linearization technique has already been realized with discrete components or III-V technology for base-station [8], [9], but for the best of our knowledge, a CMOS transmitter using CFB has not been reported in the literature for mobile handset. Thus, main challenges are to realize a single chip on 65nm CMOS technology and to increase performances of the transmitter for UMTS standard communication.

Section 2 describes the Cartesian Feedback architecture with its advantages and precautions to take into account. Each building block has been designed in a CMOS 65nm technology and measurement results are given. Section 3 presents the system level behavior of the overall architecture.

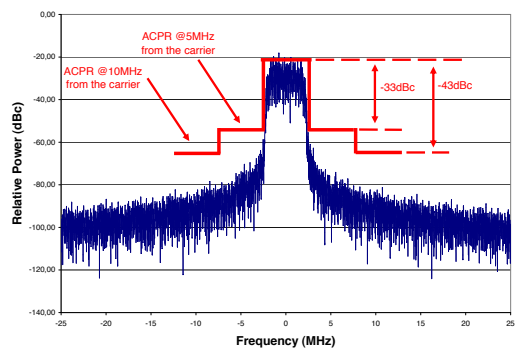

Fig. 1. Mask of UMTS standard

II. Transmitter Architecture

The trend of these last years is to reduce the transmitter area and so its cost. To achieve this goal, CMOS integrated transmitter with thick gate transistors are developed, making harder the design of power amplifiers with a high output power. This has a direct consequence on the linearity of a transmitter, which is actually a major preoccupation for the research domain. This non-linearity affects transmission results and adds distortion on the adjacent channels. With new wireless communication standards, the power amplifier has to deliver always more output power with a widen bandwidth. For example, the bandwidth of the channel for GSM, UMTS and LTE communications is 200 KHz, 5 MHz, and 20 MHz respectively. The Fig. 1

shows the spectral mask defined by the standards UMTS and a signal WCDMA associated.

Solutions must be developped to match this mask and fight against the difficulty of designing both linear and efficient transmitters. The proposed solution is to integrate a Cartesian Feedback loop on Silicon 65nm CMOS.

A. Improvement of the Linearity using a Cartesian Feedback Loop

A RF transmitter is typically composed by several components such as filters, IQ modulators, mixers, local oscillators, power amplifier and an antenna. As we can see on the Fig. 2, analog baseband signals fed the IQ modulator, and then up-converted to a RF frequency by mixers associated with a local oscillator. Finally, the resulting RF signal is strengthened by the power amplifier before driving the antenna.

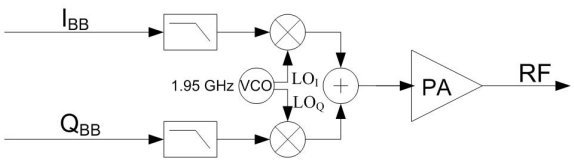

Fig. 2. Zero-IF Architecture

In a context of non-constant envelope modulation as HPSK for UMTS, precautions to design and not degrade the signal have to be taken in account. Indeed when the transmitter works close to the compression point (non linear area), distortions appear on the signal and can be spectrally observed on adjacent channels. It is therefore advisable to use components most linear as possible to avoid these distortions, and consequently a degradation of the transmitted information. Those are called Adjacent Channel Power Ratio (ACPR, also called, ACLR - Adjacent Channel Leakage Ratio). As it is shown on Fig. 1, ACPR enables to characterize distortions of the transmitter by determining the ratio between the power level of the main and the adjacent channel.

In order to decrease these phenomena we adopt the Cartesian Feedback loop which is a linearization techniques applied to correct the linearity of a transmitter. This choice has important advantages. The most important is the portability; indeed the Cartesian feedback corrects nonlinearities of any type of power amplifier. This system, thantks to the feedback path, works directly on the signal, according to the behavioural changes of the power amplifier (bias, temperature, aging etc.), and the changes related to the PA upstream components of the direct path.

Another major advantage is the possibility to implement the system on a single chip. In order to make the integration easier, and thus reduce the cost of production, some parts of the system can be implemented on

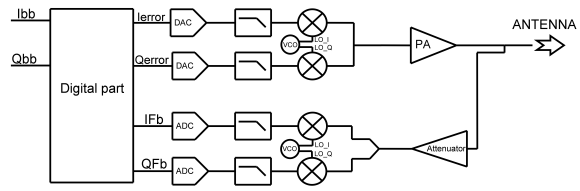

Fig. 3. Architecture of a Cartesian Feedback linearization technique

the digital domain (e.g phase correction). Last but not least, the Cartesian feedback is able to correct not only the amplitude distortions (AM/AM) but also the phase distortions (AM/PM). The main drawback is the stability of the system, a fact that demands the achievement of a carefully study to avoid this problem.

The architecture of the Cartesian feedback is depicted in Figure 3. Like the Zero-IF architecture, the direct path has the same functioning: to send a signal through the antenna. Therefore a feedback path has been added to correct the information from the output of the PA. In fact, this output signal is attenuated and down-converted to baseband domain. The intermodulation products, related to IQ demodulation, are thereupon removed by a low pass filter.

An operation of phase adjustment is applied to I_{FB} and Q_{FB}baseband signals. The aim is to eliminate any rotation of the IQ constellation caused by the nonlinearities from the direct path of the transmitter. Feedback signals are then subtracted from the original signal in order to obtain I_{Error} and Q_{Error}. These signals represent the nonlinearities of the forward path of the system. This means that I_{Error} and Q_{Error} are predistorded signals in amplitude and phase. They will be compensated through distortions added by the direct path, and more accurately, the power amplifier. All delays are corrected by the phase alignment and subtraction opertations. The linearity of the entire system will be improved and transmitted datas as well.

B. Building Blocks Description

The linearized transmitter depicted in Fig. 3 is made up of both analog and digital building blocks. Indeed, as decreasing the cost of production remains an important objective for industry, operations of subtraction and phase alignment were moved in the digital domain. All of the others components (converters, mixers, attenuator, filters, and power amplifier) have been designed in 65nm CMOS technology from STMicroelectronics. All the active circuits have been measured and the results are given in Tab. I.

The power amplifier is the main contributor of nonlinearities. Its design is based on Stacked Folded Differential Structure (SFDS) [10], which is inspired by the push-pull

TABLE I
MEASUREMENT RESULTS OF ANALOG COMPONENTS

Circuits	Architecture	Relevant Measures	Consumption	Core Area
DAC: 12 bits	Current Steering	Bandwidth 80MHz @Fs=242MHz	Analog part: 26mw Digital part: 2.5mW	0.476mm² (with PADs)
Active Filters	Leap Frag 3rd order	Cutoff frequency: 7MHz, Gain: 14dB	14.4mW	0.191mm²
Active Mixer	Gilbert Cell	Gain: 16dB Psat: 10dBm	13.2mW	-
Power Amplifier	Stacked Folded Differential Structure (SFDS)	Gain: 15dB P_{sat}: 23dBm OCP1: 21dBm PAE max: 12%	1.2W	0.672mm²
Attenuator	Capacitive strucutre	Gain: -6dB (simulated)	None	0.006mm²
Passive Mixer	Ring Structure	Gain: -4dB Output Noise: 5nV/$\sqrt{Hz}$ (simulated)	None	72e-6mm²
ADC : 12bits	Parallel Pipeline	Bandwidth: 162MHz @Fs=324MHz	Analog Part: 100mW Digital: 1mW	<0.3mm²

structure. At 1.95 GHz, the power gain of the PA is equal to 15dB. It offers a saturation power of 23dBm with an output compression point (OCP1) of 21dBm. These large signal characteristics fulfil the W-CDMA standard (21dBm at 1.95GHz - Class 4) in terms of output power and operating frequency. General information of this last is resumed on the Tab. I, as other components. Thanks to this table, a 3mm² analog core area can be targeted, consuming 1.51W with 80% coming from the PA.

III. SYSTEM LEVEL BEHAVIOR

All building blocks making the linearized transmitter have been designed in CMOS 65nm technology with cadence spectre RF framework and have been characterized stand-alone. Now, we are able to realize system level simulations in order to validate the overall architecture. The long time expended and the convergence problem made simulations on the transistor level harder, whyfor ADS Software has been used.

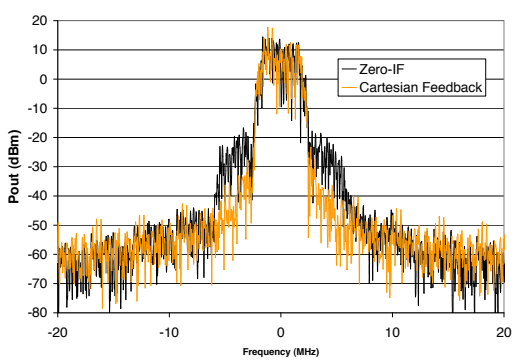

Fig. 4. Output Spectrum with and without CFB

A. Output Spectrum

The complete system exhibits a gain of 45dB and -20dB, respectively, for the forward and the feedback path. Fig. 4 depicts the output spectrum of the PA with and without Cartesian Feedback technique for a same output power. The PA output clearly shows a decrease of the distortions on the adjacent channel due to the forward path. In fact comparing with the mask presented in section II, the output spectrum for a Zero-IF architecture is out of specifications defined for UMTS communications, in opposition with the output spectrum of the Cartesian Feedback.

B. ACPR

The ACPR at 5MHz from the carrier for UMTS standards must to be less than -33dBc, as explained in Section II. To illustrate it, the Fig. 5 shows the evolution of the ACPR according to the output power of the power amplifier.

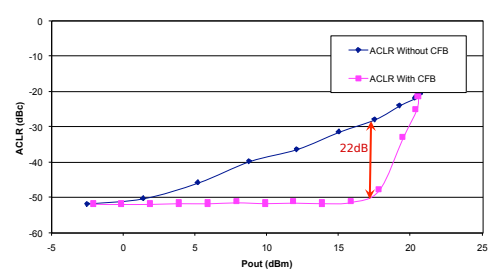

Fig. 5. ACPR at 5 MHz offset for W-CDMA signal in open and closed loop

In open loop mode only the behavior of the forward path is observed, while in closed loop mode linearity correction is applied. As we can notice on this figure, with the open loop for an output power of 12dBm, the ACPR does not respect the UMTS specifications. On the other hand, for the same output power using the Cartesian Feedback, we notice that ACPR respects the specifications and is improved by 22dB at 5MHz from the carrier.

C. Constellations

Another interesting result is the constellation before and after the PA, as shown in Fig. 6. We observe that the EVM (Error Vector Magnitude) at the output of the power amplifier is better than the other one at the input. This confirms our hypothesis explained in Section II-A about the predistortion of the I_{Error} and Q_{Error} baseband signals.

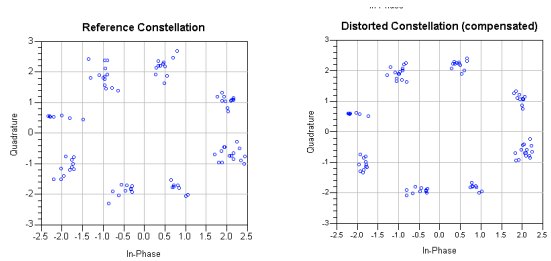

Fig. 6. Constellations for the input and output signal from the PA

D. Comparison with literature

To finish, the Table II presents a comparison of our system with a recent state of the art. As we can see, references [8] and [9] are also using Cartesian feedback correction, whereas the last one [11] uses another technique of correction called Harmonic Injection. For a same PA class operation and a same standard, the improvement of our system is 7dB better than reference [8]. Moreover, this work is a single circuit that offers a compact and cheaper system than the others.

IV. Conclusion

This paper presents the linearization of a RF transmitter by Cartesian feedback technique. It is important to note that all active components of this transmitter have been designed and realized in 65nm CMOS technology from STMicroelectronics. Measurement results gave a maximum output power of 23dBm at 1.95GHz. Their integration on a single chip with this technology remains the main challenge, and we can estimate the size of the core area about 3mm² for a power consumption of 1.5W. The whole single chip transmitter is in foundry.

TABLE II
Comparison with the literature

Ref	[8]	[9]	[11]	This Work
Technology	LDMOSFET (Freescale)	Mini-Circuits	-	65nm CMOS
PA class operation	Class AB	Class A	-	Class AB
Frequency (GHz)	2.14	0.9	1.8	1.95
Standard / Modulation	W-CDMA	16-QAM	Pi/4 - DQPSK	W-CDMA (HPSK)
ACLR improvement	15.3 dB	10dB	15dB	22 dB

Once each building characterized block , system level simulations have been done to observe the ACPR. The ACPR improvement is equal to 22dB at 5MHz from the carrier. System level simulation results demonstrate the feasibility of designing a complete transceiver with CFB technique in a low cost CMOS technology.

With the emergence of multi-standard communication systems, future work is to adapt our system to an all CMOS multi-mode linearized transmitter.

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