Impact of the Physical Layout of High-Current Rectifiers on Current Division and Magnetic Field Using PEEC Method

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Jean-Luc Schanen, *Senior Member, IEEE*, Jean-Michel Guichon, James Roudet, Cyril Domenech, and Luc Meysenc

***Abstract*—This paper addresses some problems linked to the physical layout of high-current rectifiers: paralleling components, magnetic field close to the rectifier, and also the validation of the physical layout at reduced current. Even if the impact of cabling stray inductance is well known, some new tools and methodology are available today to design quicker and safer physical layout of such high-current rectifiers.**

***Index Terms*—Circuit modeling, current distribution, electromagnetic compatibility, electromagnetic fields, power electronics, rectifiers.**

I. Introduction

ELECTROCHEMICAL process of aluminum involves high dc currents provided by high-power rectifier–transformer units (Fig. 1.) [1]. If the global behavior of these rectifiers is well known, the physical layout is still a challenging task for design engineers, since it impacts on several issues simultaneously.

1) Device design normally supposes a good current share between all SCRs of each secondary phase. However, this current division is affected by the devices' intrinsic property (but chips are often selected individually for high-power structures) and also by the layout of the rectifier itself [1]–[4].
2) Devices' cooling must be accounted for when choosing the rectifier layout.
3) The restrictions on magnetic close field in the aluminum plant and also near the rectifier are currently increasing. This field map is obviously linked to the physical layout.

It is worth noting that the price and delays of such heavy realizations do not allow any trial and error method in designing the rectifier layout.

In addition, for such high-current converters, industry rarely provides test facilities, and the rectifier behavior must be validated directly on the aluminum plant, which is always the most exciting point of the business—if all works well! There is thus a strong need of internal validation using smaller currents but allowing an extrapolation to nominal behavior.

In this paper, it will be shown that the use of computer-aided design tools associated with cabling rules can help in proposing high-current rectifier layouts, fulfilling all constraints. In addition, the comparison of simulation results with several tests at reduced current level will permit a first validation of the structure and higher current extrapolation, before final testing in the actual plant.

The main interest of the proposed approach is that it accounts for all stray elements brought by the cabling structure without any approximation. Usually, design rules are deduced from conventional geometries by neglecting coupling coefficients which are usually small in such layout. However, when changing the geometry during the design, this approximation may become false, which could lead to a bad surprise when building the rectifier. This may be all the more important in future automatic design procedures, where the optimization process may converge to a bad solution if a specific phenomenon has not been taken into account.

However, the complete design rules accounting for all the coupling inside the cabling geometry are useless if the impedance matrix of the topology cannot be computed and automatically associated to the electrical equivalent circuit. This is achieved using partial element equivalent circuit (PEEC) method [5]. This electromagnetic modeling directly results in an equivalent circuit composed of resistors, inductors, and coupling. It is particularly well adapted to industrial system with large size and complex 3-D geometries. Contrary to finite element method (FEM), this integral method does not need the meshing of the air, and only the conductors are subdivided. In addition, the computation of the complete impedance matrix using FEM is heavy and necessitates several resolutions using various excitation sources.

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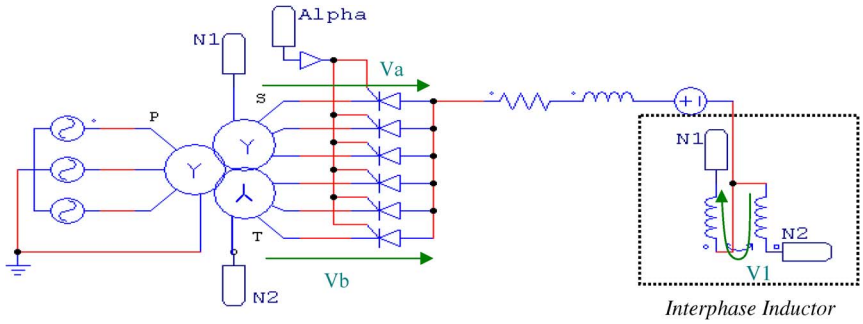

Fig. 1. Basic rectifier topology.

This paper will first investigate paralleling component issues and particularly recall the impact of transformer leakage inductance and layout parasitic. In addition, constraints on the matrix impedance representing the rectifier layout will be established. They may be useful to characterize and even optimize the layout (Section II). Then, close field computation will be addressed (Section III). In Section IV, the example of a 40-kA booster will be proposed to illustrate the methodology.

II. Paralleling Device Issues

The problem of paralleling several devices is well known and has been studied with the beginning of the rectifiers [1]. For high power, the components can be selected individually in order that their characteristics match together. Therefore, potential dissymmetry is due to cabling only. Different impedance between the semiconductors and also mutual couplings initiate dynamic differences between all components [1]–[4]. Still today, even if all the reasons of current imbalance are (or at least, should be) understood, the inverse problem is not easy to solve: how to find the right geometry to provide symmetrical electrical characteristics, even accounting for mutual coefficients? Simulation can provide useful results to achieve this task. Indeed, even a geometrical symmetry does not guarantee symmetrical impedance matrix when accounting for all mutual, as will be shown in Section IV. Approximations proposed in [1] to simplify the computation may become wrong for modern rectifier with high integration ratio.

A first analysis of dynamical effects can be proposed in order to investigate the problem of current division (Fig. 2.). During the commutation from one phase to the other, encroachment phenomenon occurs, mainly due to leakage inductance of the transformer. Global dI/dt of a phase is thus fixed, but the repartition between elementary components in each phase depends on the current divider formed by the cabling stray impedances. Stray impedance and mutual coupling must thus be accounted. It is worth noting from this simple model that all mutual inductance between all conductors have an impact, which is usually neglected in conventional design where all phase legs are designed independently. The higher level of integration will perhaps lead to the necessity of accounting for all mutual couplings during the design, including the other phases of the converter.

Cabling rules, based on the same idea as [1] but without any assumption, have been proposed in [6] and can be adapted here, starting from the equivalent circuit of Fig. 2. To obtain

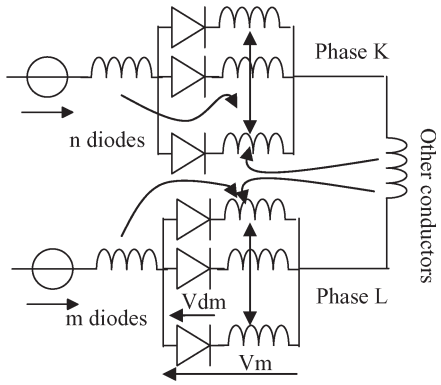

Fig. 2. Equivalent circuit during encroachment (all mutual inductances are not displayed).

synchronized turn on, all diode voltage of the same leg must be similar: this impacts on several mutual values and can be summarized with a simple cabling rule, which must be fulfilled due to the physical layout. Let us call K and L as two phases of the rectifier. Phase K has n diodes and phase L has m (usually, $m = n$, but the formulation is general). At the end of the conduction of phase K, just before phase L is being turned on, all diode voltages of phase L are expressed as a function of all current and impedance parameters

$$\begin{bmatrix} Vd1 \\ Vd2 \\ \vdots \\ Vdm \end{bmatrix}_L = \begin{bmatrix} \ddots & & \iddots \\ & M_{ij} & \\ \iddots & & \ddots \end{bmatrix} \cdot \frac{d}{dt} \begin{bmatrix} I\text{phase} \\ Id1 \\ Id2 \\ \vdots \\ Idn \end{bmatrix}_K . \quad (1)$$

$[M_{ij}]$ represents the mutual inductance matrix between the legs of phase L and all other conductors where current is flowing, including phase K. Iphase is the total current of phase K, and $Id1 \ldots Idn$ are the currents of each diode of phase K.

First, all voltage $Vd1 \ldots Vdm$ must be equal. Second, assuming that the final layout will fulfill all conditions to have balanced currents, it can be supposed that $Idi = I\text{phase}/\text{n}$. Therefore, (1) can be rewritten as

$$\begin{bmatrix} Vd \\ Vd \\ \vdots \\ Vd \end{bmatrix}_L = \begin{bmatrix} \ddots & & \iddots \\ & M_{ij} & \\ \iddots & & \ddots \end{bmatrix} \cdot \begin{bmatrix} 1 \\ 1/n \\ 1/n \\ \vdots \\ 1/n \end{bmatrix} \cdot \frac{dI\text{phase}}{dt}_K . \quad (2)$$

Equation (2) can be expressed as m cabling rules between mutual coefficients of the considered phase and the rest of the structure.

When all diodes are in the ON state, obtaining the same currents necessitates fulfilling another set of rules, including both mutual inductance and stray impedance [6]

$$\begin{bmatrix} Vm \\ Vm \\ \vdots \\ Vm \end{bmatrix}_L = \begin{bmatrix} \ddots & & \iddots \\ & Z_{ij} & \\ \iddots & & \ddots \end{bmatrix} \cdot \frac{d}{dt} \begin{bmatrix} I\text{phase} \\ Id1K \\ \vdots \\ IdnK \\ Id1L \\ \vdots \\ IdmL \end{bmatrix}. \quad (3)$$

Voltages $V1 \ldots Vm$ are the leg voltages of phase m. All paralleled legs have the same voltage. Matrix $[Z_{ij}]$ links these voltages Vm to all currents of the structure: $IdiK$, currents of each leg of phase K; $IdiL$, currents of each leg of phase L; and Iphase, the global current. Assuming that the final layout will allow equal current division, this leads to $IdiK = I\text{phase}/n$, and $IdiL = I\text{phase}/m$. Therefore, (3) can be expressed as

$$\begin{bmatrix} Vm \\ Vm \\ \vdots \\ Vm \end{bmatrix}_L = \begin{bmatrix} \ddots & & \iddots \\ & Z_{ij} & \\ \iddots & & \ddots \end{bmatrix} \cdot \begin{bmatrix} 1 \\ \frac{1}{n} \\ \vdots \\ 1/n \\ 1/m \\ \vdots \\ 1/m \end{bmatrix} \frac{dI\text{phase}}{dt}. \quad (4)$$

The same as (2), (4) corresponds to a set of m conditions on impedance matrix $[Zij]$.

Even if these two sets of cabling rules cannot be used directly to find a proper layout for an inverter, they have been obtained without any assumption and therefore account for all couplings inside the system.

They can be used to qualify a tentative layout, or even in an optimization process, to provide the "best" layout. Such procedures have been validated successfully in other applications [7].

Obtaining the complete impedance matrix of the system—necessary for the extraction of $[Mij]$ and $[Zij]$—starting from the rectifier geometry is quite simple using the PEEC method [5], [8]. This modeling method allows attributing to each part of a circuit a portion of the complete loop inductance. The complete geometry is thus decomposed into several massive segments or bars. Analytical formula can be used to determine all inductance and mutual values, starting from the bar geometry only. To account for frequency effects, each bar can be meshed into elementary conductors. The final impedance matrix results from the association of all segments at desired frequency (Fig. 3).

III. Close Field Magnetic Radiated Emission

This issue has today become more and more of a challenge and must be accounted for by new rectifiers. Indeed, due to high currents circulating in the system, the magnetic field in the vicinity may be huge. Compensating loops are used for the complete plant, but they do not cancel the magnetic field around the rectifier itself. Therefore, people entering into the rectifier area may be exposed to magnetic fields exceeding the maximum allowed values for human health. Even if the effects are not well known, new standards begin to appear, and rectifier manufacturers are strongly encouraged to anticipate this new context. The same problem is encountered, for instance, when building railway substations [9].

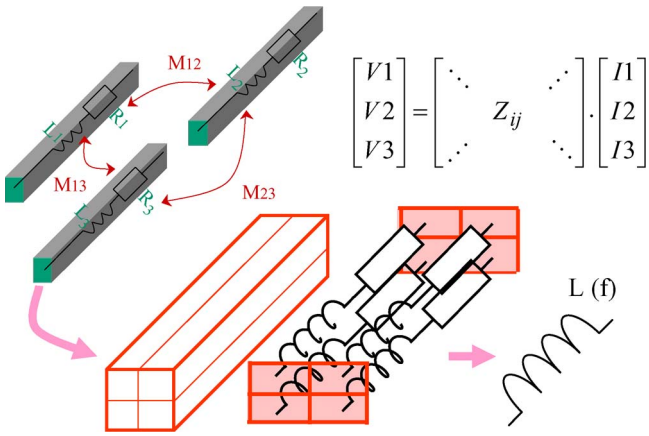

Fig. 3. Illustration of PEEC Method.

Additionally, high magnetic field may disturb all surrounding electronics, particularly the control boards of the SCRs, and all other control equipment. Therefore, the knowledge of the magnetic field will become a key point of rectifier design in the near future.

The main cause of magnetic field shape close to the rectifier is due to cabling geometry. As mentioned in the Introduction, FEM is not adapted for such large problems because it is time and memory consuming. Consequently, PEEC method will be preferred. Obtaining magnetic induction close to the conductors is quite simple using this approach: After modeling, the equivalent circuit is solved at desired frequency. Therefore, all currents in the elementary subdivisions (assumed uniform) are known. Then, Biot–Savard law can be easily used to compute the magnetic field from each subdivision of each part of the circuit since analytical formulation is available for an elementary bar [10].

The magnetic field in all free spaces around the rectifier is thus computed as the vector sum of all contributions of all elementary conductors.

IV. 40-kA Booster Design

To illustrate how modeling can be useful in layout design, we propose here a complete study of a booster, which is usually used in aluminum plant for helping the main rectifiers. In comparison with the main rectifier, the current rating of this booster is low; however, 40 kA is still a challenging design regarding current division. Eight SCRs are used for each leg. Furthermore, since the testing facility is limited to 15 kA, the complete rectifier will not be actually tested before being installed in the actual plant, which makes the simulation particularly interesting.

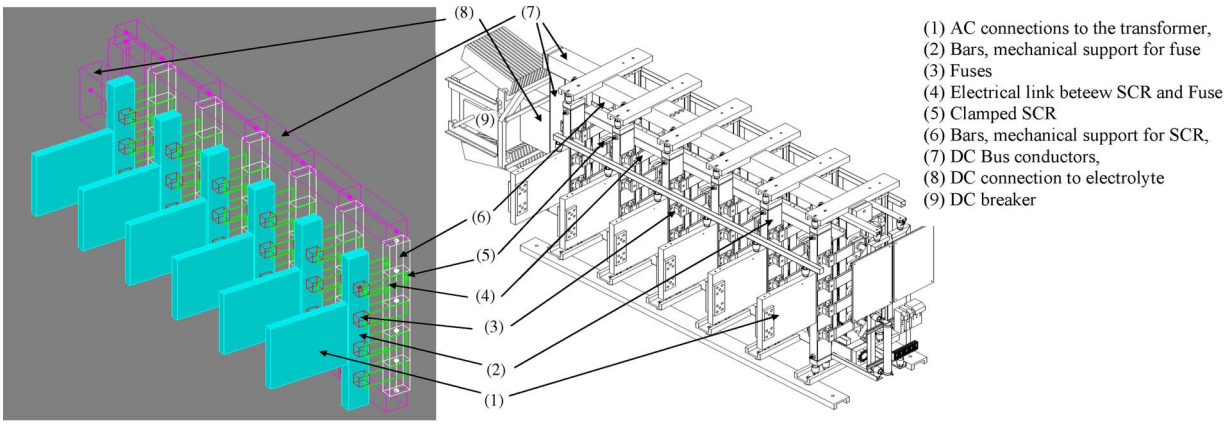

Fig. 4. Physical layout proposal and associated modeling.

A. Rectifier Structure

Fig. 4 shows a layout proposal for rectifier implementation, as well as the electromagnetic modeling using PEEC method [11]. The basic structure is as symmetrical as possible, using a ladder structure (as proposed in [1]). Thermal management is achieved using a simple solution: The mechanical support for the SCR has also the electrical role of interconnection. Furthermore, hollow bars are used, allowing liquid cooling. This allows a homogeneous cooling between all SCRs. In this case, the main cause of any temperature difference is due to the power dissipation and thus, to current imbalance. Electrothermal coupling has not been taken into account in the modeling.

B. Modeling and Simulation

After modeling with PEEC method, an automatic circuit extraction system to a circuit simulator [12] allows obtaining all current waveforms in the components. Precise ON-state characteristics have been taken into account, based on manufacturer datasheets: $V\mathrm{on} = 0.85$ V, $R\mathrm{on} = 89\ \mu\Omega$.

Transformer is also important in the model, since leakage imposes the global current variation speed, as explained in the previous section. Since two secondaries are needed, the equivalent circuit is not obvious. Complete equivalent circuits are available for multiwinding transformers [13], but they necessitate more data than usual datasheets.

The total number of parameters to represent the magnetic coupling of a two-winding transformer would be six, since it corresponds to three coupled inductors. Assuming the two secondaries to be identical, we used the equivalent scheme of Fig. 5. In this simplified scheme, only four independent parameters are needed to represent the magnetic coupling, contrary to the complete representation. Indeed, in the inductance matrix, the two secondary inductances are identical, as well as the two mutual inductances in the primary side. In the scheme of Fig. 5, Lm represents the magnetizing inductance, $L1$ and $L2$ account for the leakage, and η is the no-load transformer ratio.

Identifying all elements necessitates two short-circuit voltages $Ucc1$ and $Ucc2$: 1) $Ucc1$ should have nominal current when secondary 1 is short circuited and 2) $Ucc2$ should have nominal current when both secondaries are short circuited.

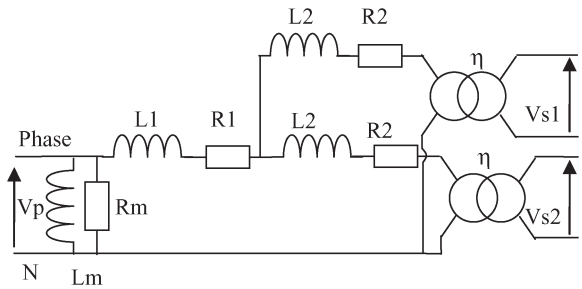

Fig. 5. Equivalent circuit used for one phase (all elements are on the primary side).

Unfortunately, only $Ucc2$ was given in the datasheet. We therefore used the empirical relation between $L1$ and $L2$: $L1/L2 = R1/R2 = 1/4$, which has been validated for various transformers of such power.

The transformer had the following characteristics:

$2 * 2300$ kVA (2300 kVA for each secondary winding);

primary voltage 11 000 V$-$secondary voltages 165 V;

$Ucc2 = 8\%$;

$Pcc2 = 76\,000$ W.

Based on $Ucc2$ and $Pcc2$, we obtained

$$R1 = 0.14\ \Omega \quad L1 = 2.15\ \mathrm{mH}$$
$$R2 = 0.56\ \Omega \quad L2 = 8.6\ \mathrm{mH}.$$

The temporal simulation results allow computing the average and rms current mismatch, and current derating can be checked.

Fig. 6 shows the simulation results for phase 3, with the current division between the eight SCRs for nominal current. The geometrical implantation as well as the SCR numbers is displayed on the top of this figure. The geometrical symmetry has obvious consequences, since SCRs 1 and 4, 2 and 3, 5 and 8, and 6 and 7 have the same behavior. However, it can be noticed that the coupling between phases is important, since SCRs 1 and 5, and 2 and 6 do not carry the same current.

These different temporal waveforms induce different mean and rms values, as illustrated in Table I. The derating is computed with respect to the ideal case, where all SCRs would carry

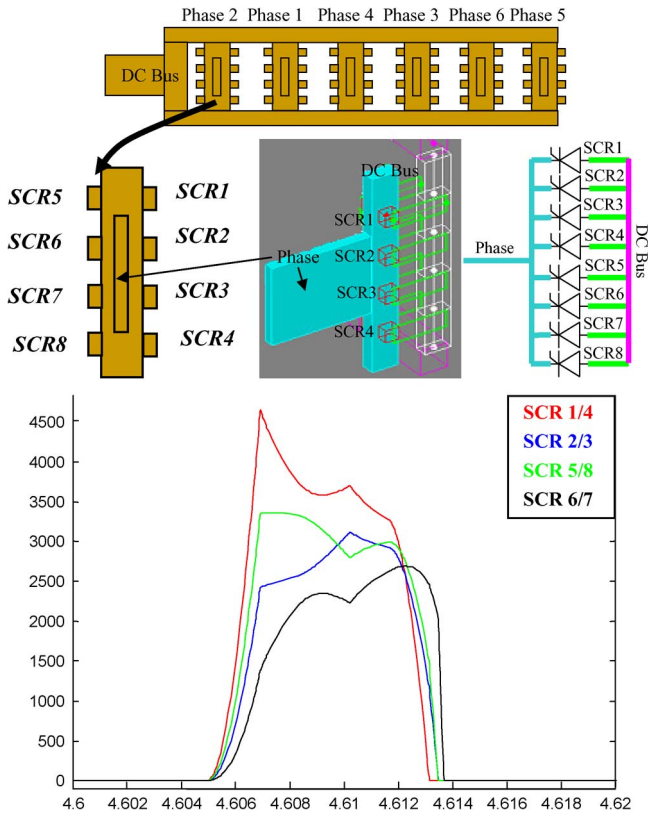

Fig. 6. Top: rectifier structure and SCR reference. Bottom: example of current division among the eight SCRs for phase 3 and a 46-kA current (simulation).

the same current. For a load current of 46 545 A (corresponding to simulation conditions), the reference mean and rms currents can be easily computed, based on the normal behavior of this structure (each secondary sees $Idc/2$ during a third of the period)

$$I\text{avg/SCR} = \frac{46545}{2 \cdot 8} \cdot \frac{1}{3} = 970 \text{ A}$$

$$I\text{rms/SCR} = \frac{46545}{2 \cdot 8} \cdot \frac{1}{\sqrt{3}} = 1680 \text{ A}.$$

The worst case of current division is for phase 2 and phase 1. This can be explained by their position in the rectifier and the impact of couplings with the rest of the structure. However, the overall derating is below 30%, which is reasonable. Indeed, the cooling system has been designed to account for a missing SCR in case of a fault. With safety margin, this corresponds to a 40% derating.

Another way of investigating the quality of the proposed layout is to check the cabling rules presented in Section II. This is all the more interesting because it avoids the heavy process of modifying the geometry, then running a long temporal simulation, analyzing the results, and modifying the geometry again.... The proposed cabling rules keep the link between the geometry and electrical characteristics and therefore, are suitable to build an optimization process: The geometry will be modified according to the cabling rule criteria using an appropriate optimization algorithm. This solution has been carried out successfully in another application [7]. In this case, however, this has not been necessary since the SCR derating was considered acceptable.

TABLE I
MEAN AND RMS CURRENTS OF ALL PHASES

Phase 1	SCR 1/4	SCR 2/3	SCR 5/8	SCR 6/7
Irms	2035	1540	1739	1351
Derating	21%	--	3.5%	--
Iavg	1194	917	1047	808.3
Derating	23%	--	8%	--
Phase 2				
Irms	2102	1588	1627	1163
Derating	25.1%	--	--	--
Iavg	1234	939	979	697
Derating	27%	--	0.9%	--
Phase 3				
Irms	1837	1434	1895	1510
Derating	9.34%	--	12.8%	--
Iavg	1083	877	1107	869
Derating	11.6%	--	14.1%	--
Phase 4				
Irms	1826	1328	1912	1401
Derating	8.7%	--	13.8%	--
Iavg	1083	812	1116	809
Derating	11.6%	--	15%	--
Phase 5				
Irms	1834	1550	1928	1423
Derating	9.2%	--	4.8%	--
Iavg	1077	863	1109	858
Derating	11%	--	14.3%	--
Phase 6				
Irms	1719	1353	1960	1447
Derating	2.3%	--	16.7%	--
Iavg	1014	766	1141	874
Derating	4.5%	--	17.6%	--

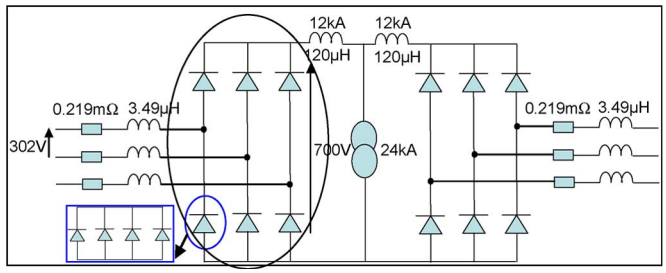

Fig. 7. Two full-bridge rectifiers feeding the same dc load. Only one has been considered for modeling. Each diode function is composed of four physical components.

Another application can be presented to illustrate the impact of a bad layout on the current division. This time, the rectifier is a conventional full-bridge topology. Two different rectifiers are used to feed the same dc load through the conventional interphase inductors (Fig. 7). The two converters are far enough; therefore, the mutual coupling between the two structures can be neglected, and only one rectifier has been studied.

Each diode function is realized using four diodes. The aim of the study is to investigate the impact of the rectifier layout on the current division. The complete layout, described in Fig. 8, has been modeled using the PEEC method, and the cabling rules (2) and (4) applied to this rectifier exhibit worse result than the previous rectifier. The time simulations (Fig. 9 and Table II) confirm this result, since the current division is poor (more than 37% derating). The explanation can be attributed to the

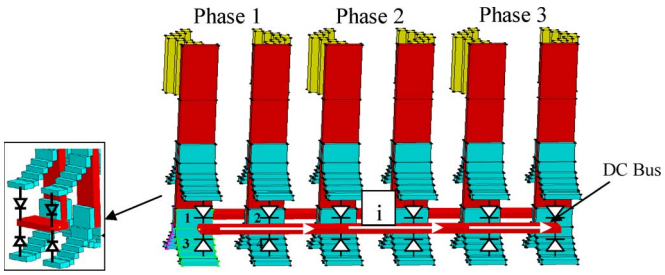

Fig. 8. The rectifier layout with the three phases and four diodes per phase.

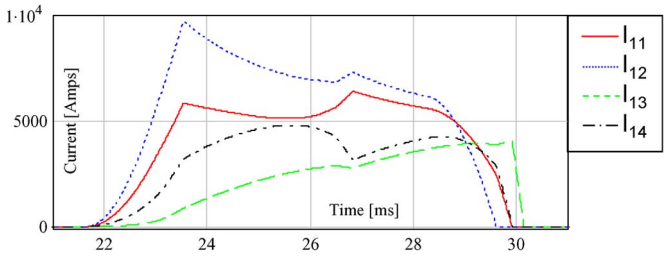

Fig. 9. Current division among the four diodes of phase 1 (simulation results).

TABLE II
RMS CURRENTS OF ALL FOUR DIODES OF PHASE 1

	Rms value	Derating
Irms D1	I_{11}rms = 3089	28.5%
Irms D2	I_{12}rms = 4052	37.4%
Irms D3	I_{13}rms = 1704	15.7%
Irms D4	I_{14}rms = 2036	21.3%

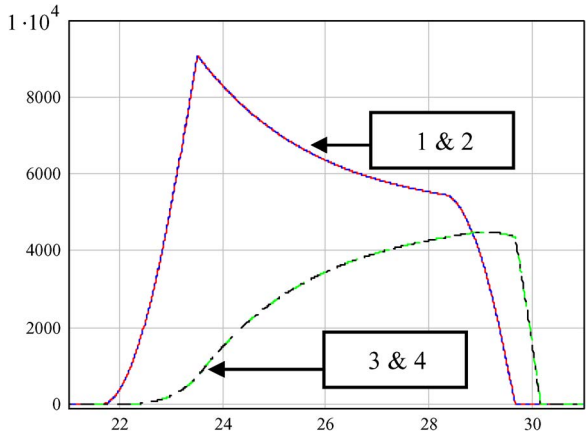

Fig. 10. Current division among the four diodes of phase 1 without any coupling between the phases and the dc bus (simulation results).

nonsymmetrical layout of the rectifier: Diodes 1 and 2, located close to the phase input, carry more current than diodes 3 and 4, which are far away. Additionally, the study of the impedance matrix has shown the importance of the couplings between the dc bus conductors and the phase conductors even if they are small, since the main directions are perpendicular. This is confirmed by the simulation results of Fig. 10, where these couplings have been mathematically cancelled. It shows the interest of the presented complete analysis without any assumption.

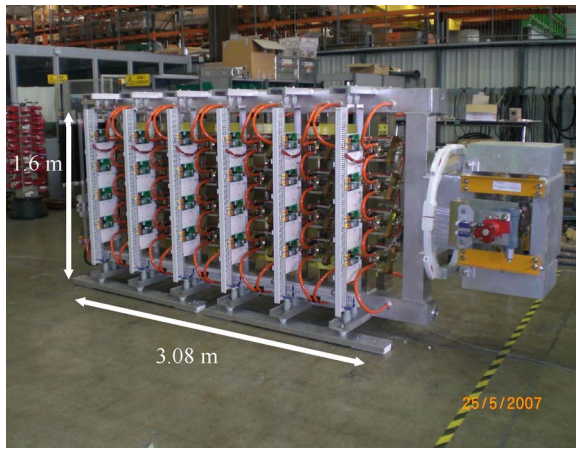

Fig. 11. View of the complete rectifier.

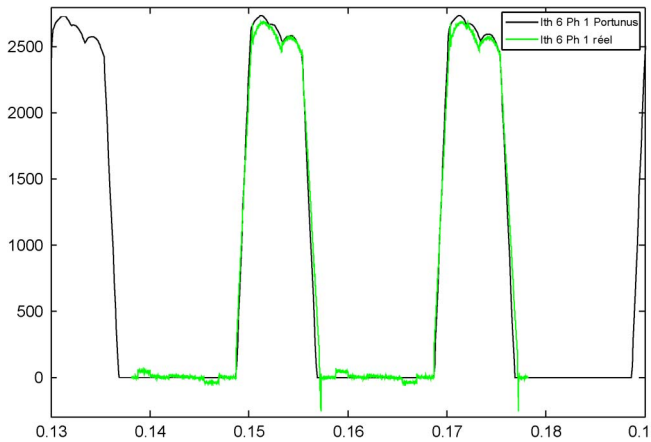

Fig. 12. Comparison of simulated and experimental results for SCR #6 of phase 1 in the case of a 10-kA test with two SCRs.

C. Experimental Validation

Several "low current" (10 and 15 kA) validations have been carried out on the actual rectifier (Fig. 11) to check the validity of the simulation (e.g., Figs. 12 and 13) and to validate the cooling aspects. At 10 kA, only two SCRs per phase were kept to validate the cooling.

The "low power" transformer was identified, since it was obviously different from the one designed for the 40-kA rectifier, and a new set of temporal simulations was carried out.

Fig. 12 shows the very good agreement between measured current in SCR #6 of phase 1. Experimental conditions were $Idc = 10$ kA, obtained in a short circuit with a firing angle of 71° and only two SCRs (5 and 6). Other measurements with SCRs 1 and 2 have also given the same good results. Fig. 13 shows the superposition of simulated and measured currents in SCRs 1 and 2 of phase 1 in the same operating conditions. In this case, the current division is not as bad as in the simulation of Fig. 6, since the operating conditions are different: The transformer is not the same, the current level is lower, and all SCRs are not used.

Some experimental results were also achieved at 15 kA with all SCRs, but all currents could not be recorded due to the number of current probes and space needed. The measurement of voltage drop across the fuses in series with the SCR allows a

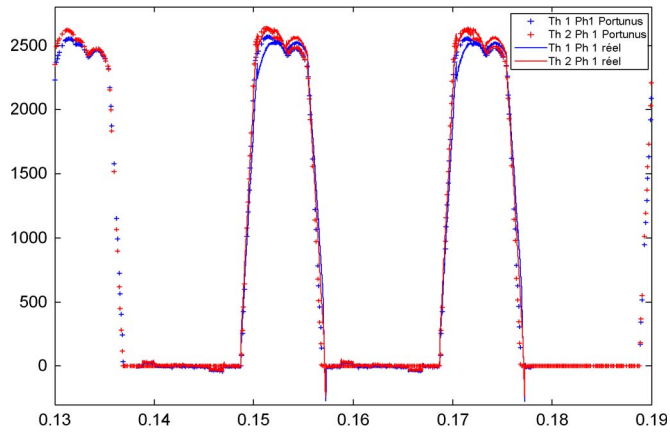

Fig. 13. Comparison of simulated and experimental results for SCRs 1 and 2 of phase 1 in the case of a 10-kA test with two SCRs. Solid lines: simulation. Cross: measurement.

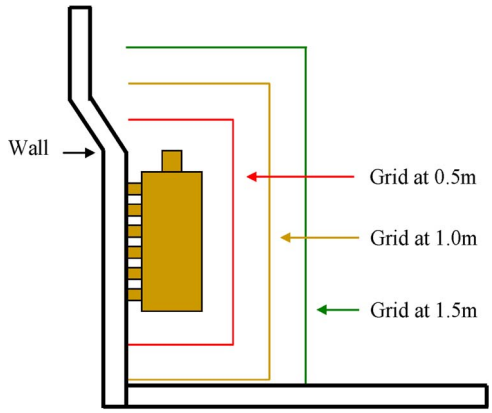

Fig. 14. Grid definition for magnetic field computation.

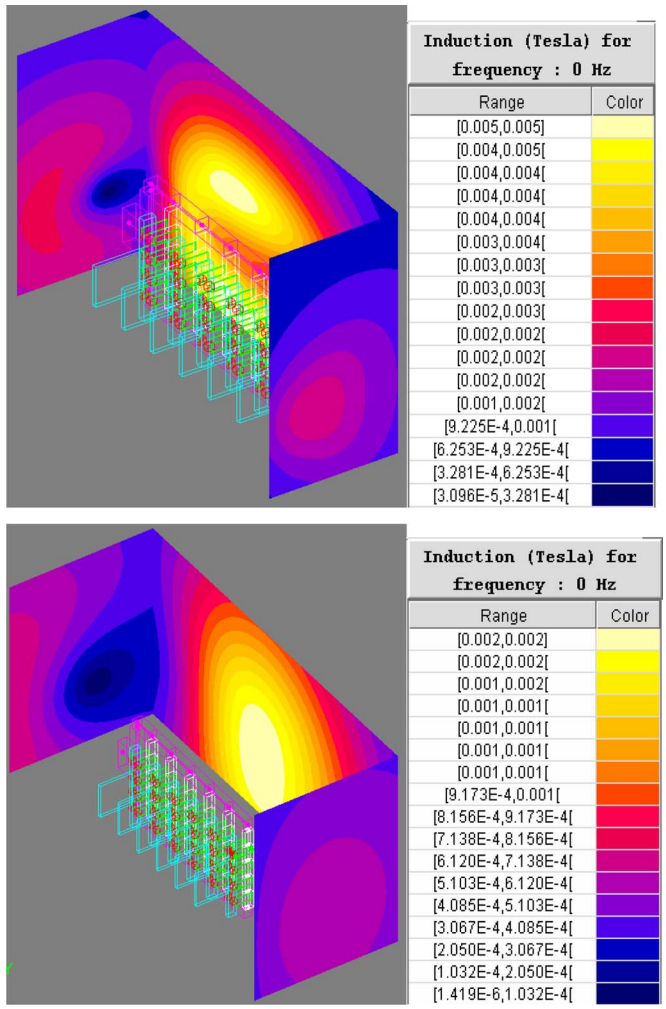

Fig. 15. DC Induction at (top) 0.5 m and (bottom) 1.5 m obtained with PEEC method.

rough estimate of the current flowing through the device. This has confirmed the tendency obtained in the simulation: The most loaded devices are the external ones (1 and 4, and 5 and 8).

In conclusion, the good agreement between current commutation speed in one SCR validates the PEEC model of the rectifier because it is only due to cabling impedance. Furthermore, the tendency when using all eight SCRs has also been validated.

D. Close Field Map

After the converter modeling validation, we focused on near magnetic field. The field spectrum obviously contains not only a dc part but also ac components, due to the waveforms of the SCR currents. By using Fourier series, the ac magnetic field can be obtained by superposition of several field maps at various frequencies representing the harmonic decomposition of the SCR currents. Due to the decrease of harmonic amplitude with the order, we only focused on the fundamental component (50 Hz). It is worthy of note that the dc field is much more restrictive for all the control boards of the SCRs and the electrical cabinets.

1) Positioning of the Cartography Grids: Magnetic induction was computed and plotted on a grid and shown in Fig. 14. Three different distances were defined in order to investigate the decrease of the field with the distance (0.5, 1, and 1.5 m). The height of the grid has been chosen 3 m higher than a human being.

Some results are shown on Fig. 15 for dc component and Fig. 16 for the 50-Hz ac field. It is worth noting that the induction global shape is more complex near the rectifier than far from it.

This can be explained by the multipole expansion theory [14]: Far from a radiating source, only the dipole term is preponderant, whereas near the device, higher orders appear.

Compared with dc, the induction shape is changed at 50 Hz, as shown in Fig. 16. This is due to the different localization of ac currents compared with dc currents.

All results are summarized in Table III. Induction stays at low values at any distance and frequency, which is reassuring for human exposure (service engineering). Furthermore, control boards of SCR have been tested at 150-gauss dc fields without any problem.

V. Conclusion

High-current rectifier layout impacts on several aspects and mainly on current division, as well as on induction radiated around the converter. Even if the problem of current division

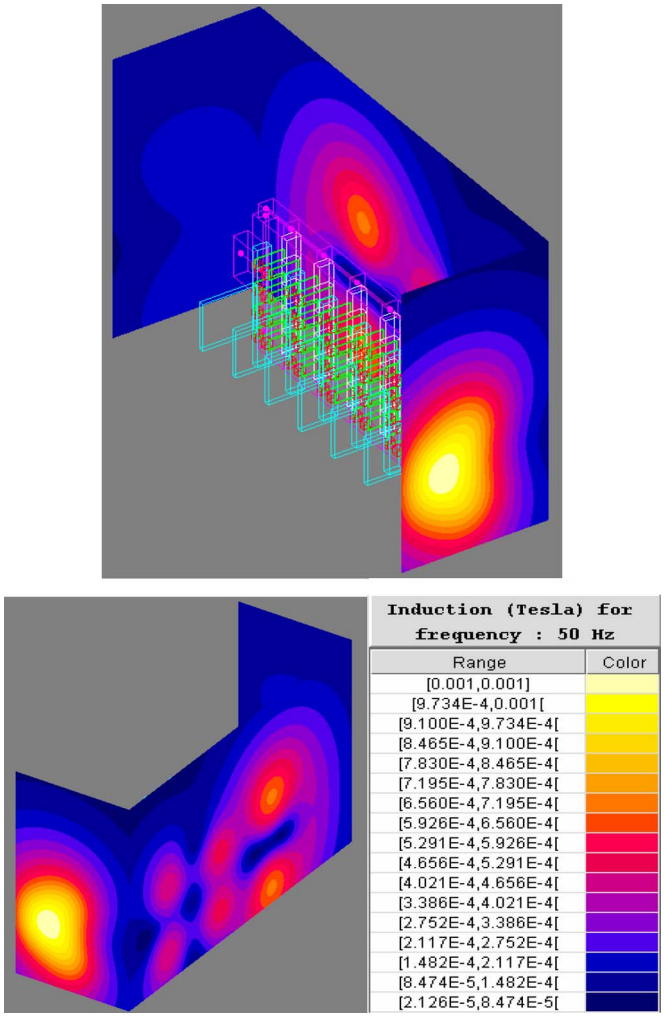

Fig. 16. AC induction at 0.5 m (50 Hz) obtained with PEEC Method.

TABLE III
SUMMARY OF MAXIMUM AND MINIMUM INDUCTION VALUES

		0.5 m	*1.0 m*	*1.5 m*
DC Field	Maximum Value (Gauss)	*50*	*30*	*20*
	Minimum Value (Gauss)	*0.309*	*0.076*	*0.0141*
AC Field	Maximum Value (Gauss)	*10*	*2.7*	*1.3*
	Minimum Value (Gauss)	*0.21*	*0.31*	*0.166*

has been known since tens of years, new modeling tools allow a better precision for layout investigation. The PEEC method is well adapted for this purpose. It provides an electrical equivalent circuit of the converter layout. A coupling with simulation software allows a direct analysis of temporal current waveforms. Cabling rules have also been presented: Starting from the equivalent modeling of the converter, they give restrictions on the impedance matrix of the system in order to guarantee a good current division. The use of these rules allows avoiding temporal simulation and opens the possibility of automatic layout optimization of such high-power rectifiers. The proposed

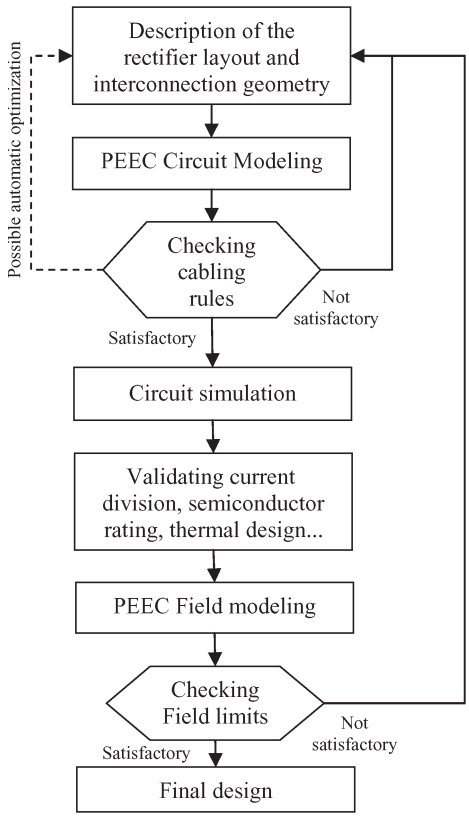

Fig. 17. Flowchart of the proposed design procedure.

design procedure is shown in Fig. 17. A tentative layout can be quickly evaluated owing to the proposed cabling rules; when it is considered satisfying, a temporal simulation can be carried out, and electrical performances checked. Then, magnetic induction limits close to the rectifier can be investigated and compared with existing or future standards. This may allow much savings in such high-power engineering design activities.

An optimization process can even be proposed in the near future: The layout geometry may be the result of automatic design; the objective function being the proposed cabling rules. This has been achieved successfully in other applications [7]: The main difficulty is to describe the complex 3-D geometry and all associated constraints with a sufficient number of parameters.

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