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F Roccaforte, F Giannazzo, V Raineri

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Consiglio Nazionale delle Ricerche – Istituto per la Microelettronica e Microsistemi (CNR-IMM),
Strada VIII n. 5, Zona Industriale, I-95121 Catania, Italy

E-mail: fabrizio.roccaforte@imm.cnr.it, filippo.giannazzo@imm.cnr.it, vito.raineri@imm.cnr.it

Abstract. Wide band gap semiconductors promise devices with performances not achievable using silicon technology. Among them, Silicon Carbide (SiC) is considered the top-notch material for a new generation of power electronic devices, ensuring the improved energy efficiency requested in the modern society. In spite of the significant progresses achieved in the last decade in the material quality, there are still several scientific open issues related to the basic transport properties at SiC interfaces and ion-doped regions that can affect the devices performances, keeping them still far from their theoretical limits. Hence, significant efforts in fundamental research at nanoscale have become mandatory to better understand the carrier transport phenomena, both at surfaces and interfaces. In this paper, the most recent experiences on nanoscale transport properties will be addressed, reviewing the relevant key points for the basic devices building blocks. The selected topics include the major concerns related to the electronic transport in metal/SiC interfaces, to the carrier concentration and mobility in ion-doped regions, and to channel mobility in metal/oxide/SiC systems. Some aspects related to interfaces between different SiC polytypes are also presented. All these issues will be discussed considering the current status and the drawbacks of SiC devices.
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1. Introduction

Nowadays, the increasing need of electric power, the rising costs of energy and its impact on environment have become important concerns in our society. Only reducing the consumption of electric energy through its efficient use also in electronics systems can lead to a remarkable decrease of the overall energy consumption. Then, the request of higher energy efficiency is investing the Information and Communication Technology (ICT), the consumer electronics, the household appliance and transportation (e.g., electric vehicles). Consequently, the power electronics semiconductor roadmap cannot be anymore approached simply by increasing the electric power density to reduce the device cost, as commonly assumed so far, but rather more efficient devices should be implemented.

Wide band gap semiconductors such as Silicon Carbide (SiC), Gallium Nitride (GaN) and related compounds are the most promising materials for the next generation of advanced electronic power devices to meet the requirements of high performance integrated electronics systems, since they can achieve performances, including energy efficiency, well beyond the silicon limits [1, 2, 3]. Then, for many applications, the implementation of devices in these materials can be justified in spite of the high material costs. The outstanding physical properties of wide band gap materials can lead to tremendous advantages for high-temperature, high-power and high-frequency operation, as well as low noise capability and radiation hardness. Devices with very low specific on-resistance (R_{on}) and high blocking voltages are in principle possible, driving to ideal "zero-loss" components in terms of the dissipated power.

SiC is undoubtedly the wide band gap semiconductor that has reached the largest maturity in terms of crystal quality, wafer size and device processing capability. It is well known that SiC presents a large number of different crystalline forms called "polytypes", differing from the stacking sequences of the basic Si-C bilayer component [4]. The most common polytypes used in electronics are 3C-SiC, 6H-SiC and 4H-SiC. Table 1 reports the relevant physical properties of these crystals, compared with those of silicon (Si). For enhanced devices performances, an important feature is the wide band gap of SiC polytypes, which determines the high critical breakdown field E_B (1-3 MV/cm), typically around one order of magnitude larger than that of Si (0.3 MV/cm). As a matter of fact, a higher critical field results into a higher breakdown voltage for a fixed thickness of the device active layer. Additionally, for a targeted device breakdown voltage, it is possible the use of thinner epilayers, thus allowing to significantly reduce the R_{on} and, hence, the power losses. Finally, the wide band gap leads to a very low intrinsic carrier concentration n_i (several order of magnitudes lower than in Si), which is important to guarantee low leakage currents even at high temperatures operation.

Starting from the beginning of the 1990s, SiC material growth and device technology have seen tremendous progresses, culminated in the availability of high quality hexagonal, large area single crystalline wafers (6H-SiC and 4H-SiC), suitable for electronics devices fabrication. In particular, the evolution of 4H-SiC material led recently to very low (< 1 cm^{-2}) or even zero "micropipe" density in commercial wafers up to 100 mm in diameter [5], while 150 mm wafers are expected for 2011. The evolution of the material quality was accompanied by the demonstration of several devices suitable for high-power applications [6,7,8,9], although the only market success has taken place in the area of Schottky diodes [9,10]. In this sense, the gradual elimination of micropipes (that are electrically "killer defects") in SiC epilayers represented a fundamental step towards ideal metal/SiC Schottky barriers and high device yield [11,12].

In spite of the significant progresses attained in the last decade, several scientific issues are still open. In particular, to date many crucial aspects concerning the carrier transport at surfaces and interfaces remain unclear. A nanoscale scientific approach, also involving innovative characterization, can be the way to unhinge the field and introduce a groundbreaking knowledge to finally achieve the material theoretical limits.

In this review paper, some recent advances on the charge transport at SiC interfaces are reported. In particular, the paper will focus on the major concerns related to the transport in metal/SiC Schottky barriers at the nanoscale, and on the critical issues related to the local carrier mobility, going from bulk and epi material, to properties in ion-implanted regions. Finally, the challenging channel mobility at SiO_2/SiC interfaces and some aspects related to heteropolytype SiC interfaces are discussed.
All these issues will be argued in the framework of the present status of SiC technology, considering the perspectives and the common drawbacks in SiC electronic devices technology.

2. Electronic transport through metal/SiC interfaces

The electronic transport across metal/SiC interfaces, i.e. both Ohmic and rectifying (Schottky) contacts, has been the subject of extensive scientific investigations in the last decade [10, 13,14]. The main reasons are the need to achieve a very-low contact resistance to reduce the passive contribution to device performances, and to attain an ideal and reliable behaviour in the forward and reverse characteristics of Schottky diodes. However, the peculiar inhomogeneous nature of metal/SiC interfaces requires the knowledge and the control of the interfacial properties at a nanoscale level, in order to predict the behaviour of macroscopic contacts and, ultimately, to achieve the desired devices performances. Only recently, a clear experimental correlation between nanoscale inhomogeneities and macroscopic properties has been demonstrated in SiC and other wide-band-gap materials [15]. In this way, the basic understanding of the electronic transport through metal/SiC interfaces has been significantly improved, thus providing a fundamental feedback to optimize the surface and interface processing and the metallization schemes, in relation to the particular device application. All these concepts will be discussed in this section, giving an overview of the studies on inhomogeneous Schottky barriers to SiC, by considering some important implications for practical devices fabrication.

2.1. Nanoscale inhomogeneity of Schottky barriers to n-type SiC

Metal/semiconductor contacts are fundamental parts of all semiconductor electronic and opto-electronic devices. The most important parameter in these systems is the Schottky barrier height (SBH). The control and reproducibility of the electrical properties of Schottky barriers are often critical issues. As a matter of fact, Schottky contacts to SiC often exhibit a non-ideal behaviour in the current-voltage characteristics (I-V), with even a large dispersion from one device to another and significant anomalies in the temperature dependence of the electrical parameters (Schottky barrier height, ideality factor,…). Therefore, it is clearly important to understand the nature of such non-ideal behaviour, investigating to which extent the material quality and/or the surface preparation play a role in the carrier transport through the interfaces.

Table 2 reports the values of the Schottky barrier height (Φ_B) for different metal/SiC contacts, for the most common polytypes, 3C-SiC [16 , 17 , 18], 6H-SiC [19 , 20 , 21 , 22 , 23 , 24 , 25 , 26 ,] and 4H-SiC [27,28,29,30,31,32,33,34,35,36]. These values are a selection among a large amount of published data. They were determined by the analysis of the forward I-V characteristics of Schottky diodes (see Ref. [37] for details on this method). The data refer to the case of non-annealed contacts on n-type material and to the Si-face terminated for the hexagonal polytypes. The small amount of data available for 3C-SiC depends on the poor material quality available, which has limited the studies on Schottky contacts in the last years. More data can be found for the hexagonal polytypes, where the most commonly used metals for Schottky contacts are Ti and Ni, which typically show a higher reproducibility of the barrier height, and have been easily integrated in the fabrication of Schottky diodes. In other works, "non conventional" metallization schemes have been recently investigated, like metal borides [38], or rare earth oxides [39], which should give a better thermal stability of the barrier.

First, it must be pointed out that the experimental values of Φ_B reported in Table 2 are lower than the theoretical ones predicted by the classical Schottky-Mott theory, as the difference of the metal work function and the semiconductor electron affinity [40]. Hence, different physical models must be invoked to explain the reduced I-V barrier height and the deviation from the ideal behaviour observed in metal/SiC contacts. As an example, the occurrence of carrier transport mechanisms other than the thermionic emission, such as tunnelling current through the barrier [41] could be considered. However, at the typical doping levels used for n-type SiC Schottky diodes ($<5\times10^{16}$ cm^{-3}), the effect of tunnelling through the barrier at room temperature is very low under forward bias, and it may become significant only under strong reverse bias [42].

Hence, a common approach is to consider of a thin interfacial insulating layer, introduced to describe the presence of interface states at the metal/SiC contact [43]. These states, located at the interface between the semiconductor and the insulating layer, are characterized by a neutral level Φ_0, i.e. the energy level (relative to the valence band) to which the interface states are filled when the surface is neutral.

According to this description, it is useful to report the dependence of the SBH on the metal work function.

The SBH values are reported in figure 1 as a function of the metal work function Φ_m for the three SiC polytypes. A general trend can be observed, with the values of Φ_B that increase with increasing metal work function Φ_m. Moreover, the experimental values of Φ_B are, on average, lower in the case of 3C-SiC, and increase for 6H-SiC and 4H-SiC, respectively. This behaviour can be explained by the different values of electron affinity, i.e., 3.8 eV in 3C-SiC, 3.3 eV in 6H-SiC, and 3.1 eV in 4H-SiC. Besides this polytype dependence, figure 1 gives useful insights on the intrinsic nature of the metal/SiC interface. The slope of the Φ_B vs Φ_m plot is the so-called "interface index" *S*, and is defined as $\frac{\partial \Phi_B}{\partial \Phi_m}$ or $\frac{\partial \Phi_B}{\partial \chi_m}$, depending on whether the work function Φ_m or the electronegativity χ_m of the metal is considered. The interface index S is a parameter that gives an indication on the ideality of the metal/semiconductor Schottky contacts. In particular, for $S \approx 1$ a pure Schottky-Mott behaviour is expected, with the barrier height given by the difference of the metal work function and the semiconductor electron affinity ($\Phi_B = \Phi_m - \chi_s$). On the other hand, for $S \approx 0$ a complete "Fermi level pinning" to the defined position Φ_0 occurs and the carrier transport properties are almost uniquely determined by the interface states, independently of the metal [44]. Under these conditions, known as the Bardeen limit [45], the barrier height value is given by $\Phi_B = E_g - \Phi_0$, where E_g is the forbidden energy gap.

For the data reported in figure 1 the values of the interface index *S* are lower than 1, meaning that a partial Fermi level pinning at the surface occurs. It is worth noting that similar values of the interface index are found for three

polytypes, being S in 3C-SiC (0.32) only slightly lower than the values found in the hexagonal polytypes (0.40-0.41). According to the model proposed by Kurtin *et al.* [46], the interface index is expected to increase with the degree of ionicity of the semiconductor, defined as the difference in the electronegativities of the two components ($\Delta\chi_s$). Hence, due to the degree of ionicity of SiC ($\Delta\chi_s$=0.65 eV) the behaviour of metal/SiC interfaces is intermediate between a strong Fermi level pinning (Bardeen limit) and an ideal Schottky behaviour (Schottky-Mott limit), in agreement with the results shown in figure 1. Edwing *et al.* [47] recently modelled the non-ideal behaviour of Schottky diodes on 4H-SiC under forward bias by the presence of two non-interacting barriers put in parallel (a high barrier and a low barrier). In particular, extracting the value of Φ_B for the high barrier regions they found a similar dependence on the metal work function (with S=0.45) as the one deduced by the data in figure 1. On the other hand, the low barrier regions of the diodes gave no dependence on the metal work function, indicating the complete pinning of the Fermi level. This latter was ascribed to the presence of specific defects in the diodes showing strongly non-ideal behaviour. Only a few authors reported that under specific surface treatments an "un-pinned" Fermi level ($S \approx 1$) can be achieved in metal/6H-SiC contacts, with the virtual elimination of interface states and the achievement of the ideal barrier value [48].

The interfacial layer model and the presence of surface states cannot fully explain important aspects related to the carrier transport through metal/SiC Schottky interfaces, such as the temperature dependence of the electrical parameters n and Φ_B , typically observed in Schottky diodes. In fact, the model predicts a temperature independent ideality factor n [42,43].

Hence, another view to describe non-ideal metal/SiC Schottky barriers, consistent with the behavior of the SBH in macroscopic diodes, is to consider the "lateral uniformity" of the barrier at a nanoscale level. In this context, a deeper understanding was accomplished in the last years, thanks to the development of novel techniques enabling to monitor the local transport properties with a nm-scale spatial resolution [49].

Starting from the evidence that the I-V characteristics of macroscopic diodes show significant variations from device to device, although the interface is prepared under the same chemical conditions, Im *et al.* [25,50] gave the first nanoscale approach to explain the non-ideal electrical behavior of Schottky contacts to SiC. In particular, they monitored the local fluctuations of the SBH in the Pd/6H-SiC system by means of Ballistic Electron Emission Microscopy (BEEM) [51], acquiring several BEEM spectra at different locations over the sample surface. The local Schottky barrier height values showed a Gaussian distribution, indicating that the metal/SiC interface is not characterized by a unique value of Φ_B but rather a lateral inhomogeneity of the barrier height is present. Correlating the behaviour of the macroscopic diodes with the nanoscale measurements of the local barrier height it was possible to explain the electronic transport and the non-ideality of the metal/SiC interface using the Tung's model on "inhomogeneous" Schottky barriers [52]. Accordingly, the inhomogeneous Schottky barrier can be described as a distribution of low barrier "patches" embedded inside a background of a higher uniform barrier [52]. Clearly, the presence of nanometer-size patches with a low barrier can give a disproportionately large effect on the I-V characteristics, due to the exponential dependence on the barrier height of the current flow through the metal/semiconductor contact. Assuming a geometry based on circular patches of low SBH embedded in a region of higher SBH Φ_{B0}, the ideality factor n and the effective barrier height Φ_{eff} can be expressed as [53]

$$n = 1 + \frac{\gamma}{3\eta^{\frac{1}{3}} V_{bb}^{\frac{2}{3}}} \tag{1}$$

$$\Phi_{eff} = \Phi_{B0} - \gamma\left(\frac{V_{bb}}{\eta}\right)^{\frac{1}{3}} \tag{2}$$

where V_{bb} is the band bending (i.e. the diffusion potential of the diode) [43] and $\eta = \varepsilon_s/qN_D$, ε_s being the permittivity of the material and N_D the doping concentration. Here, γ is a parameter that takes into account the size and the barrier height of the single patch [53].

The above formalism clearly indicates that a nanoscale lateral inhomogeneity of the Schottky interface manifests itself through a deviation from the ideal behavior ($n > 1$) and a lowering of the experimental SBH with respect to the theoretical one ($\Phi_{eff} < \Phi_{B0}$) in macroscopic diodes.

This description allowed to explain a large number of anomalies of the electrical behaviour of Schottky contacts in SiC. As an example, Roccaforte *et al.* [34] investigated the electrical behaviour of Ni_2Si/4H-SiC Schottky diodes at different temperatures, to understand the microscopic nature of the barrier. Figure 2 reports the values of n and Φ_B as a function of the temperature for Ni_2Si/4H-SiC Schottky diodes. As can be seen, both n and Φ_B exhibit a significant dependence on the junction temperature. In particular, by decreasing the temperature the ideality factor increases, while the value of the SBH decreases. The temperature dependence of n and Φ_B can be interpreted as the "macroscopic manifestation" of a nanoscale lateral inhomogeneity of the Schottky barrier. In a simplified manner, this dependence can be explained as described in the following: In a lateral inhomogeneous barrier, the current flow through the high barrier regions becomes dominant at high temperature, i.e., when the carriers can overcome the highest barrier by a nearly pure thermionic mechanism. Therefore, an ideality factor very close to one and a high value of Φ_B (close to the theoretical value) are measured. On the other hand, at lower temperatures, electrons have sufficient energy only to overcome the lower barrier "patches", thus leading to an increase of the ideality factor and a lowering of the Φ_B values. Furthermore, a linear correlation between the values of n and Φ_B obtained at the different temperatures could be observed, as shown in the inset of figure 2. Schmitsdorf *et al.* [54] ascribed the correlation between n and $\Phi_{B,}$ determined at room temperature on a set of different diodes, to the inhomogeneous nature of the Schottky barriers. In fact, starting from Tung's theory [52], in an inhomogeneous barrier a linear correlation between these parameters can be expected, as can be deduced by their analytical expressions given in (1) and (2) [53]. From the data reported in the inset in figure 2, an average barrier height Φ_{B0} = 1.69 eV could be determined by the extrapolation of the barrier height at n = 1, that is the barrier height of the "homogeneous" Ni_2Si/4H-SiC interface [34]. Using this approach, the underestimation of the Richardson's constant in 4H-SiC, often reported in literature, was attributed to the inhomogeneity of the barrier, where the effective area A_{eff} involved in the current transport can be significantly lower (even a few percents) than the geometric area of the contact [34]. After this study, a similar approach was successfully applied by other authors to explain the temperature dependence of the electrical characteristics of Schottky barriers on SiC [55, 56].

A quite important nanoscale issue affecting the properties of the Schottky barrier is the surface processing. In fact, the electrical properties of Schottky contacts to SiC show a significant dependence on the surface preparation at nanoscale before metal deposition [35,39,57,58,59,60,61], and on post deposition annealing. As an example, surface roughness, interfacial contaminants, residual thin oxide layers, etc., can affect the uniformity of the Schottky barrier and, consequently, lead to non-ideal I-V characteristics of Schottky contacts.

The "sacrificial oxidation" (i.e., the thermal oxidation of SiC followed by removal of the grown oxide layer) has been proposed as a method to obtain a "clean" surface in order to improve the electrical properties of Schottky barriers fabricated on it [58]. In fact, the consumption of a near-surface layer, which may be non-ideal in terms of crystal quality or may be contaminated during preparation, should guarantee a better homogeneity of the metal/SiC barrier. However, also the process used to remove the sacrificial oxide, and the oxidation itself, can be crucial for the nanoscale lateral homogeneity of the barrier and, hence, for the overall reproducibility of the electrical characteristics.

Giannazzo *et al.* [62] investigated the nanoscale homogeneity of the Schottky barrier in a Au/6H-SiC structure, with and without the presence of a nanometric non-uniform interfacial thermal oxide layer, i.e., a typical situation that may occur during device fabrication. A method based on conductive atomic force microscopy (C-AFM) was used for the local mapping of the barrier uniformity with a spatial resolution in the order of the AFM tip size [62] (see appendix A.1). Figure 3 shows the distribution of the local SBHs values of Au/SiC contacts, with an interfacial non-uniform oxide layer and for a "clean" surface where this interlayer was removed by an appropriate wet etch in buffered hydrofluoric acid. As can be seen, a broad barrier height distribution, peaked at 1.48 eV with a FWHM of 0.25 eV, is observed in the presence of a residual oxide layer. The average Schottky barrier height increases after optimal removal of the interlayer (1.81 eV), where also a narrower distribution (~ 0.1eV) is obtained, thus indicating a better nanoscale lateral homogeneity of the "clean" contact. This result demonstrates that only a nanoscale control of SiC surfaces can enable to approach the ideal behaviour.

Some metallic systems used as Schottky contacts to SiC have shown a better reproducibility of the electrical properties, being the barrier height almost independent of the surface preparation. As an example,

nickel silicides, formed by a thermal reaction of Ni films with SiC above 600°C, can result in a nearly ideal behaviour of the contact by the consumption of a SiC surface-layer during the silicidation process [61]. The high reproducibility of this process has recently been used for Schottky-type UV detectors fabricated in 4H-SiC [63], where the high barrier of Ni_2Si and the low leakage current are crucial to obtain a high optical sensitivity. Furthermore, due to the high SBH, Ni_2Si exhibits a lower leakage current than Ti (the low-barrier metal typically used for power device applications) and, hence, can be suitable for increasing the maximum operation temperature of Schottky diodes for high-temperature and/or high voltage applications [22].

Beyond the intrinsic inhomogeneous nature of the Schottky barrier and the influence of the surface preparation, point defects in the surface-region and/or in the bulk can also affect the carrier transport through metal/SiC Schottky interfaces. Recently, new fundamental insights have been achieved by correlating the surface preparation with the electronic properties of both metal/SiC interfaces and bulk material. In particular, the role of the sacrificial oxidation has been recently clarified, demonstrating that the process not only consumes a layer of SiC but also reduces the concentration of the Z_1/Z_2 centers in 4H-SiC in the remaining material [64]. In this way, the carrier lifetime can be increased, improving the characteristics of Schottky diodes. This recent finding is particularly important for SiC technology. In fact, the Z_1/Z_2 level is one of the most common deep centers observed in 4H-SiC and is typically associated to an intrinsic carbon-related defect such, as a carbon vacancy (V_C) or a carbon interstitial (I_C) [65]. Its presence has been demonstrated to have a strong impact on the leakage current in Schottky contacts [66]. It has been argued that carbon and/or silicon atoms emitted from the SiO_2/SiC interface formed during sacrificial thermal oxidation can diffuse inside the epilayer, and consequently, their interstitials annihilate via recombination with carbon vacancies, which may be the main constituent of the Z_1/Z_2 defect [64].

Finally, another important issue for Schottky interfaces in SiC is the possibility to tailor the Schottky barrier in power rectifiers, in order to minimize the power losses. For this purpose, a minimum on-state voltage drop is required, which in turn can be achieved by using a metal with a low SBH. This latter can however lead to an undesired increase of the leakage current under reverse bias. Hence, new devices concepts involving an engineering of the Schottky interface both at a microscopic and at a nanoscale level are required. As an example, dual-metal-pinch rectifiers formed by micrometric stripes alternating low and high barrier height metals (Ti/Ni_2Si) can allow to combine the advantages of the Ti ($\Phi_B \approx 1.2$ eV) under forward bias and of the Ni_2Si ($\Phi_B \approx 1.6$ eV) under reverse bias [22]. Furthermore, also new nanoscale approaches for the manufacturing of Schottky contacts to SiC with lower barrier have been proposed, involving the formation of Au nanoparticles/SiC interfaces, whose electrical properties (i.e., the barrier height) critically depend on the size of the nanoparticles [67,68].

Clearly, the improved knowledge gained on the inhomogeneous nature of Schottky barriers to SiC is fundamental for devices applications, to identify the right surface preparation conditions, and to define the appropriate metallization schemes or post-deposition annealing in order to achieve the desired performances.

2.2. Ohmic contacts to SiC

Ohmic contacts to SiC are typically formed by the deposition of a metal or an alloy (Ni, Ti, Ta, Ti-Al, Ni-Al, etc.) followed by post-annealing treatments in the temperature range of 900-1000°C. For the n-type doped material, Ni-based contacts are used. While Schottky behaviour is observed in Ni/SiC contacts annealed at around 600°C, a transition to Ohmic contact gradually occurs upon annealing at higher temperatures, between 600°C and 950°C. Thermal annealing above 500°C induces a solid state reaction, leading to the formation of different nickel silicides phases ($Ni_{32}Si_{12}$, Ni_2Si,…), which evolve in the most stable Ni_2Si upon annealing at 950°C [69,70]. Typical values of the specific contact resistance ρ_c of Ni_2Si contacts onto heavily doped n-type SiC reported in the literature range between 10^{-5}-10^{-7} Ωcm^2. The mechanisms of current transport and Ohmic contact formation in the Ni_2Si/SiC system have been widely discussed in some review papers [13,14]. According to the common interpretation, a high concentration of carbon vacancies at the silicide/SiC interface is generated upon annealing, acting as donors and increasing the net carrier concentration below the metal [71]. Under these conditions, the Ni_2Si/SiC barrier becomes narrower, thus enhancing the electron tunneling and, hence, an Ohmic conduction mechanism. Furthermore, a decrease of the homogeneity of the silicide/SiC barrier occurring by

increasing the annealing temperatures from 600°C to 950°C (i.e., where a significant electro-structural evolution of the silicides phases is observed) can also play a role in this electrical transition [13,72].

The formation of Ohmic contacts to p-type SiC is more complicated than in n-type material, due to the difficulty to obtain low Schottky barrier heights values. In fact, considering the energy gap (2.35-3.28 eV) and the electron affinity (3.1-3.8 eV) of SiC polytypes, the valence band lies around 6 eV away from the vacuum level. Hence, since the metals have work function in the range 4-5.5 eV, a high energy difference arises between the conducting carriers of the metal and the p-type SiC.

Because of the low Schottky barrier, Al- or Ti/Al-based alloyed contacts are commonly used as Ohmic contacts to p-type SiC, leading to values of specific contact resistance in the order of 10^{-3}-10^{-5} Ωcm^2[14]. However, from the experimental results reported on Ti-Al Ohmic contacts to p-type SiC, it is not clear whether the spiking due to intrusions of the annealed metal into SiC leads to an increase of the doping by Al-indiffusion or rather the intrusions themselves act as field emitters increasing the leakage current and leading to the formation of an Ohmic contact [14].

Even if some ambiguities still remain in the explanation of the Schottky-to-Ohmic transition after contacts annealing, the formation of low-resistance Ohmic contacts on heavily doped epitaxial SiC layers cannot be considered as a major technological concern. However, for many devices applications, ion-implantation is used to achieve selective area doping of SiC. In this case, the contact properties on ion-implanted layers will depend on the local values of the carrier concentration and mobility underneath the metal. These values, in turn, are strongly related to the implantation and post-annealing conditions, and to the presence of ion-induced material defects. Obviously, some of these aspects, that are less relevant when studying contacts and interfaces properties on epitaxial layers (i.e., with a uniform doping), become crucial in practical devices.

These important issues will be discussed in the next section, which reports the recent results on depth profiling of carrier concentration and mobility in epitaxial and implanted SiC materials.

3. Profiling carrier concentration and mobility in SiC

Profiling carrier concentration and mobility is fundamental to understand the overall electronic transport properties both of epitaxially grown and ion-implanted semiconductors. To date, most of the studies on carrier concentration and mobility in SiC have been carried out considering epitaxial substrates, where the carrier concentration is almost constant in depth. However, monitoring also the interfacial properties in epitaxial layers has become crucial to check the abruptness of the changes in concentration, which is particularly critical in some applications requiring the use of very thin epitaxial layers. In the case of ion-implanted materials, conventional "integral" characterization methods (like Hall measurements and sheet resistance measurements [37]) have been mainly employed to determine the average electrical behaviour of the layer. However, in ion-implanted materials, the carrier concentration can be affected by local phenomena, e.g., the precipitation of dopants at the projected ion-range R_p in electrically inactive complexes, or the presence of defects acting as compensating centers in the end-of-the range region, close to the junction area (depleted region). The same surface region can be affected by local phenomena influencing mobility and dopant activation.

In this section, the status of depth profiling of carrier concentration and mobility in SiC will be discussed, both for epitaxial and ion-implanted material. These aspects are crucial to predict the device behaviour, particularly in complex devices, where the carrier concentration is modulated in depth and laterally close to surfaces and interfaces.

3.1. Temperature dependence of carrier concentration and mobility

Since high-power and high-temperature electronics are the most important fields of application for SiC devices, the knowledge of the temperature behaviour of the electronics properties of the bulk material (epitaxial or implanted) is a fundamental issue.

The temperature dependence of the carrier density and electron mobility in SiC have been extensively investigated by Hall effect and sheet resistance measurements in epitaxial layers, n-type doped with nitrogen (N) [73,74] and p-type doped with aluminum (Al). N donors can occupy two different substitutional positions (hexagonal or cubic) in the C- sublattice, and two different ionization energies are associated to those

configurations (ΔE_h=62 meV, ΔE_k=110 meV below the conduction band edge). Two distinct ionization energies have been reported also for Al acceptors corresponding to two non-equivalent substitutional positions in the Si sublattice of 4H-SiC [75]. The acceptors levels with respect to the valence band (ΔE_1 and ΔE_2) depend on the acceptor concentration (N_A) according to the relation $\Delta E_i = \Delta E_i^0 - \alpha N_A^{1/3}$, where $\Delta E_1^0 \approx 190$ meV and $\Delta E_2^0 \approx 230$ meV and $\alpha \approx 1.9\times10^{-5}$ meV×cm. Due to the high ionization energies, the hole density at room temperature is only a fraction of the acceptor density.

The mechanisms limiting the electron mobility in N- doped 4H- and 6H- SiC epi-layers have been investigated in detail as a function of doping concentration and temperature. At room temperature and low concentrations the mobility μ is limited by intrinsic phonon scattering (acoustic intravalley, intervalley and polar). At carrier densities values larger than 5×10^{16} cm^{-3} the ionized impurities scattering becomes more important. Finally, at very high electron densities the neutral impurity mode comes into play [76].

Figure 4a reports the temperature dependence of the electron mobility of lightly nitrogen (N) doped (10^{15}-10^{16} cm^{-3}) 4H- and 6H-SiC epilayers, measured by Hall effect in the standard configuration (magnetic field parallel to c-axis, current parallel to the basal plane) [73,74]. In the reported temperature range, intervalley scattering by lattice phonons represents the dominant mechanism limiting in-plane electron mobility in SiC [73]. On the other hand, the "vertical" drift electron mobility (i.e., along the c-axis) of 4H- and 6H –SiC, is important to predict the performances of vertical power devices, and it can be deduced from the temperature dependence of the series resistance in current measurements on Schottky diodes fabricated on N-doped epilayers [77, 78]. The results are reported in figure 4b. A dependence of the mobility μ on the temperature as $T^{-2.1}$ suggests that lattice scattering and material defects are the main limiting factors to the carrier transport in vertical epitaxial devices [77]. It is interesting to observe that the results reported in figures 4a and 4b clearly show the strong anisotropy of the mobility in 6H-SiC. The fact that the electron mobility depends strongly on the crystallographic direction of travelling carriers is due to the anisotropic structure of conduction bands. In fact, theoretical calculations and experimental data carried out on 6H-SiC and 4H-SiC revealed that the anisotropy of the mobility values can be ultimately associated to the anisotropy in the effective masses [79,80].

3.2. Net doping concentration profiles at interfaces between epitaxial layers

The main requirements on SiC epitaxial layers for devices applications are the uniformity of the doping concentration together with the abruptness of the junctions between differently doped layers. Since N donors occupy substitutional positions in the C-sublattice, whereas Al acceptors in the Si-sublattice, an important parameter influencing the dopant incorporation during epitaxial growth is the C/Si ratio. Furthermore, since a background N concentration is always incorporated during the growth, p-type doping is obtained by overcompensation of N with Al. When characterizing the uniformity of epitaxial layers, as well as the abruptness of epitaxial p-n junctions, it is crucial to have information on the net doping concentration (N_A-N_D) profile, being N_A the acceptors and N_D the donors concentration. Commonly, secondary ions mass spectrometry (SIMS) is used to obtain the profiles of the atomic concentrations of the doping species. As an example, figure 5a reports the Al and N concentration profiles determined by SIMS analysis on a $n^{++}/p^{+}/n$ stack of 4H-SiC epilayers [81]. However, SIMS profiling is not able to provide information on the electrical activation of incorporated atoms and on the abruptness of the "electrical" junctions. Recently, scanning probe methods, like scanning capacitance microscopy (SCM), have been applied to address this topic. In SCM measurements, the derivative of capacitance with respect to voltage (dC/dV) is locally detected for each position of the atomic force microscope tip on the cross-sectioned sample surface. The amplitude of the SCM signal is related to the net dopant concentration, whereas its sign is related to the net doping type. Further details on SCM are given in appendix A.2. Figure 5b reports the SCM profile acquired on the same $n^{++}/p^{+}/n$ 4H-SiC multilayer. The comparison between the Al and N profiles determined by SIMS (figure 5a) and the SCM profile (figure 5b) indicates that the net doping concentration is uniform within each layer, whereas some fluctuation occurs close to the transitions from one layer to the other. The SCM profile allowed also estimating the abruptness of the transition regions between the differently doped layers, namely the width of the electrical junctions. In the present case, the transition region (indicated by circles in figure 5b) from the n^{++} ($N_D - N_A \approx 1\times10^{19}$ cm^3) to the p^{+} ($N_A - N_D \approx 1\times10^{18}$ cm^3) doped

layer and that from the p^+ to the n (N_D - $N_A \approx 2\times10^{17}$ cm^3) doped layer are both around 40-60 nm wide. Monitoring the nanoscale properties of the electrical junctions between epilayers can be particularly important to optimize the epilayers growth conditions and/or to understand the electrical behaviour of practical devices.

3.3. Local carrier concentration and mobility in ion-implanted SiC

As in the case of Schottky contacts, where the electrical characteristics are influenced by the surface preparation, also the fundamental transport properties in other interfaces are strongly affected by the processing steps employed for device fabrication. Among these processes, ion-implantation is the commonly adopted one to achieve selectively doped regions [2] or to locally tailor the electrical properties of SiC based devices [82]. In fact, due to the low diffusivity of dopants in SiC even at high temperatures, such locally doped areas cannot be obtained by conventional diffusion. Multiple implants at different energies and fluencies are commonly carried out to achieve the desired doping profile. During implantation, SiC substrates are typically kept at temperatures ranging from 300 to 600 °C, to avoid amorphization [83]. Furthermore, high thermal budgets are necessary to achieve the electrical activation of dopants and to recover the lattice damage. Typically, nitrogen (N) or phosphorous (P) implantations are performed to produce low resistivity, n-type SiC regions [84,85,86,87,88,89]. Implanted N atoms tend to be electrically inactive at N concentration higher than 2-5×10^{19} cm^{-3} due to the formation of precipitates during post-implantation annealing. However, high donor concentrations are required to reduce the resistivity of Ohmic contacts, as required in the source/drain areas in field-effect transistors (FETs). Under this point of view, P is used as an alternative donor species with ionization energies close to that of N donors [88]. Substitutional P atoms reside also at Si lattice sites. The critical concentration of 2-5×10^{19} cm^{-3} represents an upper limit for electrically active N donors, while P donors can be activated at concentrations above 10^{20} cm^{-3} [89].
While n-type doped layers with low sheet resistance have been obtained by annealing of N or P implanted layers at temperatures from 1300 °C [90,91] to 1800 °C [89], efficient p-type doping by Al and/or B implantation still remains a challenging task [92,93,94,95,96, 97]. This is due both to intrinsic reasons (the high ionization energies of acceptors [76]) and to the high thermal budgets required by the annealing to achieve the electrical activation of the implanted dopants (i.e. to bring them in the Si-sublattice substitutional positions) and to recover the lattice damage [98]. Different activation ratios (D_A/D_{Al}, with D_A the acceptors dose and D_{Al} the implanted Al dose) are reported in literature, depending on the implanted dose, on the target temperature during implantation, and on the post-implantation annealing conditions (temperature, ambient, etc.). In the case of Al implanted at 650 °C and annealed at 1670 °C, D_A/D_{Al} values ranging from 50% to 25% have been reported for Al concentrations increasing from 3×10^{18} to 10^{21} cm^{-3} [92]. Saks *et al.* [96], characterized Al implants in 4H-SiC at concentrations near solubility limit (~2×10^{20} Al/cm^3) as a function of the implant and anneal temperatures. For a typical implant temperature of 650°C, the authors obtained a ratio D_A/D_{Al} of ~6% – 35% upon post-implantation annealing from 1600 to 1750°C, respectively. For higher implant temperatures (1000°C) and for the same post-implantation annealing temperatures (1650-1750°C), the same authors reported significantly improved Al activatied fractions approaching the 100%. These results suggest that higher wafer temperatures during Al-implantation should be used during device fabrication, in order to operate with lower post-implantation annealing temperatures and to obtain an almost complete Al-activation. The temperature dependence of the hole mobility in Al-implanted sheets has been investigated in detail in Ref. [76]. As a matter of fact, defects introduced during the implant strongly affect both the electrical activation of Al and the hole mobility. The nature of these defects and their evolution during annealing has been investigated by structural and spectroscopic analyses [83,99,100]. In particular, some of those defects, arising from the Al-implant, exhibit a donor like behaviour and compensate the acceptor centers present in the material. These compensating centers strongly affect the transport properties (free hole concentration and mobility) in Al-implanted SiC layers. The density of the compensating centers (N_D) as well as the density of active dopants, are typically obtained fitting temperature dependent measurements of carrier concentration (by Hall effect) with the neutrality equation. These densities are average values over the implanted thickness. However, since the implanted layers are typically obtained from the overlap of several implantation profiles performed with different projected ranges, the integral damage depth profile is expected to be non-uniform and, consequently, also the concentration of compensating centers is

expected to be dependent on the depth. Recently, the depth distributions of the compensating centers (N_D (cm^{-3})) and that of the acceptor (N_A (cm^{-3})) in the implanted sheet have been determined by scanning probe microscopy [101]. SCM was used to obtain the net doping profile (N_A-N_D) [102,103], while the resistivity (ρ) profile was obtained by scanning spreading resistance microscopy (SSRM) [101] (details and references for SSRM can be found in appendix A.3). The measured ρ values are related to the local hole concentration p and to the drift mobility μ_p, by the relation $\rho=1/(qp\mu_p)$, where q is the electron charge. On the other hand, the local hole concentration is related to the local densities N_A and N_D by the neutrality equation:

$$p + N_D = \sum_{n=1}^{2} N_{A,n}\left[1+\frac{p}{gN_V}\exp\left(\frac{\Delta E_{A,n}}{k_B T}\right)\right]^{-1} \quad (3)$$

where $N_{A,1}$ and $N_{A,2}$ are the concentrations of the two Al acceptor levels (i.e. $N_A=N_{A,1}+N_{A,2}$), $\Delta E_{A,1}$ and $\Delta E_{A,2}$ are the ionization energies of those levels, g is the degeneracy factor and N_V is the effective density of states in the valence band. Inserting the measured local values of ρ and N_A-N_D in these equations, the profiles of N_A and N_D and the drift mobility (μ_p) profile in the implanted layer were determined [101]. Such depth resolved profiles are reported in figure 6 for 4H-SiC implanted at 400 °C with Al ions at various energies in the range 40-550 keV and subjected to annealing at three different temperatures, 1400 °C (a), 1500 °C (b), and 1650 °C (c) for 30 minutes in Ar+SiH_4 ambient. The multiple implants yield a ~700 nm thick box-like Al profile (~1×10^{18} cm^{-3}), but the profiles of substitutional Al (N_A) and of compensating centers (N_D) are strongly non-uniform with respect to depth. After the annealing at 1400 °C, N_D is only slightly lower than N_A both in the surface region and in the tail of the profile, thus resulting in a very low net doping concentration and a very high resistivity. After the annealing at 1500 °C and 1650 °C, N_D becomes a smaller fraction of N_A (except in the near-surface region) and this is reflected in an overall decrease of the sheet resistance. In general terms, the thermal evolution of the electrical activation in Al-implanted 4H-SiC is the result of a counterbalance between the decrease in the percentage compensation and the increase in the acceptor concentration [101]. The local hole drift mobility μ_p (figure 6d) in the implanted layer decreases with increasing annealing temperatures, due to the increase of the acceptor concentration N_A.

Typically, as extensively reported in literature, conventional annealing techniques involving horizontal or vertical furnaces (like the results shown in figure 6), lamp annealing systems, etc., are used to achieve electrical activation in ion-doped SiC. Recently, ultra-rapid solid-state microwaves annealing techniques, operating up to 2000°C, have been proposed to increase the electrical activation of ion-implanted SiC and to limit the step bunching phenomena [104]. However, these methods still need significant technical improvement to be successfully employed on large area SiC substrates.

4. Interface transport properties in the SiO_2/SiC system

The progress of SiC-based power switching devices has been fast developing in the field of unipolar devices for blocking voltages in the range 600 V – 2000 V. Nowadays, Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) are the power-switching devices in SiC which are predominantly under development, together with Junction Field Effect Transistors (JFETs). In fact, the performances of SiC MOSFETs in terms of R_{on} are still far from the theoretical expectations, due to some limitations related to the carrier transport at the SiO_2/SiC interfaces. On the other hand, JFETs have been proposed as normally-on devices. Although normally-on devices may not be a problem for the most of applications, in some cases normally-off devices are mandatory to guarantee for intrinsic safety conditions.

The complete fabrication of a vertical MOSFET requires ion-implantation for the formation of the n-type source-drain and of the p-type body regions. As discussed in the previous section, these processes involve high-temperature annealing (1400-1800°C) for electrical activation of the ion-species, which considerably impact on the morphological and electrical properties of the surface and interfaces in the proximity of the channel.

The surface morphology of 4H- and 6H-SiC is typically strongly modified by the high thermal budgets necessary for the electrical activation of implanted dopants. At temperature >1400 °C preferential evaporation of Si from the surface starts to occur. Furthermore, a peculiar roughening of the surface is visible, with the formation of

large terraces parallel to the original miscut angle ("step bunching"). This step bunching is greatly enhanced in sample regions subjected to high fluence ion-implantation [105,106]. As an example, in figure 7, surface morphology images measured by atomic force microscopy (AFM) are reported in the case of 4H-SiC as-implanted with Al fluence of 1.2×10^{15} cm^{-2} (figure 7a). The increase of the surface roughness after annealing at 1650 °C (figure 7b) for 30 min is evident, as can be seen also from the reported values of the root mean square (RMS) roughness.

The presence of a step bunching can have an influence on some electrical devices parameters, like the contact resistance and the channel channel conductance in SiC MOSFETs. As an example, Lee *et al.* [107] observed an anisotropy of the drain current in 6H-SiC MOSFETs in the presence of a significant step bunching on the surface oriented along the [1-100] direction. The lower drain current observed when the channel was fabricated with an orientation perpendicular to the step bunching (i.e. along the [11-20] direction) was explained by the different interface roughness appearing to the carriers in the two directions.

Several methods are adopted to reduce roughness, like the use of a graphite capping layer before annealing [108, 109,110] or chemical-mechanical-polishing (CMP) after annealing [111]. As an example, figure 7c shows the morphology of 4H-SiC implanted with Al fluence of 1.2×10^{15} cm^{-2} and annealed at 1650 °C, after encapsulation in a graphite capping layer. The reduction of the roughening in comparison with 4H-SiC annealed under identical conditions without the capping layer (see figure 7b) is evident. In spite of the beneficial effect on the surface roughness of using a capping layer during annealing, it is still not clear if a better morphology systematically results also in an improvement of the channel mobility [112].

Beyond the need of a nanometric control of the surface and interface roughness before the gate-oxide formation (which can be achieved e.g. by CMP, capping layers, sacrificial oxidation after activation annealing, etc.), the present serious drawback, hindering the carrier transport in MOS-based SiC devices seems to be the high density of charged states at SiO_2/4H-SiC interfaces [113,114,115]. Several works in the last decades have correlated the microstructure of the SiO_2/SiC interfaces with the electrical properties of MOS-based devices. Basing on these studies, it is now commonly accepted that the high density of interface traps D_{it}, particularly those located close to the conduction band edge, is responsible for a low effective electron channel mobility in SiC MOSFETs.

Concerning the oxide microstructure, it is known that thermal oxidation of SiC results in the formation of SiO_2 and CO, which diffuses out of the bulk oxide layer. However, residual carbon remains at the interface and can be detrimental for the carrier transport properties in the inversion layer [116]. Hence, the origin of charged traps at the SiO_2/SiC interface has been associated to interface defects, which are likely related to the presence of residual carbon (graphite-like films, carbon clusters, ….), to silicon suboxide bonds or oxide defects with energy levels inside the SiC bandgap [117, 118]. The compositional profile of the thermal oxide on SiC, studied by Vathulya *et al.* [119] using angle resolved x-ray photoelectron spectroscopy, indicated a direct correlation between the overall carbon content in the oxide and the density of interface states determined by C-V measurements. Accordingly, also Afanas'ev *et al.* [120] found that the interface states at the SiO_2/SiC interface can be associated to the presence of carbon atoms and that removal of the carbon species (i.e., by an UV pre-oxidation treatment) is beneficial to reduce the interface state density and fixed charges in the MOS capacitors on SiC. A further direct evidence of an accumulation of carbon at the interface between thermally grown SiO_2 (formed by wet oxidation at 1100°C) and SiC was given by Chang *et al.* [121] combining transmission electron microscopy (TEM) with electron energy loss spectroscopy (EELS). The thickness of these C-rich regions was estimated to be 10–15 Å. The absence of carbon at the interface with a deposited oxide on SiC suggested that the carbon accumulation was the result of the oxidation process.

The most reliable approach to partially overcome the problem of a low channel mobility in SiC MOSFETs is to employ post-oxidation annealing processes of the gate oxide in nitrogen-rich ambient (N_2O, NO,..) in the temperature range 1100-1300°C [114]. In fact, only after such nitridation annealing treatments of the gate oxides values of channel mobility in the range of 30-50 $cm^2V^{-1}s^{-1}$ could be achieved [114]. As an alternative to the nitridation, other methods have been also studied with the aim to reduce the interface states density in SiC MOSFETs. As an example, ion-implantation has been proposed to introduce nitrogen at the SiO_2/SiC. In fact, performing a thermal oxidation after N-implantation of the SiC epilayer leads to a reduction of the interface state density D_{it} in MOS capacitors [122], and to an improvement of the mobility in 4H-SiC MOSFETs [123,124]. However, implantation-induced damage remains a serious limitation for the illustrated

method. Higher values of the channel mobility (up to 154 $cm^2\ V^{-1}\ s^{-1}$) were achieved using oxidation processes performed in alumina furnaces [125], but the existence of mobile charge in these oxides prevents practical use of this method for device manufacturing.

The role of nitrogen in the reduction of interface traps density is quite complex and several explanations have been given on the basis of both structural and electrical analysis performed.

The first experiments on nitridation of oxides on SiC were presented by Li *et al.* [126], who observed a reduction of the interface state density at SiO_2/6H-SiC interfaces after an annealing in NO, with respect to a rapid thermal oxidation process in O_2. The beneficial impact of the NO process on the interface state density was generically attributed to a reaction of nitrogen with the silicon dangling bonds during the oxidation. The established improvements of electrical properties of the NO annealed oxides were better explained by Jamet and Dimitrijev [127], who studied the nitridation (in N_2O and NO) by either annealing or direct growth of gate oxides on 4H SiC. In particular, x-ray photoelectron spectroscopy (XPS) and SIMS depth profiles of nitrogen, revealed a "clean" SiO_2/SiC interface after NO and N_2O processes, while interfaces annealed in Argon exhibited the presence of complex suboxides and oxide–carbon compounds. Furthermore, for nitrided oxides, XPS showed that the complex suboxide and oxide–carbon bonds were removed, thus being accompanied by the formation of strong $Si \equiv N$ bonds and the significant reduction of the spectral intensity of $C–C$ bonds [127]. Mc Donald *et al.* [128] studied the reduction of the interface states density by NO-nitridation, observing a saturation effect upon a nitrogen incorporation level of 2.5×10^{14} cm^2. The presence of such saturation is consistent with a model of the interface in which large clusters composed of an excess of interfacial carbon or silicon are subsequently passivated (and dissolved) by the indiffusing nitrogen, with the formation of strong $C\equiv N$ and $Si\equiv N$ bonds. Finally, according to the more recent work by Wang *et al.* [129] the action of nitrogen at the interface can assimilated to that of a positive oxide charge, neutralizing the negatively charged acceptor-like traps commonly present on 4H-SiC surfaces and forming charge dipoles at the SiO_2/4H-SiC interface.

Recent works by Zheleva *et al.* [130] and by Biggerstaff *et al.* [131], based on a nanoscale characterization using high resolution TEM and EELS, definitively correlated the existence of a "transition layer" on both sides of the SiO_2/SiC interface with the electrical properties of the SiO_2/SiC interface. In particular, the structural degradation (amorphization) observed in the top few atomic layers of SiC and the presence of this interfacial transition region was associated to changes in the SiO_2 and SiC stoichiometry. A detailed chemical analysis indicated the formation of a silicon-oxycarbide layer (SiC_xO_y), where the layer on the SiO_2 side contains C, whereas the top layer of SiC contains excess C and small amounts of O [130]. This nanometric transition layer is something inherent to the SiO_2/SiC interface, as it is always present at the interface independent of the processing condition of the oxide. However, the thickness of the transition layer can be partially reduced, even if not completely removed, by N incorporation by post-annealing treatments [132]. It is worth noting that the width of this transition layer is strongly correlated with the values of the effective channel mobility. Figure 8 reports the peak effective channel mobility and the interface trap density, measured on fully processed 4H-SiC MOSFET devices [131], as a function of the transition layer thickness. As can be seen, the channel mobility decreases almost linearly with increasing the thickness of this transition layer. Notably, the increase of the transition layer thickness is also correlated to the increase of the interface trap density D_{it}.

Another important concern for dielectric/SiC interfaces is the long-time electrical reliability of the dielectric itself. Even if the used materials can be the identical in SiC and Si MOS systems (e.g., SiO_2), due to the large band gap of SiC the conduction band offset between the SiC substrate and SiO_2 is smaller than in the case of the SiO_2/Si system. Hence, similar MOS systems in SiC typically exhibit a much higher tunnelling current than in Si under similar applied electric fields. This latter, in turn, can contribute significantly to the charge to breakdown, limiting the temperature performance of the oxide. Furthermore, as mentioned before, the oxidation of SiC involves the oxygen in-diffusion and the subsequent binding of O atoms to the Si atoms. Simultaneously, residual C can be released either as CO gaseous compounds at the oxide surface, otherwise form graphite, or interstitial defects at the interfaces [116,117,118,119,120,121,130] according to a balance between the oxidation rate and the C solubility. Considering these intrinsic differences, it is important to accurately assess the reliability of the SiO_2/SiC system at a nanoscale level, in order to establish a comparison (analogies and differences) with the case of Si, i.e., whose technology for MOSFETs devices is already well consolidated. In this context, Fiorenza *et al.* [133,134] investigated the reliability of thermal oxide grown on 4H-SiC, determining the Weibull statistics mapping the oxide local failure (pre-breakdown hot-points) at a nanoscale by using an

original C-AFM based method to provide a local voltage stress. While for thinner thermal oxides (up to 5-7 nm) an intrinsic behaviour according to the ideal percolation model in SiO_2 was found, significant deviations from the theory were observed in the case of thicker (>10 nm) SiO_2 layers. Since the Weibull theory includes only the defects inside the oxide, this behaviour can be related to the presence of C inside the SiO_2 layer, i.e., namely to the previously described transition layer. In particular, the presence of a defective transition region in the oxide, whose thickness depends on the oxidation conditions and increases for thicker thermal oxides [131, 135], can enhance the intrinsic defect formation probability.

All the above recent insights gained on the nanoscale electro-structural properties of the SiO_2/SiC interfaces are the fundamental starting point to predict the carrier scattering in the inversion layer and the breakdown phenomena, and, eventually, to approach with novel solutions (new dielectrics, new oxidation procedures, etc.) the present drawbacks in SiC MOSFETs.

5. Interfaces considering different SiC polytypes

As pointed out in the previous sections, to date the vast majority of SiC devices and applications have been implemented using the two stable hexagonal polytypes (4H, 6H). However, several properties make 3C-SiC unique among SiC polytypes, such as high low-field mobility, low ionization energy for the nitrogen donor levels, isotropic electrical and thermochemical properties, etc.[136]. Furthermore, 3C-SiC is expected to give a better SiO_2/SiC interface in terms of inversion channel mobility [137,138]. In fact, since the bottom of the conduction band in 3C-SiC is about 0.9 eV lower than in 4H-SiC, the near-interface traps located close to the bottom of the conduction band in 4H-SiC, should be inactive in 3C-SiC, leading to higher inversion channel mobility [113,114].

Unfortunately, the possibility to grow high-quality single crystalline 3C-SiC films on large area Si substrates is strongly limited by the high lattice mismatch (20%), and the mismatch in the thermal expansion coefficients (8%) between 3C-SiC and Si, leading to interfacial strain during the processes of growth and cooling down. Hence, a large variety of defects are formed both at the interface and in the films, as misfit dislocations, stacking faults, twinning rotations, voids, anti-phase domains, etc. [139], making this material unsuitable for devices fabrication. Due to these limitations, for a while 3C-SiC has been defined as the “forgotten polytype” [136].

A significant progress was achieved during the last few years, when single crystalline 3C-SiC material with a lower defect density, obtained starting the growth process from an “undulant” Si substrate, has been demonstrated, showing a potential impact for vertical power devices onto large-diameter wafers [140]. As a matter of fact, using such “free-standing” material, values of channel mobility up to 260 cm^2/Vs could be obtained in 3C-SiC vertical MOSFETs [141]. Considering the higher channel mobility with respect to 4H-SiC and the recent progresses in the growth of large area free standing substrates of good quality, 3C-SiC has been indicated as the polytype of choice for medium voltage (600 V to 1200 V) vertical MOSFETs, in spite of the lower critical electric field of this polytype [142].

In principle, a combination of 3C-SiC with different polytypes (like the hexagonal ones) is particularly interesting because their different electronic structures could allow the spatial confinement of carriers in quantum wells. However, for many years the formation of such heterostructures has been limited by the high defect density resulting from the heteropolytypical growth. A critical problem in the growth of 3C-SiC/α-SiC heterostructures is the occurrence of incoherent twin boundaries, i.e., the so called double positioning boundaries (DPB). DBPs are formed when 3C-SiC islands of different orientation (rotated by 60º with respect to each other) nucleate and subsequently expand and meet during growth [143]. Hence, the growth of SiC heteropolytypic structures requires well definite conditions (i.e., temperature, C/Si ratio, etc.) in order to control the crystalline quality of each polytype forming the structure.

The first demonstration of good quality heteropolytypic SiC structures was given by Fissel [144] using solid-source molecular beam epitaxy. Pseudomorphic 3C–SiC layers were grown on α-SiC; they were unintentionally doped (as deduced by optical measurements) and nearly free of twins. Furthermore, the growth of other 4H/3C/4H heterostructures was also demonstrated, whose optical properties could be explained on the basis of theoretical calculations of the band structure of such systems [145,146].

Recently, theoretical and experimental works on heterojunctions formed between cubic (3C) and hexagonal (6H, 4H) SiC, opened new prospects for 3C-SiC for high-frequency devices. In particular, the formation of a two-dimensional electron gas (2DEG) at the heterointerface has been theoretically predicted by Polyakov and Schwierz [147], by numerical self-consistent solving the Schrödinger-Poisson equations in the 4H/3C SiC and 6H/3C SiC systems. The results of these calculations predicted the formation of a 2DEG with a sheet carrier density n_s in the range of 0.8-1.3×10^{13}cm^{-2}, i.e., of the same order of magnitude of the values found in GaN-based heterojnctions, thus being particularly interesting for fabricating high electron mobility transistors (HEMTs) using a complete SiC technology.

Basing on these theoretical predictions, the electronic properties of SiC heteropolytype junctions, in which a 3C-SiC layer was grown either on the C- or on the Si-terminated face of hexagonal SiC, were recently investigated by Chandrashekhar *et al.* [148,149] using capacitance-voltage (C-V) and Hall measurements. Following these studies, a 2DEG was experimentally observed for the first time in 3C-SiC/6H-SiC (C-face) heterostructures [150]. Figure 9 shows the electron distribution at the heterointerface as a function of the depth, determined by C-V analysis. The peak located at a depth of 32 nm, i.e. the position of the 3C-SiC/6H-SiC interface, indicates the formation of the 2DEG. The peak electron density is as high as 4×10^{19} cm^{-3}, giving a sheet charge density of 2.5×10^{12} cm^{-2}. A schematic band diagram of the 3C-SiC/6H-SiC heterointerface is also reported in the inset. It must be pointed out that this result could be achieved thanks to high quality 3C-SiC heteroepitaxial layers grown on the C-face of a 6H-SiC buffer layer. However, typically 3C-SiC grown onto hexagonal substrates (6H, 4H) is characterized by a large variety of defects, like misfit dislocations, stacking faults, double positioning boundaries (DPBs) and microtwins [143]. Clearly, in the presence of such a large variety of defects, the control of metal/3C-SiC interfaces becomes critical.

In this context, to fully exploit the potentiality of cubic SiC for devices, the development of reliable Schottky contacts, with a high barrier height and low leakage currents, still represents a big challenge. Such contacts, in fact, should be required for modulating the sheet charge density inside a 2DEG channel in a transistor. The typical values of the SBH on 3C-SiC however are in the range of 0.4–0.7 eV (see table 2), i.e., below the theoretical values expected considering the 3C-SiC band-gap. This long standing fundamental topic was recently addressed by Eriksson *et al.* [151], who analyzed the electrical characteristics of Au/3C-SiC Schottky barriers as a function of contact area, establishing a correlation between the Schottky barrier and the material defects. Figure 10a reports the I-V characteristics acquired by means of C-AFM on Schottky contacts fabricated on a region containing DPB or on a DPB-free region. As can be seen, DPBs are “killer defects” for metal/3C-SiC Schottky contacts, since in the presence of a DPB the Au/3C-SiC contact exhibit an Ohmic rather than a rectifying behaviour. Furthermore, restricting the study to DPB-free regions, I-V measurements showed an increase of the SBH with decreasing the contact area, as reported in figure 10b. In particular, by reducing the contact size down to 5 μm in diameter, the value of Φ_B becomes closer to the ideal barrier height of Au on 3C-SiC [151]. An analytical model to describe the dependence of Φ_B on the defect density was proposed, and fits well the experimental results (see figure 10b). Details on this model are reported in Ref. [151]. These results suggest that, beyond the surface conditions (chemistry, interface index, …), specific polytype defects also play a crucial role in the formation of Schottky barriers on 3C-SiC. Hence, with the present available material quality, the main applications of 3C-SiC remain in the field of sensors and micro electro mechanical systems (MEMS).

6. Summary and Outlook

In this paper, some relevant nanoscale aspects of carrier transport in SiC materials and devices were reviewed. They are playing an increasing importance along with the crucial role provided by interfaces in current SiC technology. Clearly, although the significant progresses achieved in the last years in the material quality and device processing opened significant perspectives for SiC, several scientific open issues related to the transport properties still remain. Hence, for a further development of SiC technology, significant efforts in fundamental research are required to better understand the transport phenomena, where a nanoscale approach appears to be mandatory.

The lateral inhomogeneity of Schottky barrier is mainly associated to the device processing even if the material quality can still play a significant role. The degree of homogeneity of Schottky barriers in SiC, that is critical for a family of devices, can be significantly improved by employing appropriate metallization schemes,

post-deposition annealing or sacrificial oxidation steps. The use of nickel silicides as Schottky metal, having a higher reproducibility of the electrical characteristics, can be an interesting alternative to other metals for high temperature applications or radiation and/or light detectors.

Profiling carrier concentration and mobility is fundamental to understand the overall electronic transport properties of either epitaxial or ion-implanted SiC materials. Particularly interesting for devices is the case of ion-implanted material, in which the carrier concentration and mobility can be locally dependent on the ion-induced damage, e.g., by the precipitation of dopants in electrically inactive complexes, or by the presence of defects acting as compensating centers. The high temperatures required for implant activation lead to a high surface roughness and significant step bunching. In this sense, the nanoscale control of surface and interface properties by novel encapsulation and/or polishing techniques, and the development of ultra-rapid annealing steps are current subjects of investigations.

In the case of SiO_2/SiC interfaces, crucial for MOSFETs devices, the channel mobility is typically limited in the range 30-50 cm^2/Vs due the presence of a high interface state density. The high interface states density is correlated to the existence of a transition layer, which is intrinsic in the nature of the SiO_2/SiC interface. The control of surface and interfaces during annealing and gate-oxidation is fundamental, even if a real technological breakthrough in the nanoscale control of SiO_2/SiC interface state density seems to be required to increase the channel mobility values. The use of other dielectric/SiC interfaces and/or non-conventional oxidation techniques should be considered to overcome the present physical limitations of the SiO_2/SiC system.

Finally, due to the crystalline quality of the available SiC materials, applications in power electronics are still restricted to the hexagonal polytypes, where the use of cubic 3C-SiC seems at the moment to be limited to the field of sensors and MEMS, in spite of the promising results obtained recently on heteropolytype 3C-SiC/6H-SiC interfaces.

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Appendix

A.1. Schottky barrier height mapping with nanoscale resolution

Ballistic electron emission microscopy (BEEM) [51], the first demonstrated method for local mapping of metal-semiconductor Schottky barrier height (SBH), is based on the tunnel injection of hot electrons from the reverse biased tip of a scanning tunneling microscope (STM) to the metal film. If the film thickness is comparable or lower than the electron mean free path in the metal, a significant fraction of the hot electrons propagate ballistically through it. When a bias higher than a threshold value $V_{th} = \Phi_B/q$ (with Φ_B the SBH and q the electron charge) is applied to the tip, the ballistic electrons are able to overcome the barrier, propagate in the semiconductor and a current is collected at the backcontact. A SBH map is obtained by measuring the threshold voltage for each tip position on the metal. Although BEEM proved a high spatial and energy resolution, it suffers the intrinsic limitations of STM. In fact, since the injected tunnel current intensity is used also in the tip-height control feedback, BEEM cannot be applied to samples containing both conductive and insulating regions on the surface. Moreover, the BEEM current, i.e., the fraction of the injected current propagating ballistically in the metal film, is typically very low (in the order of the pA, with a high noise level).

Lately, an alternative approach based on conductive atomic force microscopy (C-AFM) was demonstrated [62], which overcomes some of the BEEM limitations. Scanning a forward biased C-AFM tip in contact on an ultra-thin (< 5 nm) metal film, current flows only through a very localized region (in the order of the tip diameter) of the macroscopic metal-semiconductor contact, i.e., a "nano-Schottky diode" is formed point by point. This localization of the current is due the electrons propagating ballistically in the direction perpendicular to the ultra-thin metal film, whereas they encounter a high-resistivity in the direction parallel to the interface. For such measurements, the back side Ohmic contact of the semiconductor is connected to a current amplifier enabling the detection of currents on the nA scale with a pA sensitivity. In this way, two-dimensional maps of the SBH can be extracted from the current-voltage characteristics collected for different tip positions. The lateral resolution of the method is 10-20 nm and the energy resolution is in the 0.1 eV range.
For some specific applications, the C-AFM-based approach is more suitable than BEEM. In fact, since it is based on "contact mode" AFM, the feedback for the tip height position is based on the cantilever deflection. This latter allows to characterize also samples containing both conductive and insulating regions on the surface. Moreover, the collected current values are typically in the order of the nA, i.e. 2-3 orders of magnitude higher than BEEM currents.

A.2. Scanning Capacitance Microscopy (SCM)

Scanning capacitance microscopy (SCM) is based on the use of a conductive AFM tip, connected to a high sensitivity capacitance sensor. The probe is scanned in contact mode on the surface of a semiconductor coated by an ultra-thin (a few nm) insulating film, thus forming a nanometric metal-insulator-semiconductor (nanoMIS) device. During the measurement, the sample is biased by a DC bias and a high frequency (~100 kHz) small amplitude AC bias. A high sensitivity capacitance sensor connected to the probe measures the capacitance variations induced in the nanoMIS structure by the modulating AC bias. Due to the nanoscale dimensions of the system, these capacitance variations are in the order of the attoF (10^{-18} F) or sub-attoF. The capacitance sensor in the state of the art SCM equipments is based on the RCA video disc capacitive-pickup circuitry, working at 900-1000 MHz with a sensitivity from ~10^{-19} to ~10^{-21} F×Hz$^{-1/2}$. Since the stray capacitances are several orders of magnitude larger (in the order of pF) than the tip/sample capacitance, the small capacitance variations of the "nanoMIS" system are extracted filtering the sensor output by a lock-in amplifier, locked at the modulating AC bias frequency. The lock-in output is an arbitrary units (a.u.) signal proportional to the derivative of capacitance with respect to voltage (*dC/dV*) of the nanoMIS.
A SCM map is formed by a 2D array of dC/dV values measured at the fixed DC bias applied to the sample. The DC bias is usually fixed on the peak of the dC/dV curve, corresponding to the flatband voltage condition of the nanoMIS. The capacitance variations are mainly related to the local net doping concentration underneath the tip. According to the MIS theory, the *dC/dV* sign is negative for p-type doped and positive for n-type doped semiconductors, thus enabling to distinguish between different type doped areas. Moreover, the absolute value of the dC/dV curve peak decreases monotonically with increasing the net doping concentration concentration. The relation between the *dC/dV* signal and the net doping concentration is typically experimentally determined using dedicated calibration samples [152].
Both the case of Si and of SiC [103], a high sensitivity (~10%) on a wide doping concentration range (from ~10^{15} to ~10^{20} cm^{-3}) has been demonstrated on dedicated p-and n-type calibration samples. This range is limited at the highest concentrations (>10^{20} cm^{-3}), due to the very small capacitance variations, i.e. no depletion region is formed in the semiconductor. For the lowest concentrations (<10^{15} cm^{-3}) the sensitivity is limited by oxide fixed and trapped charges and oxide-semiconductor interface states. The nanometric depth resolution of this method has been demonstrated on dedicated Si and SiGe test structures [152,153].

A.3. Scanning Spreading Resistance Microscopy (SSRM)

In scanning spreading resistance microscopy (SSRM) a hard conductive AFM probe (typically a diamond coated tip) is scanned in contact mode across the sample, while a DC bias is applied between an Ohmic contact on the back-side of the sample and the tip. The current flowing between the tip and the back-side is measured using a logarithmic current amplifier with a typical range from 1 pA to 1 mA. The total measured resistance R in SSRM

experiments includes the resistance of the probe R_{tip}, the tip-semiconductor contact resistance $R_{contact}$, the spreading resistance R_{spread} encountered by the current flowing from the nanometric contact to the semiconductor, the sample series resistance R_{series} and the back-contact resistance $R_{back.}$ When a pressure in the order of GPa (corresponding to a μN force on a contact surface of ~10 nm radius) is applied between the conductive tip and the semiconductor sample, a very stable electrical contact is tipically established. In fact, the native oxide on the semiconductor surface is pushed through and, in same cases (like for Si), the large pressure can be responsible of local changes of the electronic properties (from a semiconducting to a conducting phase), due to elasto-plastic or even fully plastic deformations of the in indented sample region. Under these conditions, the measured resistance R is dominated by the spreading resistance contribution R_{spread}, which, in the first approximation, is linearly related to the local semiconductor resistivity ρ by $R_{spread}=\rho/4a$, being *a* the "effective contact radius". In the practical cases, however, this relation is experimentally determined using dedicated calibration samples. The resistivity is, in turns, related to the carrier concentration n and to the carrier mobility μ as $\rho=1/(qn\mu)$.
To date, SSRM has been applied both to Si [154], Ge, SiGe [153], III-V semiconductors (GaAs, InP) [155] and SiC [101]. Similarly to SCM, SSRM benefits from an extremely large dynamic range (from 10^{15} to 10^{20} cm^{-3}). This range is limited at the high carrier concentration ($>10^{20}$ cm^{-3}) by the presence of the diamond probe resistance in series with the spreading resistance. In low doped areas ($<10^{15}$ cm^{-3}), the SSRM measurements are disturbed by the presence of surface charges.

Table 1. Physical properties of the most common SiC polytypes. For comparison, the properties of Si are also reported.

Property	**Si**	**3C-SiC**	**6H-SiC**	**4H-SiC**
Bandgap (eV)	1.12	2.35	3.08	3.28
Breakdown field E_B (MV/cm) (at $N_D=5\times10^{15}cm^{-3}$)	0.3	1.5	2.2	2.3
Intrinsic carrier concentration n_i (cm^{-3}) (at T=300K)	1×10^{10}	1.5×10^{-1}	1.6×10^{-6}	5×10^{-9}
Electron mobility μ_n (cm^2/Vs)	1350	900	370	800
Hole mobility μ_h (cm^2/Vs)	480	40	80	120
Saturated electron velocity v_s (10^7 cm/s)	1	2	2	2
Thermal conductivity κ (W/cmK)	1.5	4.9	4.9	4.9
Dielectric constant ε	11.8	9.6	9.7	9.7
Electron affinity χ_s (eV)	4.05	3.8	3.3	3.1

Table 2. Schottky Barrier Height values for different metals on n-type 3C-SiC, 6H-SiC and 4H-SiC. The values were determined by I-V measurements in Schottky diodes. For the hexagonal polytypes, they are referred to the Si-terminated face.

3C-SiC	SBH (eV)	Ref.
Ti	0.40 eV	[16]
Ni	0.56 eV	[16]
Au	0.47 eV	[17]
Au	0.67 eV	[16]
Pt	0.85 eV	[18]
6H-SiC	SBH (eV)	Ref.
Al	0.26	[19]
Ag	0.83	[20]
Ti	0.76	[21]
Ti	0.93	[22]
Ti	0.96	[23]
Ni	1.08	[23]
Ni	1.24	[19]
Ni	1.29	[24]
Ni_2Si	1.39	[22]
Cu	1.18	[23]
Au	1.41	[23]
Pd	1.21	[25]
Pt	1.04	[26]
4H-SiC	SBH (eV)	Ref.
Mo	1.04	[27]
Mo	1.11	[28]
W	1.17	[28]
Ta	1.10	[29]
Ti	1.23	[22]
Ti	1.27	[30]
TiW	1.22	[31]
Ni	1.32	[32]
Ni	1.44	[33]
Ni_2Si	1.60	[34]
Au	1.73	[35]
Pt	1.39	[36]

FIGURE CAPTIONS

Figure 1. Schottky barrier height Φ_B as a function of the metal work function Φ_m for different metals on 3C-SiC (open squares), 6H-SiC (solid circles) and 4H-SiC (open triangles). The values of Φ_B (taken from Table 1) are determined from I-V measurements of Schottky diodes on n-type SiC. For the hexagonal polytypes, the Schottky contacts were formed on the Si-face.

Figure 2. Ideality factor n (solid circles) and Schottky barrier height Φ_B (open triangles) as a function of measurement temperature for Ni_2Si/4H-SiC Schottky contacts. The inset shows the correlation plot Φ_B vs n. The extrapolation of the barrier height at n=1 gives the values of the "homogeneous" Ni_2Si/4H-SiC barrier, Φ_{B0}=1.69 eV (data from Ref. [34]) .

Figure 3. Distribution of the local Schottky barrier height values (determined by C-AFM) for Au/6H-SiC contacts, with and without an interfacial non-uniform oxide layer (data from Ref. [62]) .

Figure 4. Temperature dependence of the electron mobility of lightly N doped (3×10^{15} - 1×10^{16} cm^{-3}) 6H- (solid circles) and 4H-SiC (open triangles). (a) In-plane mobility by Hall effect measurements (data from Refs. 73 and 74) and (b) c-axis (vertical) drift mobility by I-V measurements on Schottky diodes (data from Refs. [77] and [78])

Figure 5. (a) Profiles of the concentrations of Nitrogen (solid line) and Aluminium (dashed line) atoms in a $n^{++}/p^{+}/n$ stack of 4H-SiC epilayers measured by secondary ions mass spectrometry (SIMS). (b) Scanning capacitance microscopy profile (SCM) acquired on a cross section of the same sample, giving information on the net doping concentration and the doping type. The variations of the doping at the interfaces between the epilayers are marked by the cricles (data from Ref. [81]).

Figure 6. (a-c) Concentration profiles of acceptors N_A (solid lines) and compensating donors N_D (dashed lines) for the samples annealed at 1400 °C, 1500 °C and 1650 °C for 30 min. (d) Hole mobility profile determined from the N_A and N_D profiles for the samples annealed at the three temperatures, 1400°C (dot line), 1500°C (dashed line) amd 1650°C (solid line).

Figure 7. AFM surface morphology on Al implanted 4H-SiC (fluence 1.2×10^{15} cm^{-2}). As-implanted (a), annealed at 1650 °C for 30 min without (b) and with a graphite capping layer (c). The measured surface root mean square (RMS) roughness is also reported. (data extracted from Refs. [106,110]).

Figure 8. Inversion channel mobility (μ) (solid squares) and interface traps density (D_{it}) (open triangles) as a function of the transition layer thickness. The parameters were determined from the characteristics of 4H-SiC MOSFETs (Data extracted from Refs. [130,131]).

Figure 9. Electron density as a function of the depth in 3C-SiC/6H-SiC heterojunction. The presence of a peak located at a depth of around 32 nm indicates the formation of a 2DEG (data from Ref. [150]). The inset shows a schematic band diagram of the 3C-SiC/6H-SiC system.

Figure 10. (a) I-V curves of Au/3C-SiC Schottky contacts formed on a region containing double position boundaries (DPB) (open squares) or on a region without DPBs (DPB free) (solid triangles). (b) Schottky barrier height of Au/3C-SiC contacts as a function of the contact area, determined in DPB-free regions. The continuous line is fit of the experimental data with the theoretical model discussed in detail in Ref. [151].

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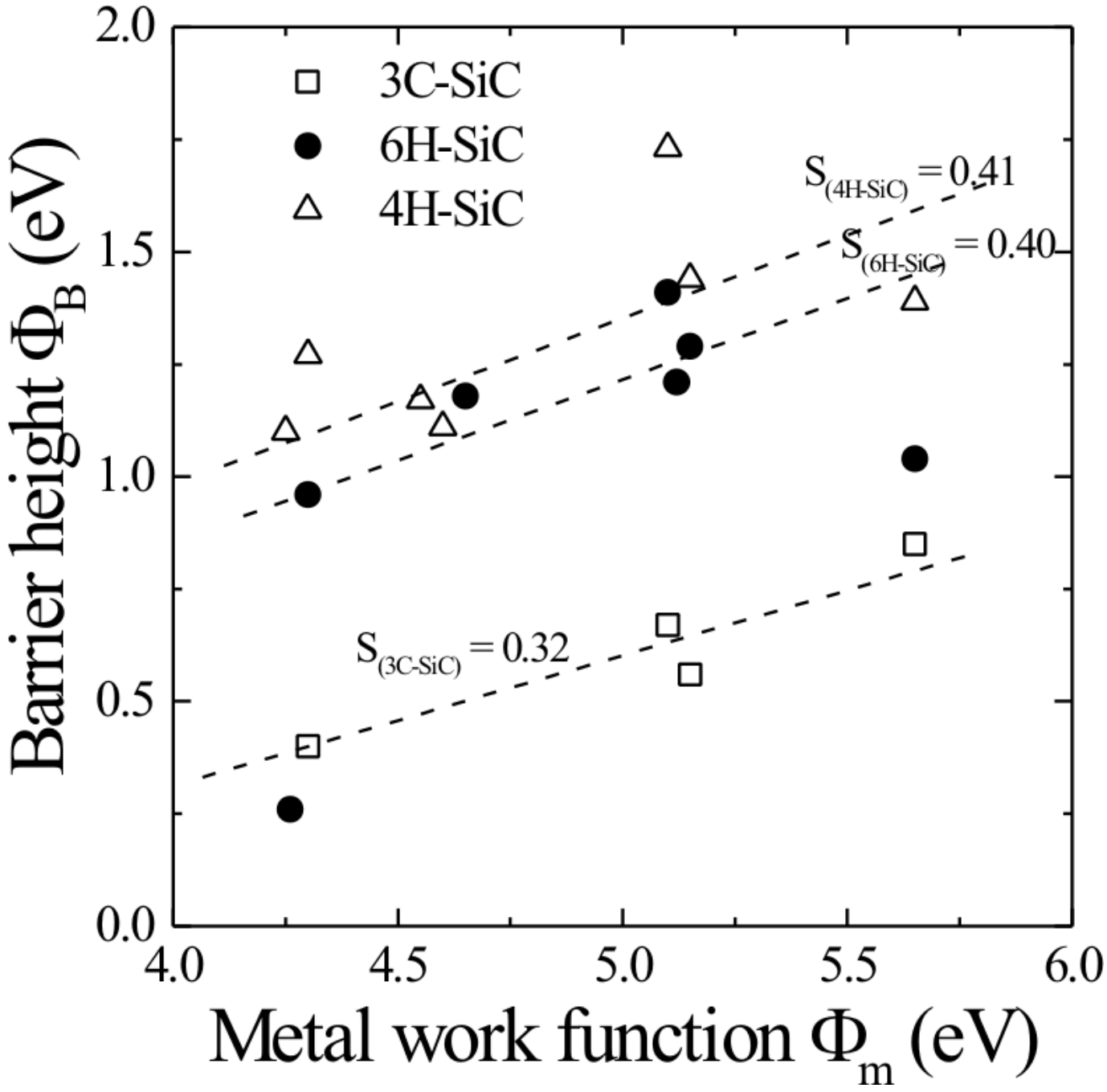


Figure 1 (figure1.tif)

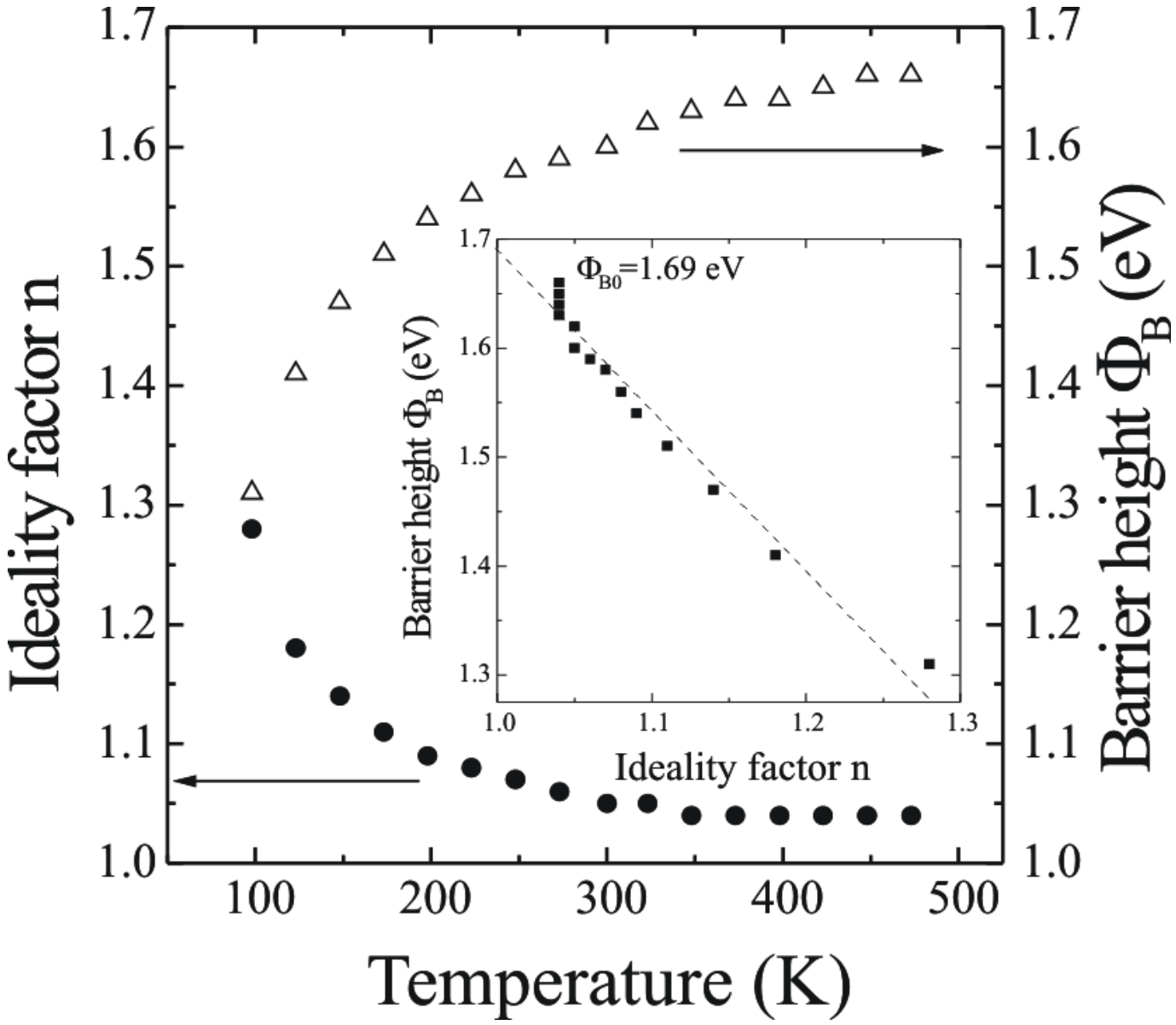


Figure 2 (figure2.tif)

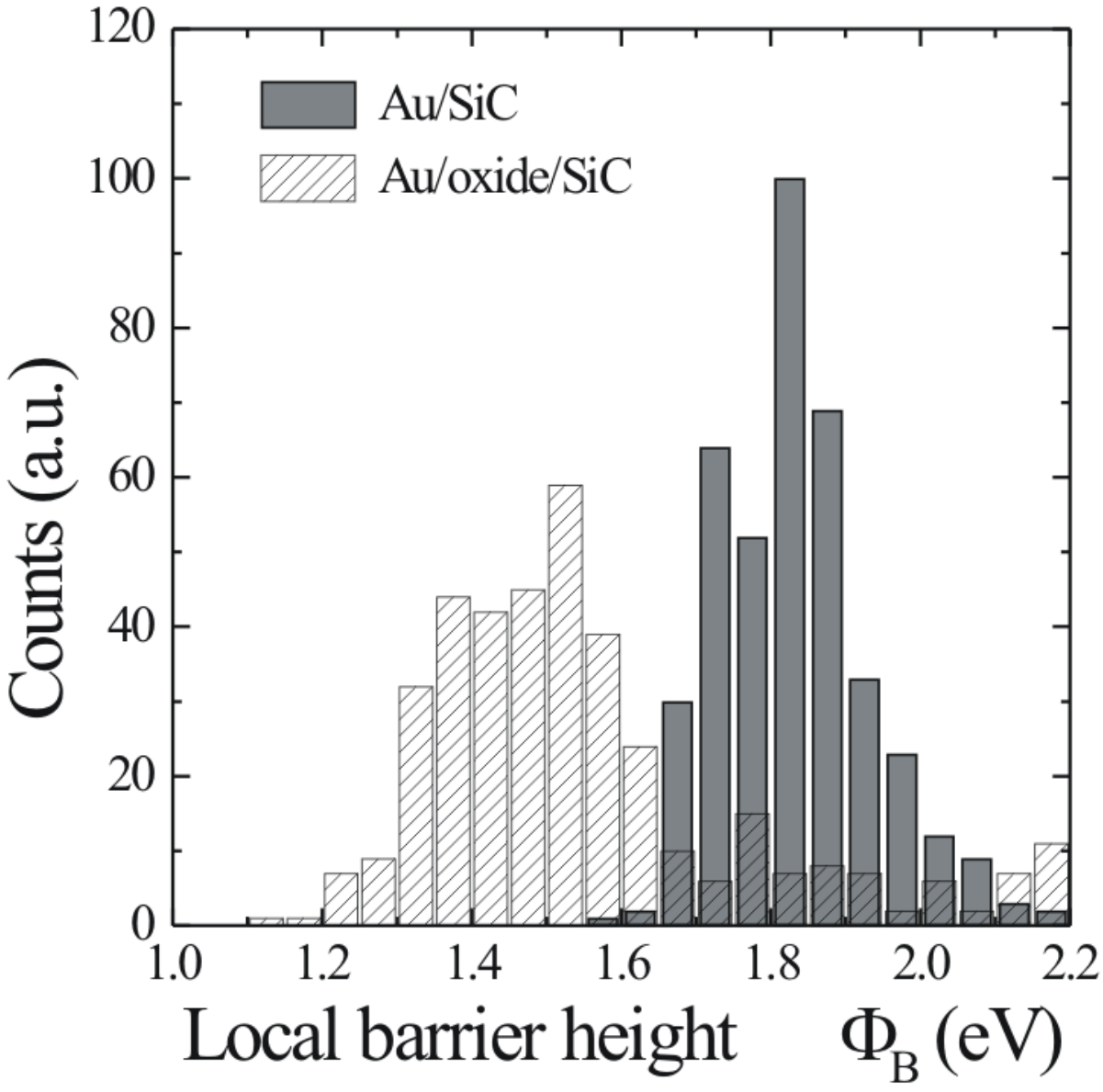
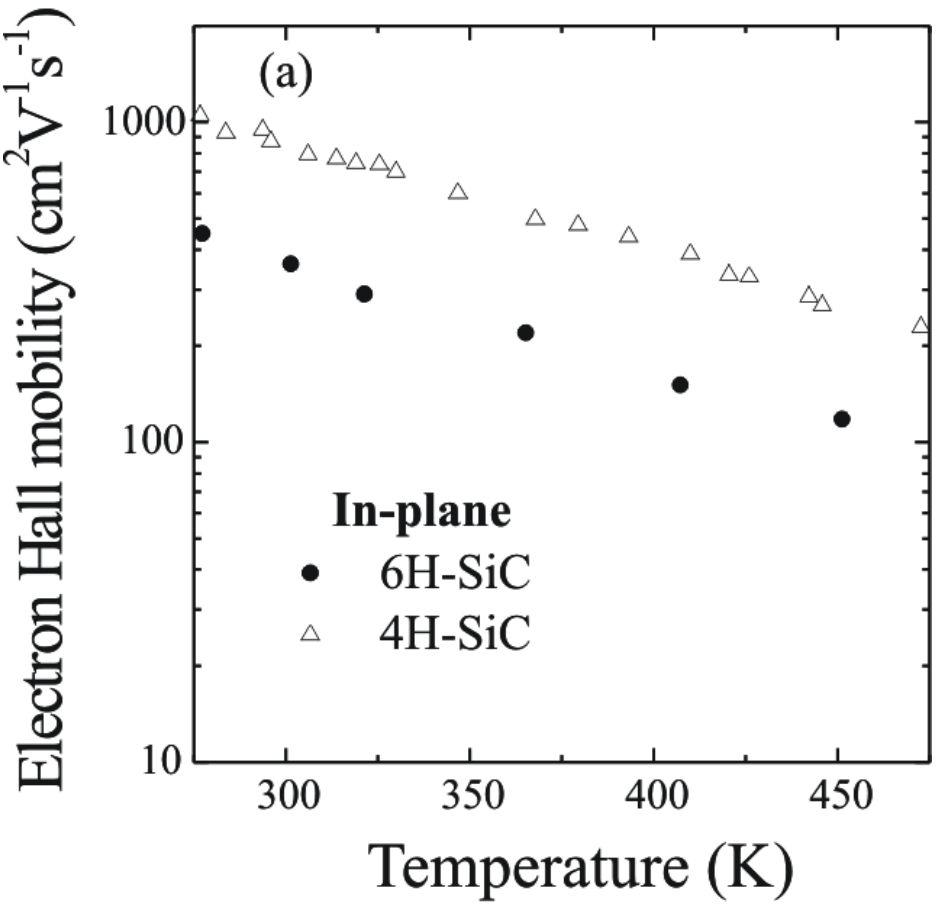


Figure 3 (figure3.tif)



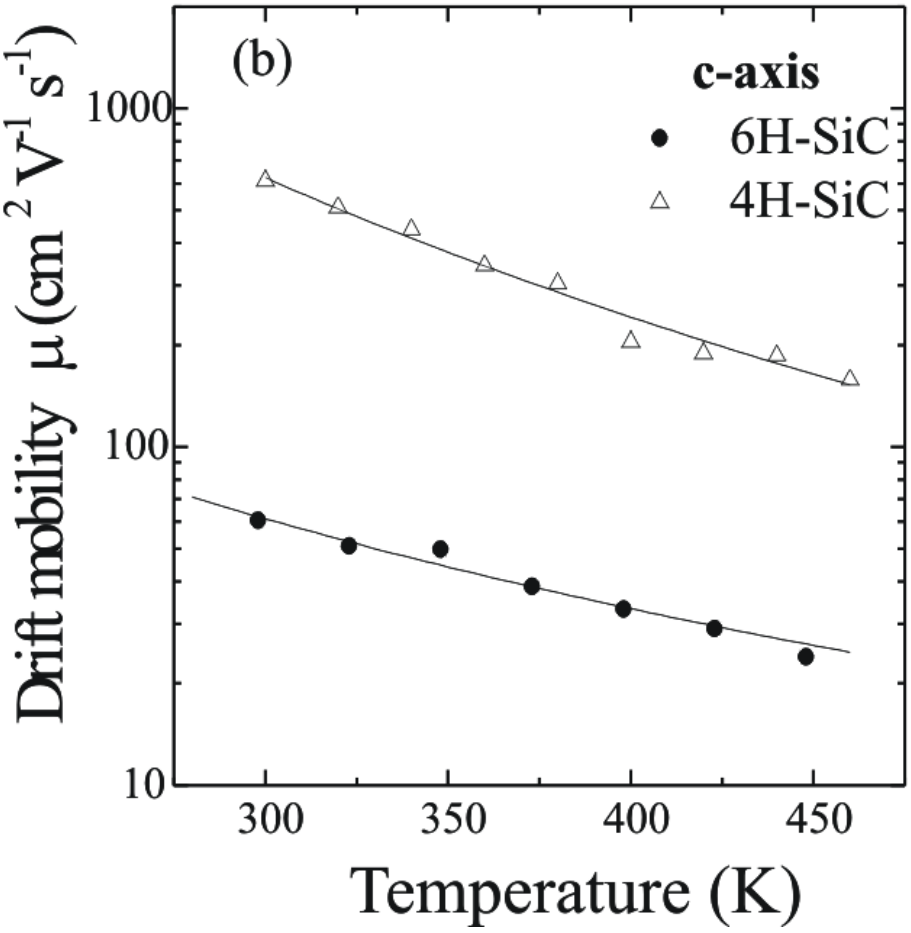


Figure 4 (figure4.tif)

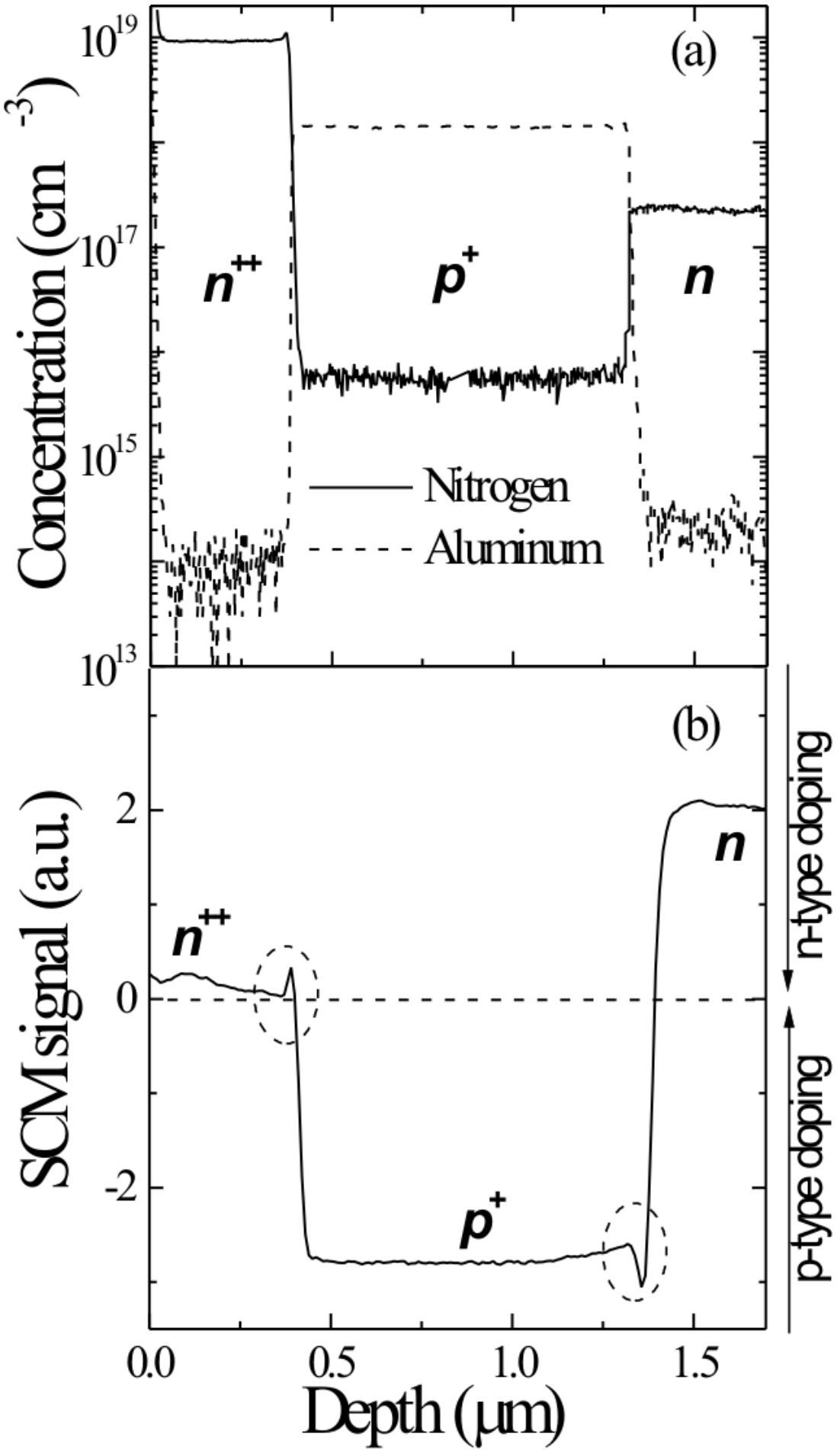


Figure 5 (figure5.tif)

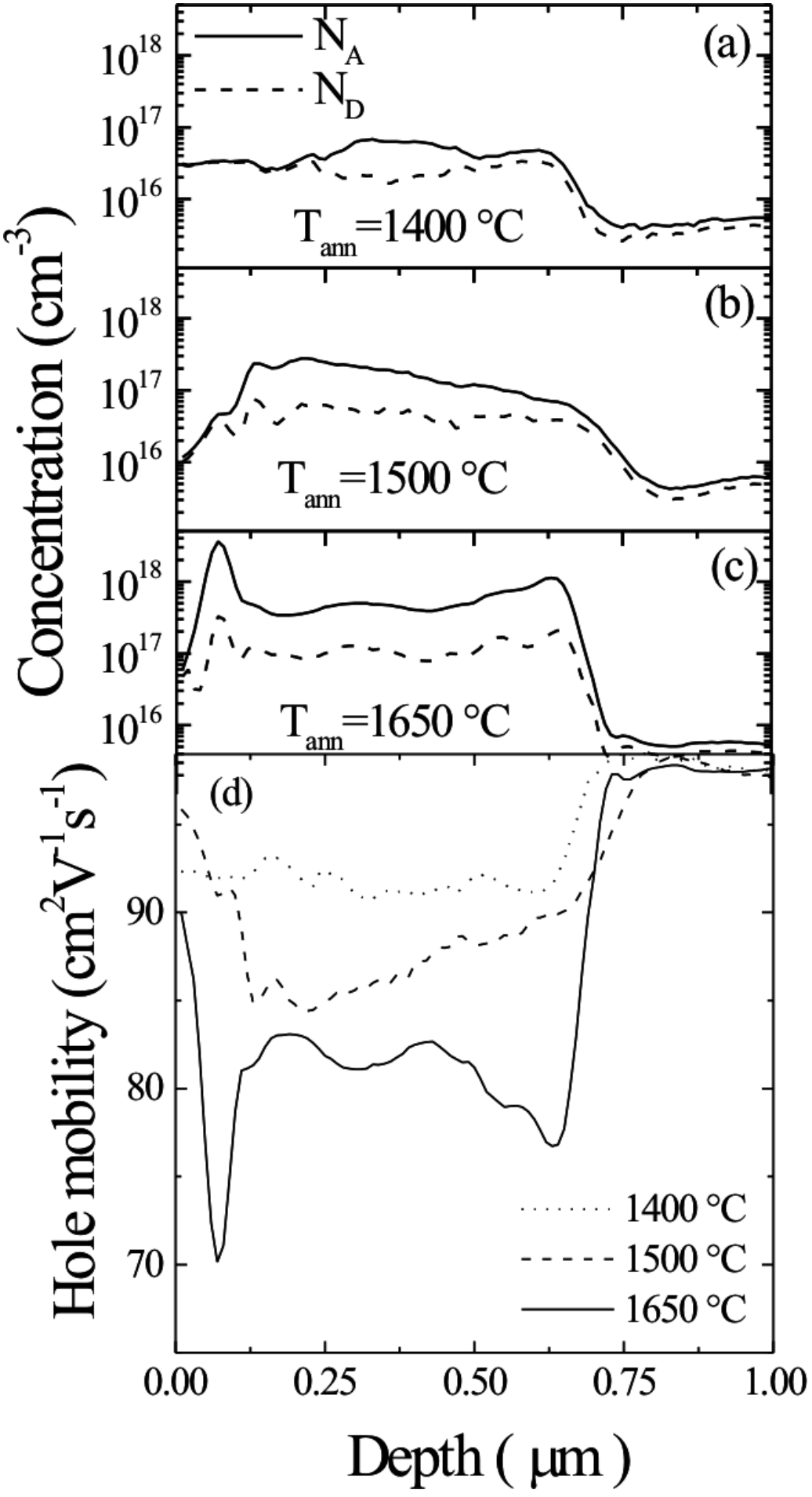


Figure 6 (figure6.tif)

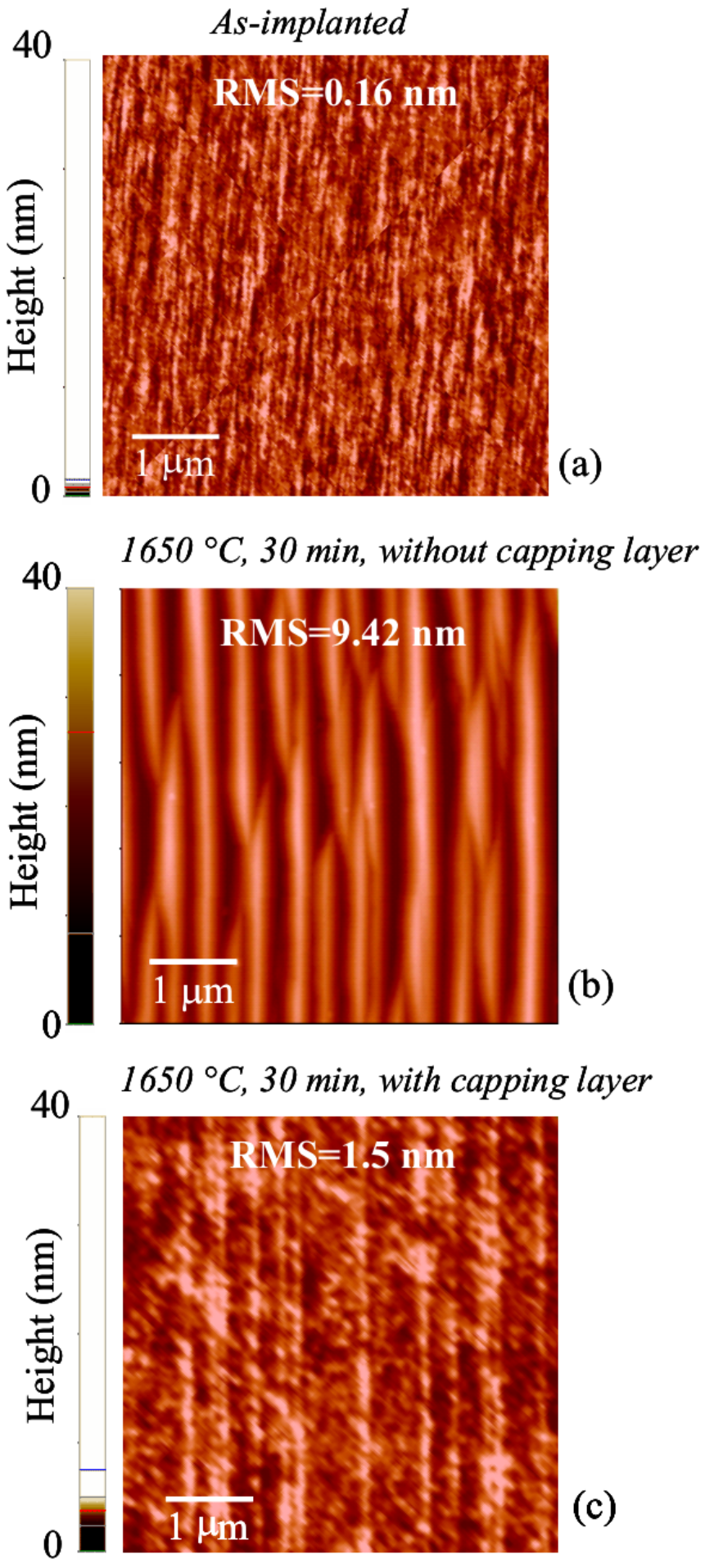


Figure 7 (figure7.tif)

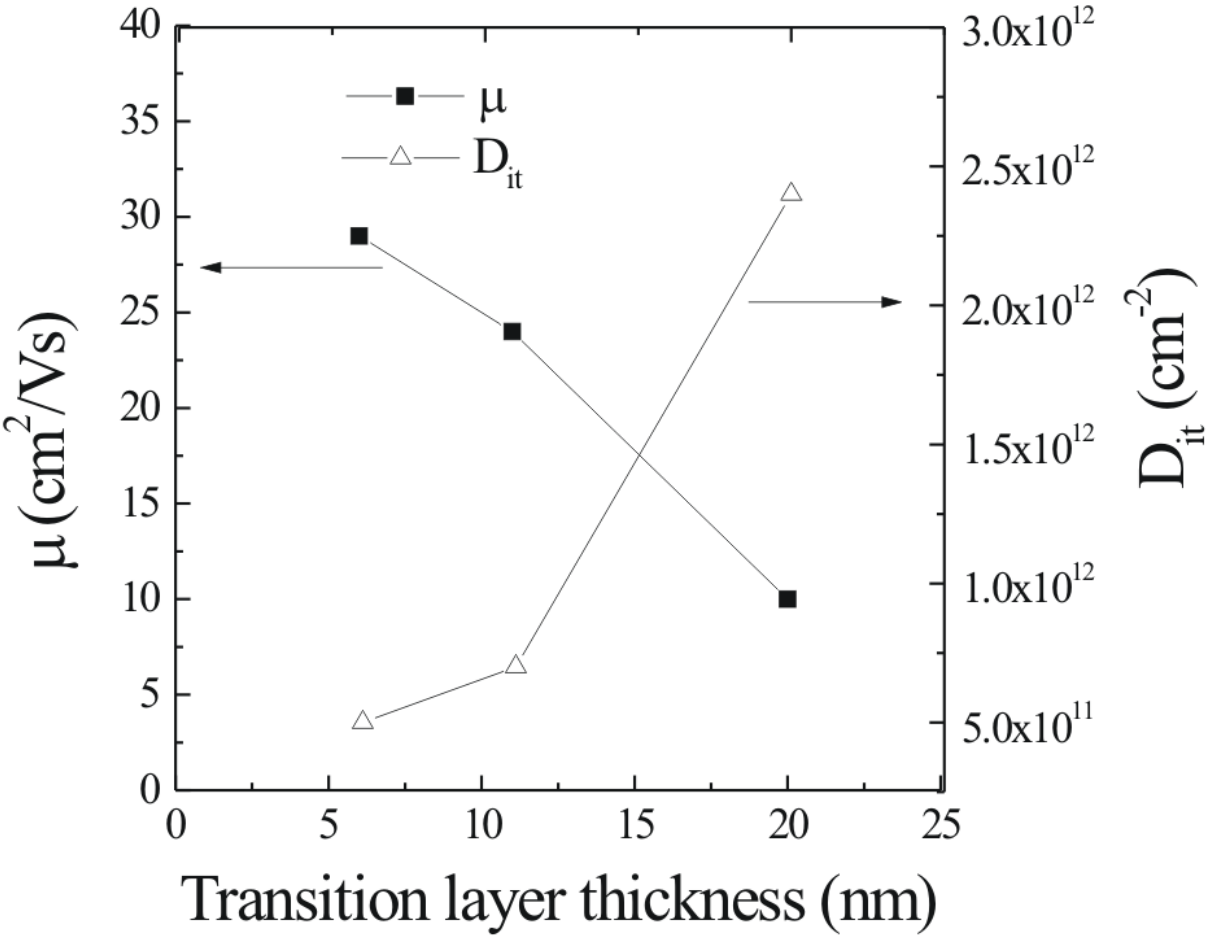


Figure 8 (figure8.tif)

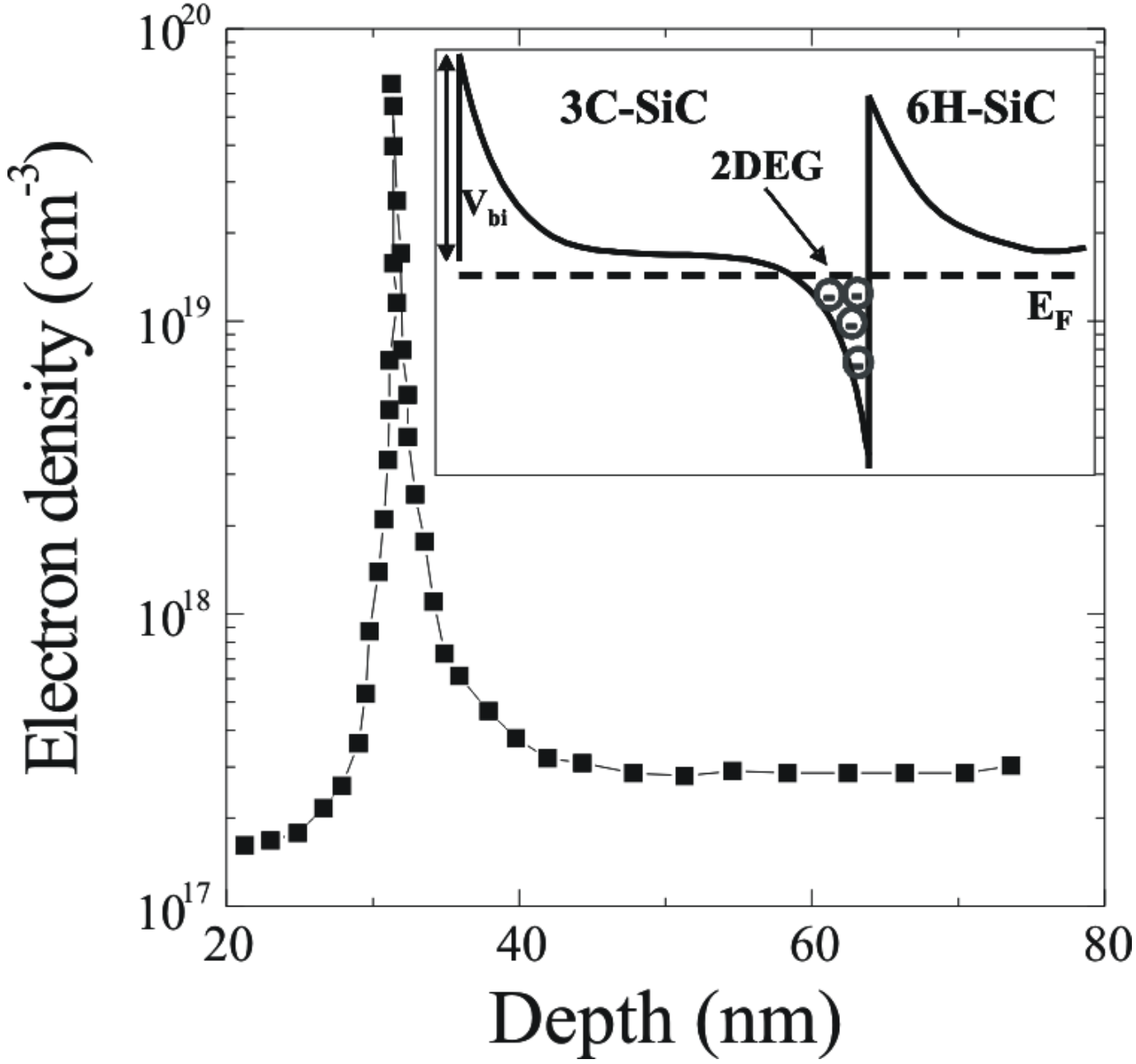
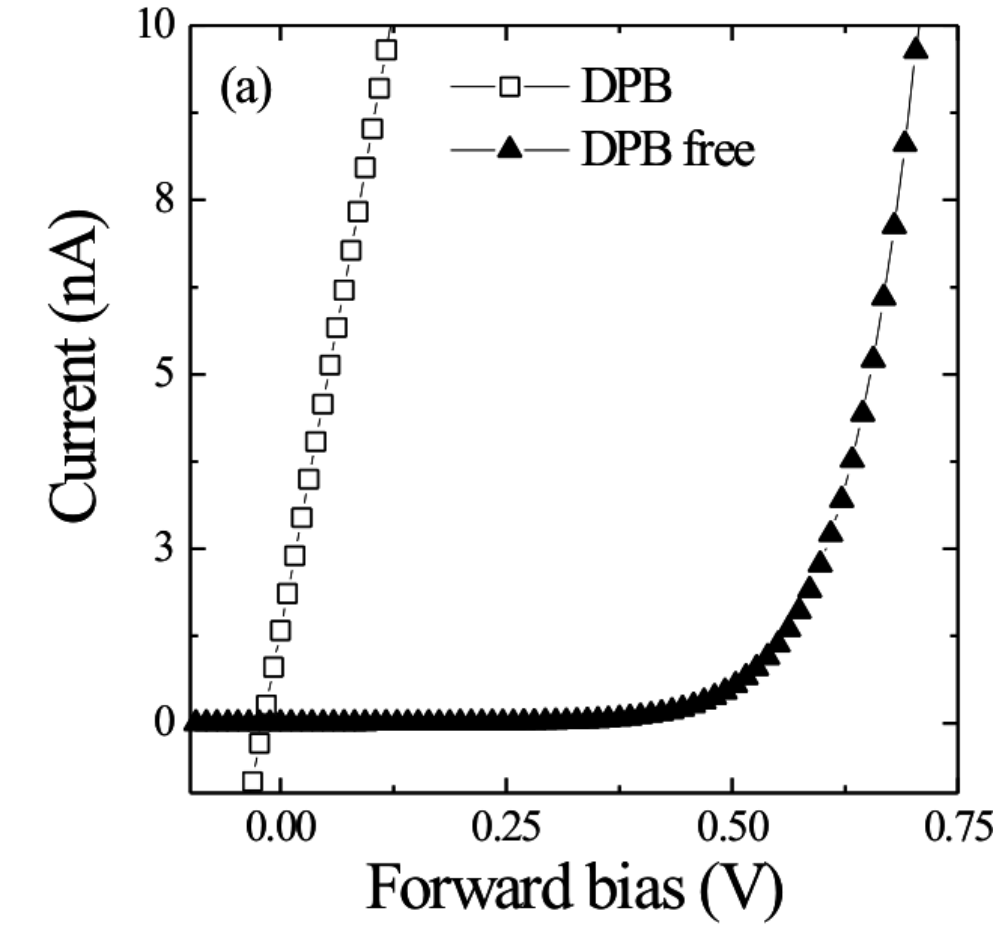


Figure 9 (figure9.tif)



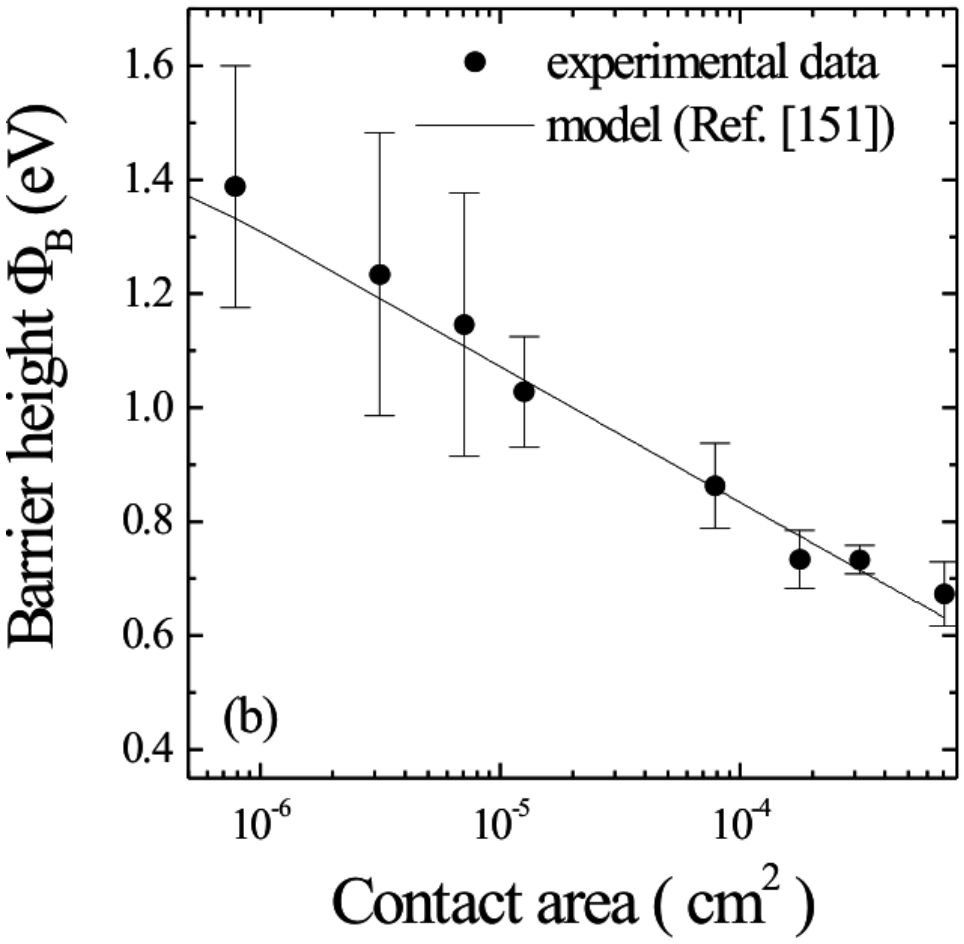


Figure 10 (figure10.tif)